Noise-driven architectures toward beyond CMOS LSIs with failure-prone nano-electronic devices

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Abstract:
We investigated the implications of noises in a 1-bit analog-to-digital (pulse-density) converter consisting of single-electron devices. The proposed circuit architecture exploits fabrication mismatches (noises) to improve the performance of the pulse-density modulator. The modulator consists of three single-electron circuits that receive the same input and are connected to a common output. The output is inhibitorily fedback to the three circuits through a capacitive coupling, tuned to obtain a winners-share-all operation. The circuit performance was evaluated through Monte-Carlo based computer simulations. We demonstrate that the proposed circuit possesses noise-shaping characteristics, where the output signal and noises are separated into low and high frequency bands, respectively. This significantly improved the signal-to-noise ratio (SNR) by 4.34 dB in the noisy network, as compared to the case where the feedback and noises were not employed. The noise-shaping properties are as a result of i) the inhibitory feedback between the output and the single-electron circuits, and ii) noises (originating from device fabrication mismatches and thermally induced tunneling events) introduced into the network.

1. Introduction

Scaling of semiconductor devices has been the primary driving force behind enhancing the performance of LSI processors and systems, in terms of increasing computation speed and integration densities which translate to diversified functionality. However, in recent years, the physical sizes of transistors have reached the deep sub-nano sizes, where high degrees of process variations and undesirable internal (and or external) noises associated with nanoscale properties are inevitable. These noises dramatically reduce the reliability of electronic devices, posing critical challenges to circuit designers. Getting rid of these nanoscale characteristics would involve introducing error-detecting circuits into the system, which leads to advanced complexity, and design tradeoffs in using high integration capacities available to the circuit designer.

In this work, we propose a novel circuit architecture consisting of single-electron devices which exploits, instead of mitigating, these noises to improve the signal-to-noise ratio in a 1-bit analog-to-digital converter. The circuit architecture is inspired by information coding mechanisms in biological neural networks that convert analog input signals into spike densities (digital-pulse streams) in the time domain[1].

2. Model and Implementation

Fig.1 (a) shows the model of the proposed circuit, consisting of three circuit elements (or neurons). The neurons receive the same analog input and produce (fire) digital pulses toward the global inhibitor. The output is fed-back to the three elements through inhibitory synapses denoted by shaded circles in the network. The model is implemented with single-electron oscillators[2] (fig. 1(b)) that receive the same analog input and release pulses toward the output terminal when the analog input voltage exceeds the threshold. Noises emanating from fabrication fluctuations are modeled by introducing variations in the series resistances, while thermal noises were introduced by increasing the operation temperature.

3. Results

Fig. 2(a) shows the ISI distribution of firing events in the whole network with an input voltage of 7.85 mV. The histogram for the coupled network (with noises) shows a Gaussian-like distribution, while that of the

uncoupled network (without noises) shows a Poisson-like distribution.

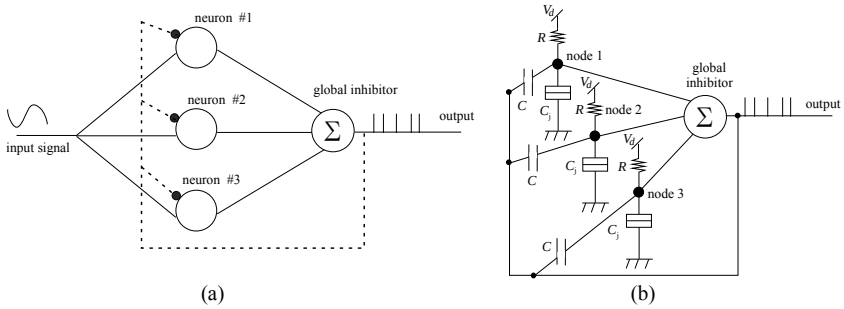

Fig.1 (a) Model (b) Circuit structure. Noises are introduced as variations in values of R

Fig. 2(b) shows the power spectra for the coupled and uncoupled networks. The three neurons in both networks were fed with a sinusoidal input $V_d = 7.85 + A\sin(2\pi ft)$, where amplitude $A = 2.5$ mV, frequency $f =$ 100 MHz. The signal-to-noise ratio in the noisy network improved by 4.34 dB, as compared to the noiseless network.

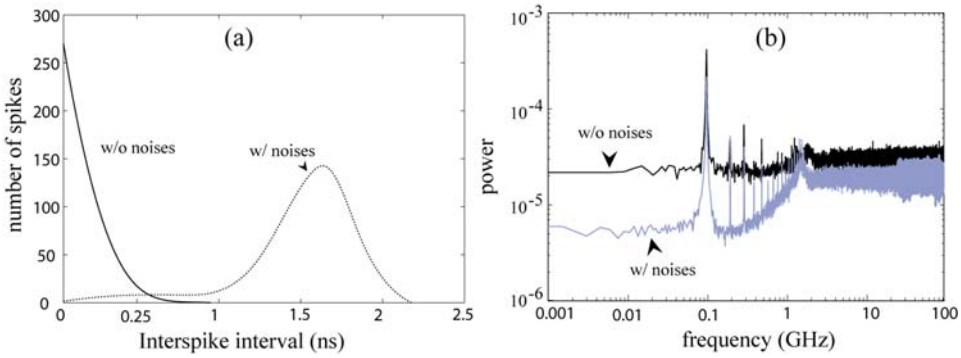

Fig. 2 Simulation results (a) Inter-spike intervals (b) Power spectra

These results could be explained as follows. Neurons in the noiseless network tend to fire at the same timing as opposed to the noisy network, where firing neurons fired rather randomly because of the variations in firing time constants, reducing the probability of neurons attaining the firing threshold at the same time. In addition, firing in either of the network neurons reduced the probability of others from firing by deducting a certain amount of voltage from the nodes. Consequently, these two collectively contributed to the improvement of the inter-spike intervals distribution from a Poisson- (in the noiseless network) to a Gaussian-like distribution in the noisy network. The same holds true for the results in (b) where the improved ISI distribution leads to an improved signal-to-noise ratio in the noisy network.

In summary, this work introduced a novel architectural approach exploiting fabrication mismatches toward realizing reliable computation with error-prone electronic devices. The concept presented here can be applied to CMOS devices facing similar fabrication challenges[3].

References:

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