2009 International Symposium on Nonlinear Theory and its Applications
NOLTA'09, Sapporo, Japan, October 18-21, 2009

A Noise-Driven Neuromorphic Pulse-Density Modulator: Experimental Results with Discrete MOS Devices

Akira Utagawa†, Tetsuya Asai, and Yoshihito Amemiya

Graduate School of Information Science and Technology, Hokkaido University.
Kita 14, Nishi 9, Kita-ku, Sapporo, 060-0814 Japan.
Phone:+81-11-706-7147, Fax:+81-11-706-7890
† email: utagawa@lalsie.ist.hokudai.ac.jp

Abstract—Recently, Hospedales *et al.* proposed a neural network model of "vestibulo-ocular reflex" (VOR) where a common input was given to multiple (nonidentical) spiking neurons accepting uncorrelated temporal noises, and the output was represented by the sum of the neurons' outputs. Although the function of the VOR network is equivalent to pulse-density modulation, the neurons' non-uniformity and temporal noises given to the neurons certainly improved the output spike's fidelity to the analog input. In this paper, we propose a CMOS analog circuit implementing the VOR network that exploits non-uniformity of real MOS devices. Through extensive laboratory experiments using discrete MOS devices, we show that the output's fidelity to the input pulses is certainly improved by the multiple neuron circuits where the non-uniformity is naturally embedded into the devices.

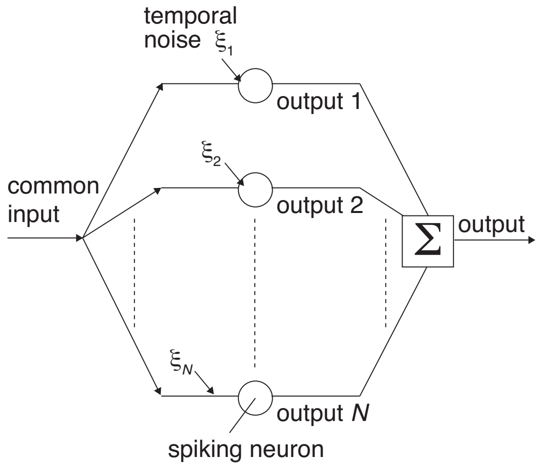


Figure 1: Neural network model of VOR

1. Introduction

Charge-based ultra-low-power analog circuits may suffer from physical limits of their temporal responses because the present designing strategy is to decrease the amount of the power-supply voltage or that of the bias currents [1]. Is there a possible way to construct an analog circuit that can perform high-speed information processing with slow-but-low-power semiconductor devices? Neural networks seem to be a possible choice because they perform high-speed parallel information processing with slow neural elements as compared to present semiconductor devices. Recently, Hospedales *et al.* reported that in a neural network model of "vestibulo-ocular reflex" (VOR) non-uniformity of neurons and temporal noises given to the neurons certainly improved the net-output's fidelity to the analog input [2]. Figure 1 shows a simplified schematic of the model. A common input is given to N spiking neurons that accept uncorrelated temporal noises ξ_i ($i = 1, 2, \cdots, N$), and the output is represented by the sum of the neurons. When the neurons are identical and no noises are applied to the network, all the neurons would generate synchronous spikes. On the other hand, when they accept temporal noises (or the neurons are not identical), they no longer can generate synchronous spikes. Here it should be noticed that the averaged inter-spike interval of the noisy network's output is roughly N-times larger than that of the synchronous one. Therefore, the response (firing) frequency of the noisy network is always larger than that of the noiseless network, which results in the fidelity improvement to the input.

Inspired by these interesting results, we here propose a CMOS circuit implementing the VOR network that exploits non-uniformity of real MOS devices. Through extensive laboratory experiments using discrete MOS devices, we show that the output's fidelity to the input pulses is improved by the multiple neuron circuits where the non-uniformity is naturally embedded into the devices.

2. A CMOS circuit implementing a neural network model of VOR

Based on the VOR model proposed by Hospedales *et al.* [2], we developed a network circuit consisting of multiple MOS neuron circuits. In the network, we use an excitable neuron circuit based on the Wilson-Cowan oscillator circuit [3, 4]. Figure 2 shows a schematic of the neuron circuit. The circuit consists of a standard operational amplifier (OP-AMP) and a pMOS operational transconductance amplifier (OTA) acting as a comparator. In Fig. 2, u_i and v_i represent the system variables, V_{bias} the bias voltage, C_1

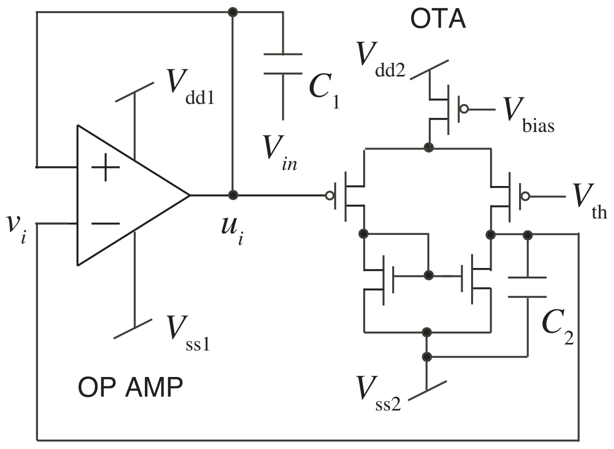


Figure 2: Wilson-Cowan neuron circuit.

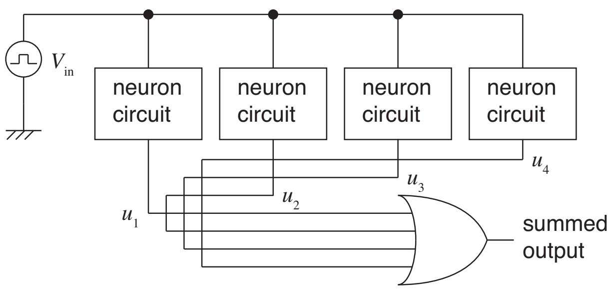
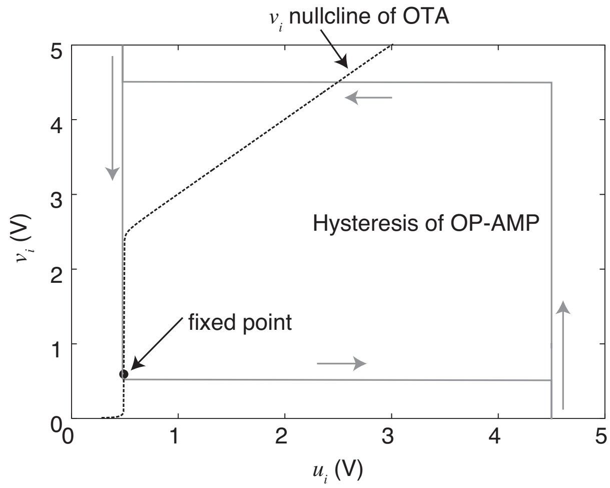


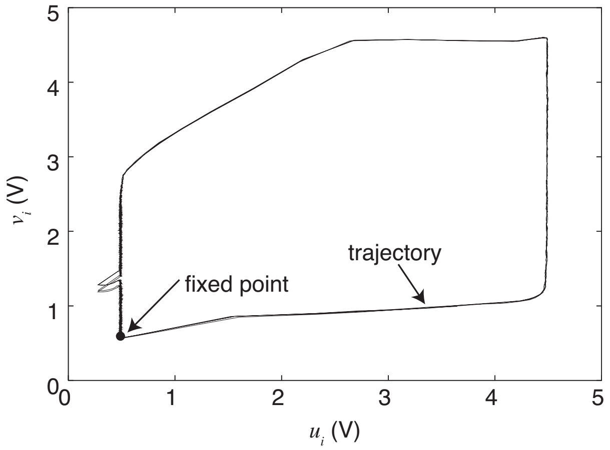
Figure 3: VOR network with four neuron circuits.

and C_2 the capacitance, $V_{dd1,2}$ and $V_{ss1,2}$ the supply voltages. Since the OP-AMP has a positive feedback loop (in node u_i), there exists hysteresis between the negative input (v_i) and the output (u_i) [3]. Consequently, the OP-AMP acts as a hysteresis inverter when u_i and v_i are regarded as the output and input, respectively. If u_i is increased by temporal input V_{in} and u_i exceeds V_{th} of the OTA, v_i approaches to V_{dd2}, which results in $u_i \rightarrow V_{ss1}$ with time delay due to the hysteresis. Therefore as long as V_{th} is set at lower than V_{ss1}, the circuit exhibits an excitable behavior. In contrast, the circuit exhibits an oscillatory one when $V_{th} > V_{ss1}$. It should be noted that the refractory period of this neuron circuit is tuned by C_2 because the output current of the OTA is charged by C_2 to generate v_i, and if v_i is high, u_i could not approach to V_{dd1} due to the hysteresis of the OP-AMP.

Figure 3 show a schematic of a VOR network circuit consisting of four neuron circuits. A common input (V_{in}) is given to the neuron circuits. Since the neuron's output is represented by spikes (logical "0" for resting and refractory states, "1" for firing state), the summed output can be represented by logical OR of the neuron's output. It should be noted that in real world experiments each neuron circuit has a slightly different physical parameters. Therefore non-uniformity in the original VOR model is naturally embedded into the circuits.



(a) Nullcline of OTA and hysteresis of OP-AMP



(b) Closed trajectory of single neuron circuit

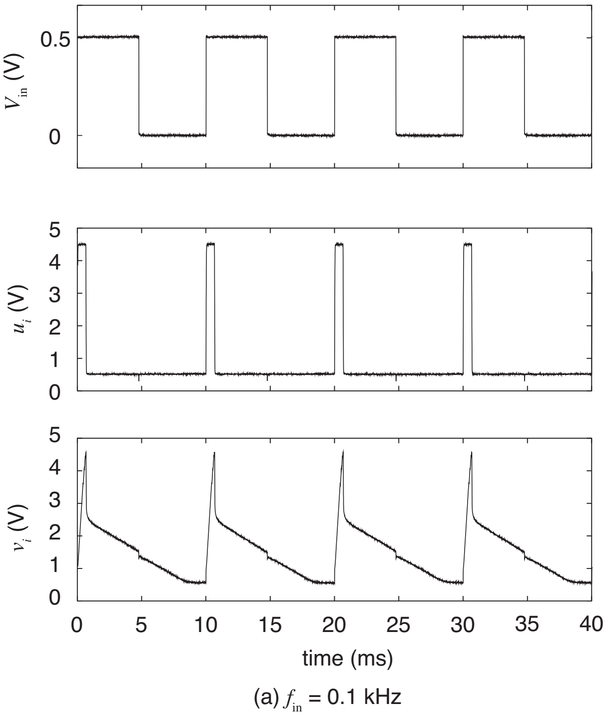
Figure 4: Trajectories and nullclines of single neuron circuit (experimental results).

3. Experimental results

In the following experiments, we used discrete devices ($C_1 = C_2 = 0.1$ μF, $V_{dd1} = 4.5$ V, $V_{ss1} = 0.5$ V, $V_{dd2} = 5$ V, $V_{ss2} = 0$ V, $V_{bias} = 2.8$ V). We used nMOS-FET (2SK1398) and pMOS-FET (2SJ184) for the OTA, and used LMC-6482 for the OP-AMP.

Figure 4(a) shows a v_i-nulllcline of the OTA and hysteresis curves of the OP-AMP, and Fig. 4(b) shows trajectories of a single neuron circuit. V_{th} was set to 0.5 V so that the neuron circuit is stable (in excitatory mode) when V_{in} is zero. When a voltage pulse (0-0.5 V, pulse width: 50 ms) was applied to V_{in}, a closed trajectory along with the hysteresis curve and the v_i-nulllcline was obtained, as shown in Fig. 4(b), which exhibits the correct excitatory operation of the neuron circuit.

Figure 5 shows temporal responses of the single neuron circuit accepting two different V_{in}s ($f_{in} = 0.1$ kHz and 0.2 kHz). When f_{in} was 0.1 kHz [Fig. 5(a)], the neuron circuit



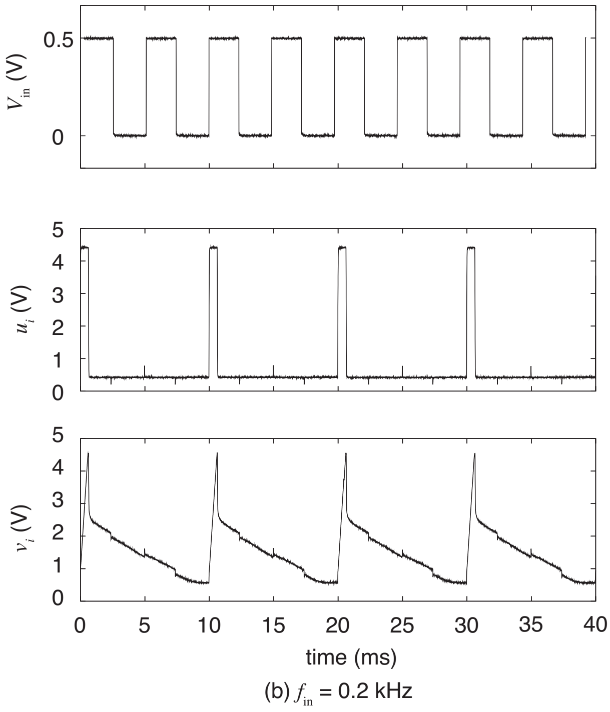


Figure 5: Responses of single neuron (experimental results).

generated one spike when one pulse was applied, which indicated that the circuit could respond to all the input pulses. On the other hand, when f_{in} was 0.2 kHz [Fig. 5(b)], the circuit generated spikes once every two input pulses, which results in the low fidelity (the circuit could not respond to all the input pulses). To visualize the relationship between the frequency of input pulse (f_{in}) and the generated spike (f_{out}), we plotted the f_{in}-f_{out} characteristics of the single neuron circuit in Fig. 6 ("×" represents the experimental raw data, and the dashed line is the approximated curve). From this figure, we could confirm that the circuit could respond to all the input pulses (at maximum fidelity) when $f_{in} < 0.1$ kHz if the present parameter sets were used.

Now let us evaluate the effect of noises (non-uniformity of neuron circuits) using our network circuit. Figure 7 show the temporal responses of the network. In this experiment, we applied input pulse of $f_{in} = 0.6$ kHz [Fig. 7(a)] which is six-times larger than the operational limit of the single neuron circuit (0.1 kHz). Figure 7(b) shows each neuron's firing event (+, ×, ∗ and □ represents firings of neurons 1, 2, 3 and 4). Apparently, each neuron could not respond to all the input pulses. Figure 7(c) shows the summed output of the four neuron circuits (vertical lines represent the summed firings). As compared to each neuron's firing, firing rates of the summed output were increased by about four times, and the response rate to the input pulse was certainly increased by about four times, which indicates the fidelity improvements in the non-uniform network. Figure 8 plots the f_{in}-f_{out} characteristics of the network circuit

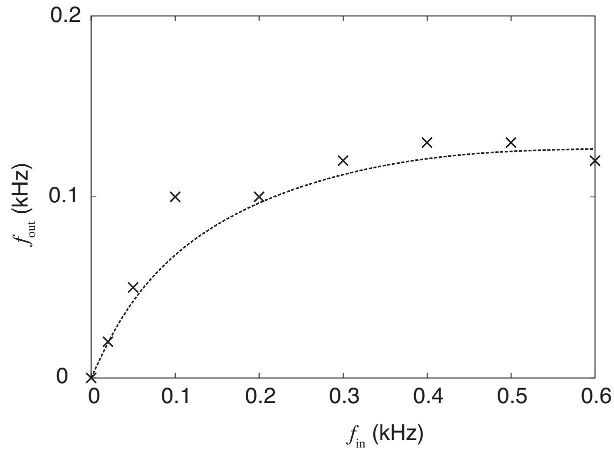


Figure 6: Input-output frequency characteristics of single neuron circuit.

(filled circles) as well as that of the single neuron circuit ("×"). This figure clearly shows that the network circuit could respond to all the input pulses (at maximum fidelity) when $f_{in} < 0.4$ kHz. From this figure, we could confirm that the fidelity was improved by four times and the degree of the improvements is proportional to the number of neurons in the network circuit.

In [5], we have already demonstrated that an inhibitory neural network performing noise-shaping pulse-density

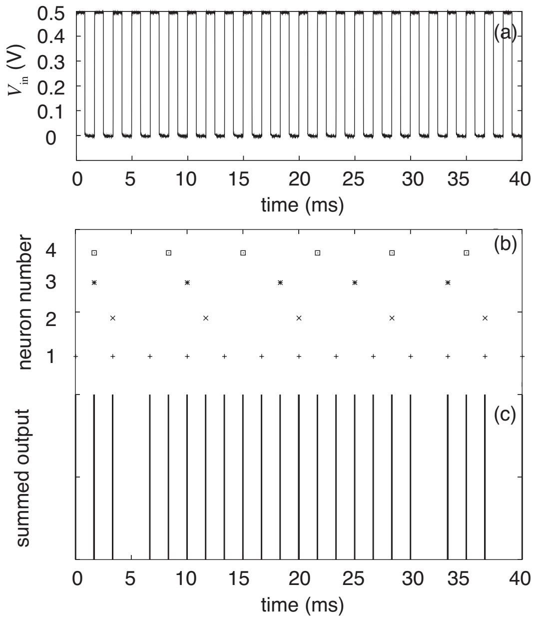


Figure 7: Responses of noisy VOR network circuit.

modulation took the same strategy where multiple neurons accept a common input and uncorrelated noises as well as different synaptic weights between the input and the neurons. The neuron's outputs were summed and negatively fed backed to the neurons. This negative feedback was a key for the noise-shaping pulse-density modulation. Apparently, if the number of neurons were increased in the network, the cutoff frequency was shifted toward high, as in our present results. So far we have demonstrated only the fidelity of the VOR network, however, we should evaluate the responses of the network for sinusoidal inputs, i.e., we should calculate correlation values between the sinusoidal inputs and DA-converted values of the pulse-modulated outputs, to construct a useful pulse-density modulator based on our noise-driven circuits.

4. Conclusion

We developed a noise-driven pulse-density modulator having high fidelity to input signals based on a neural network model of vestibulo-ocular reflex. We constructed a network circuit consisting of multiple CMOS neuron circuits and a standard OR logic circuit. Through extensive laboratory experiments, we showed that the fidelity to the input pulses was certainly improved by the multiple neuron circuits where the non-uniformity was embedded into the MOS devices. We confirmed that a single neuron circuit could respond to input pulses of up to 0.1 kHz, while when four neuron circuits were employed in the network, the circuit could respond to input pulses of up to 0.4 kHz which is four-times larger than the upper limit of the single neuron circuit.

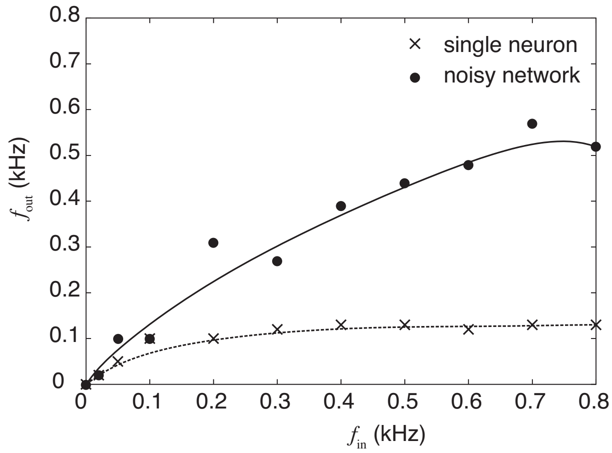


Figure 8: Input-output frequency characteristics of single neuron circuit and noisy VOR network circuit.

Acknowledgment

This study was supported by a Grant-in-Aid for Scientific Research on Innovative Areas [20111004] from the Ministry of Education, Culture Sports, Science and Technology (MEXT) of Japan.

References

[1] M. Sanduleanu and E. van Tuijl, *Power Trade-offs and Low Power in Analog CMOS ICs*, Kluwer Academic Publishers, Dordrecht, Netherlands, 2002.

[2] T.M. Hospedales, M.C.W. van Rossum, B.P. Graham, and M.B. Dutia, "Implications of noise and neural heterogeneity for vestibulo-ocular reflex fidelity", *Neural Computing*, vol. 20, no. 3, pp. 756–778, 2008.

[3] T. Asai, Y. Kanazawa, T. Hirose, and Y. Amemiya, "Analog reaction-diffusion chip imitating the Belousov-Zhabotinsky reaction with Hardware Oregonator Model," *International Journal of Unconventional Computing*, vol. 1, no. 2, pp. 123–147, 2005.

[4] G.M. Tovar, T. Asai, T. Hirose, and Y. Amemiya, "Critical temperature sensor based on oscillatory neuron models," *Journal of Signal Processing*, vol. 12, no. 1, pp. 17–24, 2008.

[5] A. Utagawa, T. Asai, T. Hirose, and Y. Amemiya, "An inhibitory neural-network circuit exhibiting noise shaping with subthreshold MOS neuron circuits," *IEICE Transactions on Fundamentals of Electronics, Communications and Computer*, vol. E90-A, no. 10, pp. 2108–2115, 2007.