A 0.02-to-2-MHz Tunable Clock Reference Circuit for Intermittent Pulse Generators

Ken Ueno, Tetsuya Asai, and Yoshihito Amemiya

Department of Electrical Engineering, Hokkaido University
Kita 14, Nishi 9, Kita-ku, Sapporo, Hokkaido, 060-0814 Japan
Phone: +81-11-706-7149, Fax: +81-11-706-7890
E-mail: k_ueno@labsie.ist.hokudai.ac.jp

ABSTRACT
An ultra-low power clock reference generator has been developed using a 0.35-µm CMOS parameters. The circuit is based on a simple frequency-locked loop technique with no inductors, quartz resonators, and MEMS oscillators. Theoretical analyses and measurement results showed that the clock frequency could be controlled over a frequency range of 20 kHz - 2 MHz. The circuit showed a temperature coefficient of 170 ppm/C, a line regulation of 1%/V, and a power dissipation of 3 µW when operated at 200 kHz. A process sensitivity (σ/µ) was 5% without calibration technique. The proposed clock generator can be used as a reference clock for intermittent operation for use in subthreshold-operated, power-aware LSIs.

Keywords: CMOS, Reference clock, Frequency-locked loop, Ultra-low power, Power-aware

1. Introduction

The development of ultra-low power LSIs is one of the promising research areas in microelectronics. These LSIs will be useful for use in power-aware LSI applications such as smart sensor networks, portable mobile devices, and implantable medical devices [1], and they have to operate for a long time with limited energy resources such as microbatteries or energy-scavenging power sources [2]. As a step toward designing such LSIs, we are now developing a smart sensor device as shown in Fig. 1. The device consists of sensors [3]-[4], AD/DA converters, digital signal processors, memories, reference circuits [5]-[7], power supply circuits [8], and transceiver circuits. Microwatt operation requires that, all of the circuits in the LSI are operated in the subthreshold region of MOSFETs [9], and that the main system of the LSI is operated intermittently under the control of an on-chip reference clock circuit. Intermittent operation contributes to a drastic reduction in the power consumption of the LSI.

This paper focuses on a clock reference circuit for power-aware LSIs. Many clock reference circuits have been reported recently [10]-[12] but they are unsuitable for use in power-aware LSIs because of their large power dissipation (several milliwatts or more), large surface area (over 1 mm²), and use of MEMS technology, which however is incompatible with standard CMOS processes. Therefore, modified low-power clock reference circuits with standard CMOS process have been reported [13]-[16]. However, these circuits have some problems. For example, their power dissipations are still large, they require high precise temperature-insensitive reference voltages and currents, and their clock frequencies are too high (over 2 MHz); these are inconvenient for use in ultra-low power LSIs. Moreover, the effect of the process variations on the reference clock was not showed in detail.

To solve these problems, we developed a clock ref-
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Fig. 2. Block diagram of our clock reference generator.

circuit that can be operated with microwatt-level power dissipation, and controlled over a wide frequency range of 20 kHz - 2 MHz. The circuit makes use of a frequency-locked loop and generates a clock frequency that is insensitive to temperature and the supply voltage.

2. Circuit configuration

Figure 2 shows a block diagram of our clock reference generator. The circuit generates a reference clock using a frequency-locked loop technique. It consists of a bias current circuit, a current comparator, a voltage-controlled oscillator (VCO), and a frequency-to-current converter, and these circuits form a feedback loop. The current comparator detects the difference between the reference current and the output current of the frequency-to-current converter and generates the output voltage proportional to the difference. The VCO accepts the output voltage and produces oscillation pulses with a frequency dependent on output voltage. The frequency-to-current converter accepts the oscillation pulses and generates the output current proportional to the frequency. Then the current comparator again compares currents and output current to produce a readjusted output voltage. This feedback operation is repeated to make equal to . The resulting clock frequency is independent of temperature and power supply voltage.

Figure 3 shows the entire circuit configuration of our clock generator including a intermittent pulse generation circuit. The following sections describe the operation of the generator in detail.

2.1 Bias Current Circuit

The bias current circuit consists of a pMOSFET and a resistor . A resistor is implemented as off-chip components with little temperature dependence to adjust the bias current . The reference current is given by

\[ I_{BIAS} = \frac{V_{DD} - V_{GSP}}{R_{REF}}, \]

where is the gate-source voltage of pMOSFET. Therefore, the bias current that is dependent on the resistor value can be obtained.

2.2 Current Comparator

The current comparator is a commonsource circuit used to detect the difference between reference current and output current of the frequency-to-current converter. It generates output voltage proportional to the difference between the two. The capacitor is added to stabilize the circuit operation.

2.3 Voltage Controlled Oscillator

The VCO consists of seven current-starved inverters connected in a ring that is operated in the subthreshold region of MOSFET. The circuit is used for producing oscillation pulses that are dependent on output voltage of the current comparator. Oscillation frequency depends on applied current and is given by

\[ f_{REF} = \frac{I_b}{2mA C_L V_{DD}} \]

\[ = \frac{I_0}{2mA C_L V_{DD}} \exp \left( \frac{V_{DD} - V_{OUT} - V_{TH}}{\eta V_T} \right), \]

where is the number of inverters in the oscillator, is a load capacitance for each inverter, is a delay fitting parameter [17], \( I_0 = (W/L)\mu C_{OX}(\eta - 1)V_T^2 \) is a process dependent parameter, is the thermal voltage, is the threshold voltage of MOSFET, and is the subthreshold slop factor [3]. Oscillation frequency depends on output voltage.

2.4 Frequency to Current converter

The frequency-to-current converter consists of a diode-connected pMOSFET and a switched-capacitor resistor. The circuit is used to produce output current proportional to oscillation frequency of the VCO. The switched-capacitor resistor consists of capacitor and two switches (sw1, sw2) driven with the oscillation pulses from
the VCO, and operates as a resistor with a resistance of \((C_S \cdot I_{OUT})^{-1}\). Non-overlapping clock generation circuit of the frequency-to-current converter is used to prevent switches (sw1-sw2) from simultaneously being turned on. The capacitor \(C_B\) removes high-frequency noise resulting from switching operation. Therefore, output current \(I_{OUT}\) of the frequency-to-current converter is

\[
I_{OUT} = f_{REF} \cdot C_S \cdot (V_{DD} - V_{GSP}).
\]  
(3)

This current is copied into the current comparator through a current mirror. Because of the feedback operation, the circuit operates so that \(I_{OUT}\) will be equal to \(I_{BIAS}\) (i.e., Eq. (1) = Eq. (3)), and consequently, oscillation frequency \(f_{REF}\) will be

\[
f_{REF} = \frac{1}{R_{REF} \cdot C_S}.
\]  
(4)

Because the off-chip resistor \(R_{REF}\) are little temperature dependence, output frequency \(f_{REF}\) is also insensitive to temperature, and by adjusting the resistor value, the oscillation frequency can be controlled.

This way, a constant reference clock with little dependence on temperature and supply voltage can be obtained.

### 2.5 Intermittent pulse generation circuit

The intermittent pulse generation circuit consists of a digital counter and “AND” logic circuits. The circuit accepts the reference clock \(f_{REF}\) and generates intermittent pulse \(f_{INT}\). A duty ratio of the intermittent pulse depends on the number of the digital counter.

Therefore, adjusting the number of digital counter, a intermittent pulse with large duty ratio
3. Experimental Results

We fabricated a prototype chip with a 0.35-µm, 2-poly, 4-metal standard CMOS process. For flexibility, the intermittent pulse generation circuit was implemented as off-chip components. Figure 4 shows a micrograph of our prototype chip. The chip area is 0.06 mm². The supply voltage was set to 3 V. The reference resistor $R_{\text{REF}}$ consisting of an off-chip metal-film resistor with a low temperature coefficient was swept in a range from 1 MΩ to 100 MΩ. The results of the measurement are shown in the following.

Figure 5 shows the oscillation frequency as a function of the reference resistor. The output frequency was able to be adjusted by the reference resistor, and we found oscillation in the 20 kHz - 2 MHz frequency range at room temperature. Figures 6, 7 and 8 show an example with the resistor of 10 MΩ. Figure 6 shows measured output frequency as a function of temperature at a 3-V supply voltage. The average of the output frequency was 205 kHz. The temperature variation was 3.5 kHz in a temperature range from −20 to 80°C. The temperature coefficient was 170 ppm/°C. Figure 7 shows the oscillation frequency as a function of supply voltage. The circuit operated correctly with a supply voltage higher than 1.5 V. The variation in the frequency was 3.4 kHz, and the line regulation was 1%/V for a 1.5 - 3 V supply voltage. Therefore, a constant reference clock with little dependence on temperature and supply voltage could be obtained.

To examine the process variations of our devices, we measured 20 samples, each on a different chips from same wafer. Figure 8 shows the distribution of oscillation frequency $f_{\text{REF}}$ at room temperature. The coefficient of variation ($\sigma/\mu$; $\mu$ is the mean value and $\sigma$ is the standard deviation of the distribution) was 5%. The process variations of oscillation frequency $f_{\text{REF}}$ are mainly determined by the variations of the capacitor $C_S$ in switched capacitor resistor. Therefore, adjusting the resistor value, the output frequency can be calibrated.
Figure 7 shows an example of the output waveforms $f_{REF}$ and $f_{INT}$. In this measurement, the intermittent pulse generation circuit consists of a 6-bit digital counter, so the duty ratio of $f_{INT}$ was 64:1. Therefore, adjusting the number of digital counter, a intermittent pulse with large duty ratio can be obtained.

Table I summarizes the performance of our clock generator in comparison with other CMOS clock reference generator [12]-[14]. The power dissipation of the circuit with a 1.5-V power supply was 3 $\mu$W at a 200 kHz and varied from 0.5 to 30 $\mu$W at frequencies from 20 kHz to 2 MHz. Our circuit is superior to others in power consumption.

4. Conclusions

A CMOS clock reference circuit was developed. A prototype chip with a 0.35-µm CMOS process was fabricated and its operation was demonstrated in this paper. The temperature coefficient and line sensitivity were 170 ppm/C and 1%, respectively. The power dissipation was extremely low, about 0.5 to 30 $\mu$W. Our circuit would be useful for intermittent operation of power-aware LSIs that are required to operate with ultra-low-power dissipation.

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References


### Table 1. Comparison of reported CMOS clock reference circuits

<table>
<thead>
<tr>
<th>Process</th>
<th>This work</th>
<th>[13]</th>
<th>[14]</th>
<th>[12]</th>
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<tbody>
<tr>
<td>Temperature range</td>
<td>-20 - 80°C</td>
<td>-35 - 85°C</td>
<td>0 - 120°C</td>
<td>-40 - 125°C</td>
</tr>
<tr>
<td>$V_{DD}$</td>
<td>1.5 - 3 V</td>
<td>1.8 - 2.5 V</td>
<td>1.2 V</td>
<td>2.4 - 2.75 V</td>
</tr>
<tr>
<td>$f_{REF}$</td>
<td>20 kHz - 2 MHz</td>
<td>2 MHz</td>
<td>6 MHz</td>
<td>7 MHz</td>
</tr>
<tr>
<td>Power</td>
<td>0.5 - 30 µW ($V_{DD}$=1.5 V)</td>
<td>3 µW ($V_{DD}$=1.8)</td>
<td>66 µW ($V_{DD}$=1.2)</td>
<td>1.5 mW</td>
</tr>
<tr>
<td>Temperature Coefficient</td>
<td>170 ppm/°C</td>
<td>165 ppm/°C</td>
<td>86 ppm/°C</td>
<td>95 ppm/°C</td>
</tr>
<tr>
<td>Line regulation</td>
<td>1%/V</td>
<td>1.3%/V</td>
<td>N.A.</td>
<td>1.8%/V</td>
</tr>
<tr>
<td>Process sensitivity ($\sigma/\mu$)</td>
<td>5% (w/o calibration)</td>
<td>N.A.</td>
<td>0.8% (w/o calibration)</td>
<td>0.13% (w/ calibration)</td>
</tr>
<tr>
<td>Chip area</td>
<td>0.06 mm²</td>
<td>0.015 mm²</td>
<td>0.03 mm²</td>
<td>1.6 mm²</td>
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