Single-Electron Circuit for Inhibitory Spiking Neural Network with Fault-Tolerant Architecture

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***Abstract*—An inhibitory spiking neural network that uses single-electron circuit devices is described. The network consists of a number of identical neuron circuits constructed from single-electron oscillators with coupling capacitors. The neurons are cross-connected in a competing fault-tolerant architecture. Computer simulations show that the proposed circuit is capable to overcome a high rate of random device failures.**

I. INTRODUCTION

The development of systems that imitate the behavior of living neural networks opens a promising area of research in nanoelectronics. To proceed toward this goal, we propose a spiking artificial neural network that combines the advantages of single-electron circuits with a multi-layer fault-tolerant architecture.

The single-electron device is a nanodevice which behavior is based on quantum effects such as electron tunneling and Coulomb blockade. Temperature of operation, electrical noise as well as random device failure are key issues that influence the reliability in the development of nanodevices. The successful development of novel systems based on nanoelectronic circuits requires addressing the reliability issues related to systematic errors due to fabrication as well as transient errors which occur in a random way due to background charge effects, for example. A competitive neural network that exhibits winners-share-all (WSA) behavior is a possible candidate to solve these problems, taking advantage of a high resistance to noise. The WSA competition selects multiple winners in the order of magnitudes of external input, which can be used to reduce the influence of the noise when multiple winners select the external signal [1]. Recently, fault-tolerant circuit architectures have been proposed as a new system design approach for nanodevices [2]. In this paper, we show an adapted version of the fault-tolerant architecture proposed earlier which can accommodate single-electron spiking neurons, to be used in a competitive artificial neural network. The fault-tolerant architecture is described in Section II. Section III describes a method adapted for constructing an artificial spiking neuron that uses single-electron circuits with the fault-tolerant architecture. A number of identical single-electron spiking-neuron circuits consisting of five single-electron nonlinear oscillators with coupling capacitors have been used to construct a fault-tolerant neuron circuit. The single-electron oscillator produces nonlinear oscillation caused by the Coulomb blockade phenomenon (Sections III-A and -B). A novel single-electron spiking-neuron circuit (Section III-C) is constructed by merging the fault-tolerant architecture and the spiking-neuron circuit. The fault-absorbtion properties of the fault-tolerant neuron circuit are confirmed by computer simulations, guaranteeing that the proposed neuron circuits overcome random device failures (Section III-D). An artificial competitive neural network with fault-tolerant neurons is proposed in Section IV, and the simulation results of this network are shown Section V. Concluding remarks are given in Section VI.

II. FAULT-TOLERANT CIRCUIT ARCHITECTURE

The proposed fault-tolerant architecture consists of four layers in which data is strictly processed in a feed-forward manner (Fig. 1). The first layer is denoted as the input layer. The core operation is performed in the second layer, which consists of a number of identical, redundant units implementing the desired Boolean logic function. It will be seen that the fault immunity increases with the number of redundant units, yet the operation is quite different from the classical majority-based redundancy. The third layer receives the outputs of the redundant logic units in the second layer,

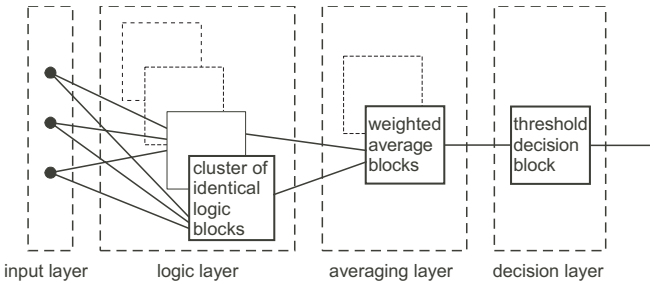

Figure 1. Fault-tolerant architecture based on multiple layers [2].

creating a weighted averaging with rescaling. In this work, the value of the weights has been chosen to be equal to one for all connections. Finally, the fourth layer is the decision layer where a binary output value is extracted using a simple threshold function. By using this architecture, the circuit can operate correctly under high error density in logic elements [2].

III. CIRCUIT STRUCTURE

A. Nonlinear oscillator with single-electron circuit

A single-electron nonlinear oscillator has been used to construct an artificial spiking neuron. The nonlinear oscillator consists of a tunneling-junction (C_j) and resistance (R_i) of large value connected in series to a common node, and biased by voltage source (V_{dd}) as shown in Fig. 2 (a). The oscillator produces a nonlinear voltage oscillation that is caused by electron tunnelings at low temperatures at which the Coulomb-blockade effect occurs, as shown in Fig. 2 (b) [4]. The node voltage of the oscillator is dependent on the value of V_{dd}, and is stable in absence of input signal, under the condition of correct threshold magnitude for electron tunneling across C_j, to be selected above the node voltage, for a positive value of V_{dd}. When an external input is applied to the oscillator, the node voltage sweeps over the threshold, thus causing an electron tunneling to occur, and the node voltage to change from a positive to a negative value. The node voltage restores to a stable state by charging from V_{dd} afterwards. This electron tunneling phenomenon is defined and used as a spike in this work. A chain of oscillators is required in order to allow the propagation of spikes. Fig. 3 (a) shows a unit circuit where two oscillators are connected with a coupling capacitor (C). In this unit circuit, the oscillators with bias V_{dd} put in reverse polarity alternately in order to permit transmission of the spikes. When an external input is applied to the oscillator A, the node voltage of the oscillator A is changed suddenly. This sudden change of node voltage induces an electron to tunnel through on the oscillator B. Applying the same principle to a chain of successive oscillators, each of which has inverted bias polarity with respect to its next neighbors, allows an electron tunneling phenomena to be propagated. Consequently, the spike is transmitted through the circuit.

B. Spiking-neuron circuit with single-electron oscillators

Fig. 4 illustrates a spiking-neuron circuit that uses five single-electron nonlinear oscillators with coupling capacitors. Input spikes lead to electron tunneling at the oscillator 1, which results in subsequent electron tunneling at oscillators 2, 3, and 4. The oscillator 5 is biased with a positive voltage V_L which is set lower than V_{dd}. In doing so, multiple oscillator input signals are required to activate oscillator 5, e.g., 3 oscillators in Fig. 4. Simultaneous electron tunneling at 3 junctions, oscillators 2, 3, and 4 in our example, leads to an electron tunneling at oscillator 5. In this arrangement of the oscillators, spikes are transmitted from the input terminal to the output terminal. Unwanted spikes that may be randomly generated at the output terminal do not cause electron

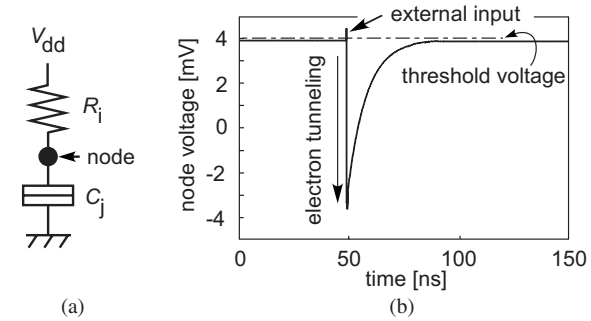

Figure 2. Single-electron nonlinear oscillator. (a) circuit configuration and (b) operation of the oscillator (simulated).

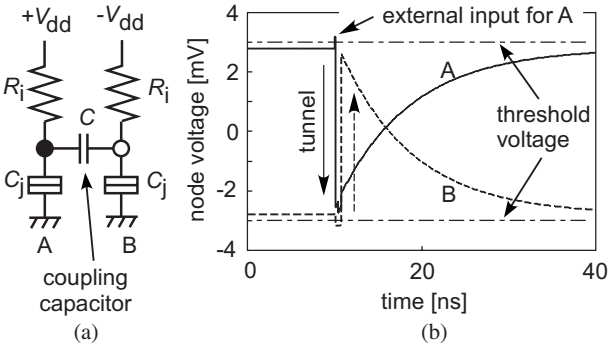

Figure 3. Unit circuit for single-electron neuron circuit. (a) circuit configuration and (b) operation of the circuit (simulated).

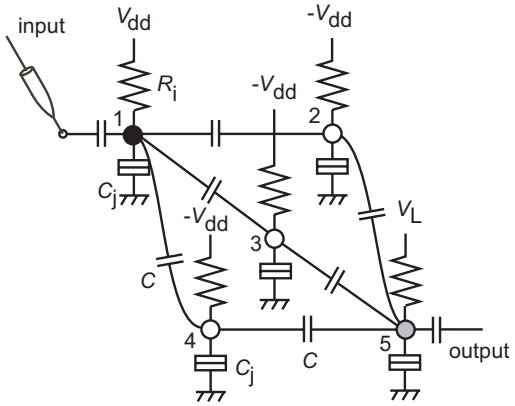

Figure 4. Single-electron spiking-neuron circuit.

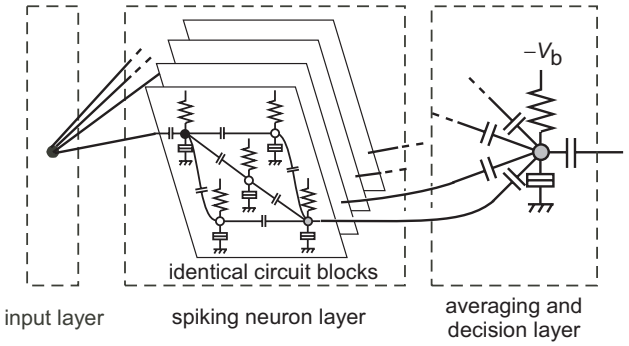

Figure 5. Single robust neuron based on the fault-tolerant architecture. In the second layer, the single-electron spiking-neuron circuits are used instead of logic circuits.

tunneling at the oscillator 5. Consequently, this neuron circuit can mimic the generation of an action potential in a living neuron, and guarantee correct direction of the data flow [3].

C. Single robust neuron

The novel single-electron spiking-neuron circuit operating with the fault-tolerant architecture is shown in Fig. 5. This circuit, named "single robust neuron," consists of three layers according to the fault-tolerant architecture. The first layer is denoted as input layer. In this neuron circuit, the input signal is a periodic spiking signal. The second layer is the spiking neuron layer consisting of identical redundant single-electron spiking-neuron circuits. The third layer is the averaging and decision layer where the single-electron oscillator is operating. The oscillator is biased with $-V_b$, and propagates an output spike when it receives input spikes from the second layer oscillators. The actual threshold value which dictates the firing of a spike is dependent on the oscillator bias voltage $-V_b$, which relates to the number of required simultaneous input spikes.

D. Simulation results

Extensive computer simulations were carried out in order to validate the proposed models. (In simulation, we used a modified Monte Carlo method. Also see Appendix in [5].) Reliability results are shown in Fig. 6, where R is the redundancy factor representing the number of identical spiking neuron circuits in the spiking-neuron layer of a single robust neuron. The probability of correct operation is defined as the proportion of correct output spikes over the total number of input spikes. Random circuit failures were applied to the neuron second layer elements causing local disruption of correct behavior. The probability of correct operation, or success rate was observed for a sweep of various probabilities of error occurrences. Also the impact of increased redundancy was considered.

Clearly, the original spiking-neuron circuit which had been initially built with no consideration for fault-tolerance (Fig. 6, solid line) shows a large failure rate with increasing error densities. On the other hand, a redundancy factor of seven to nine allows absorbing a significant error density of up to 0.3 with unaffected circuit behavior.

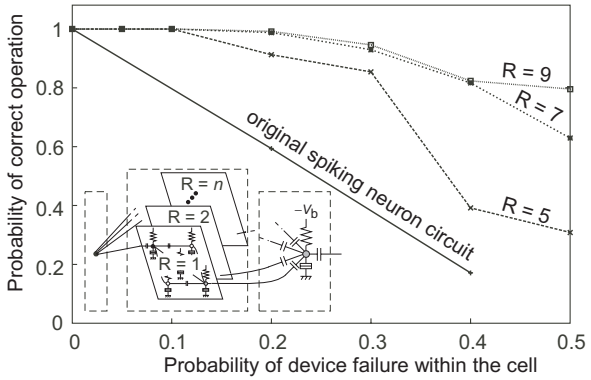

Figure 6. Simulation results that show the probability of correct operation as a function of the probability of device failure in single robust neurons (with redundancy factor R = 5, 7, and 9) and original spiking-neuron circuit (with no fault immunity).

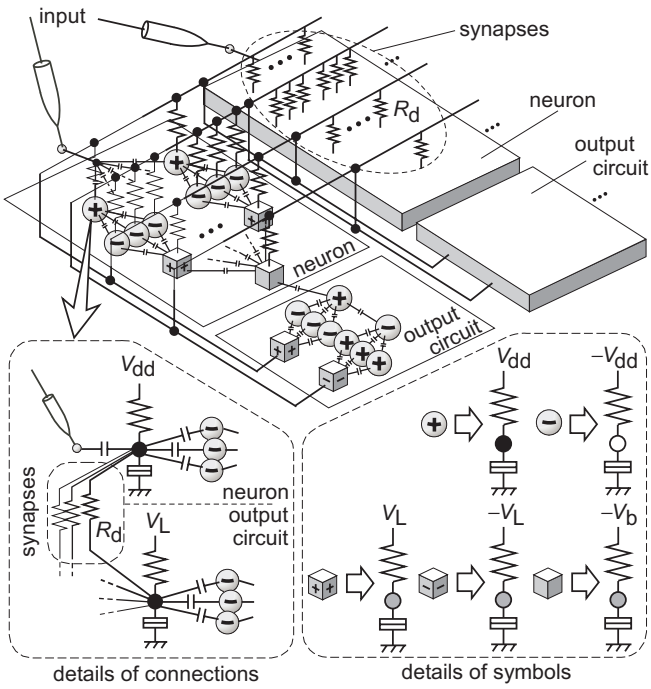

Figure 7. Competitive neural network with single robust neuron. The neuron is connected with the output circuit and the input terminal. The oscillators that are biased by $\pm V_L$ respectivery in output circuit is connected with every oscillator in the neuron by R_d.

IV. Competitive Network System

The proposed single robust neuron has been used in the development of a competitive spiking neural network as depicted in Fig. 7. In this network, the single robust neuron is connected with output driver circuits and an input terminal. The driver circuits connect with all single-electron oscillators which are located in the neurons through a coupling resistance (R_d). R_d performs the role of an inhibitory synapse. When the spike travels through a neuron, propagating from its input to output terminals, a difference of electric potential is generated between both terminals of R_d. Consequently, a current flows through R_d until the voltage difference vanishes. As long as current flows, the magnitude of the node voltage of the oscillator in the neuron decreases, preventing any electron to tunnel through the oscillator. This behavior is similar to inhibitory phenomenon in living neurons.

V. Competitive Network Simulation Results

A competitive neural network of 100 cross-connected neurons was simulated. Excitatory input spike frequencies are provided in linearly decreased ranking of the neurons. Fig. 8 shows the result of sample simulations where the number of spikes is represented as a function of the neuron number (rank), under the condition of a redundancy factor

of R = 5 in each single robust neuron, and considering two levels of error densities (error rates = 0 and 0.1). The observed nodes are the central node of the oscillators referred to as the averaging and decision layer oscillator in Fig. 5, and which is biased with $-V_b$. The network circuit operates as the WSA competition network, where a "cluster" of winner neurons is extracted out of the total set of neurons. Introducing random errors into the circuit does not affect the WSA competition operation, as depicted for an error rate of 0.1.

Network simulations have been applied using different error rates, and a redundancy factor of 5, which was selected as an appropriate value which optimally balances the reliability improvement with the hardware overhead. The similarity rate of a neural network behavior under the imposed errors vs. under no error is shown in Fig. 9 as a function of the applied error density in the artificial neural network. The similarity rate shows a significant contrast for both cases where no fault-tolerant architecture was applied, and where a fault-tolerant architecture was used with a redundancy factor of 5. The similarity rate is processed from the simulation result data, delivered as shown in Fig. 8. A function approximation in the form of: $f(n) = an + b$ is extracted, where n is the neuron number (rank), a and b are fixed numbers. The similarity rate is defined as the value of the slope (constant a) of the target function f_i(n) considering error rate i, over the value of slope of the standard function f_0(n) considering no induced error.

The original spiking neural network does not operate under an error density of more than 0.05. A modest value of the redundancy factor R allows absorbing a higher level of error density, as shown on Fig. 9 for R = 5. However, it must be emphasized that the similarity rate estimates the how similar the functions remain despite of induced errors. The circuit still operates as a WSA under dissimilar functions.

VI. CONCLUSIONS

An artificial neural network constructed from single-electron circuits and using a fault-tolerant architecture has been proposed. The network uses the single robust neuron which overcomes random device failure. The artificial neuron consists of three layers which are the input layer, the spiking neuron layer, and the averaging and decision layer. A number of identical spiking-neuron circuits consisting of five redundant single-electron nonlinear oscillators with coupling capacitors in the spiking neuron layer are part of the proposed competing WSA artificial neural network. Simulation results confirm that the single robust neuron overcomes random device failures. An error rate up to 0.3 can be absorbed with no significant modification of circuit behavior. Also the network circuit has been confirmed to operate correctly as a WSA competition network under random device failure. A large value of the redundancy factor allows absorbing a higher level of error density. Thus, confirmation is provided that circuit-level fault-tolerant architectural design consideration improves the error immunity of single-electron artificial neural networks.

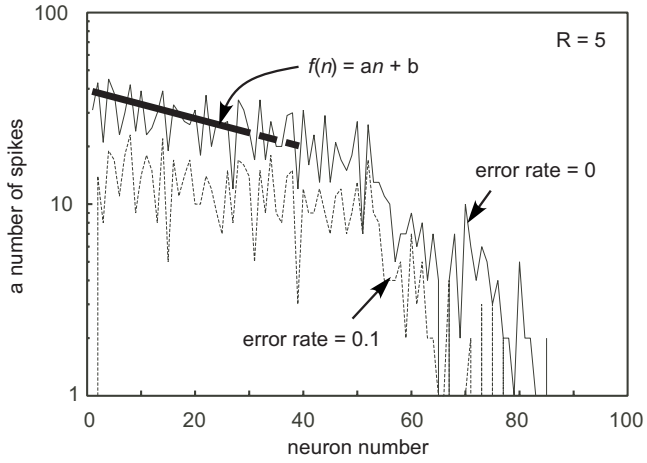

Figure 8. Simulation results that show the number of spikes as a function of the neuron number.

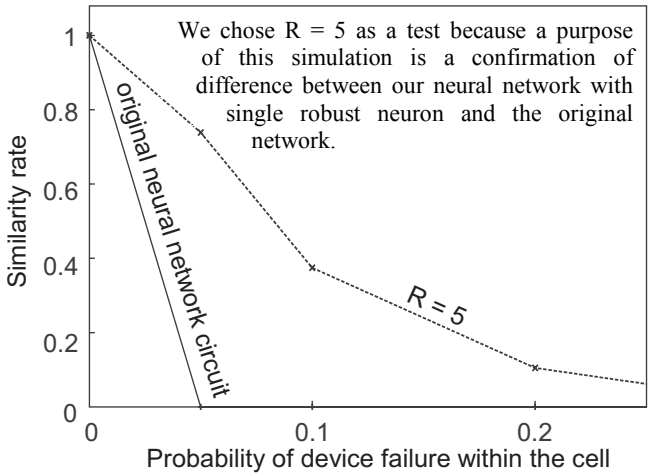

Figure 9. Simulation results that show the probability of correct operation as a function of the probability of device failure in the network circuit with the single robust neuron (R = 5) and original spiking-neuron circuit.

Future work will see experiments of the fault-tolerant architecture including varying weight values. The impact of second-layer units with a suspected error can be limited by prepare adaptation of the connection strength, depending on the probability of erroneous output.

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