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A MOS circuit for bursting neural oscillators with excitable oregonators

Yusuke Kanazawa,[a)] **Tetsuya Asai, Tetsuya Hirose, and Yoshihito Amemiya**

Department of Electrical Engineering, Hokkaido University, Kita 13, Nishi 8, Kita-ku, Sapporo, Hokkaido, 060–8628 Japan

a) *asai@sapiens-ei.eng.hokudai.ac.jp*

Abstract: An analog MOS circuit that imitates bursting properties of spiking neurons is proposed and fabricated. The circuit consists of the Oregonator device that can easily be implemented on analog CMOS LSIs. We demonstrate temporal properties of the proposed circuits by SPICE and fabricated ICs.

Keywords: neuromorphic LSI, bursting neurons, spiking neurons

Classification: Integrated circuits

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1 Introduction

Spiking neural networks have attracted the attention of neuromorphic engineers who have mainly focused on the dynamic implications of neurons. Recently, Senn presented an easy, practical way of extracting coherence information from cortical neurons by projecting bursting spike trains through depressing synapses onto a postsynaptic neuron [1]. Although the silicon spiking neurons and depressing synapses required for implementing such neural network have been developed, bursting neural circuits that are suitable for CMOS VLSI implementation have not yet been fully developed. We here propose a novel bursting neuron circuit based on the Oregonator [2], which represents a model of the Belousov-Zhabotinsky reaction and exhibits quite similar excitable behaviors to spiking neurons to achieve compact and neuromorphic design for bursting neural circuits.

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2 Bursting neuron circuits

We constructed a bursting neural circuit by using a "fast-slow burster" [3] which has two oscillatory components ("FAST" and "SLOW"). FAST operates at higher frequency than SLOW, and the output of SLOW (x_s) is treated as a parameter of FAST. If x_s exceeds certain threshold (θ), FAST becomes oscillatory. While, if x_s does not exceed θ, the FAST becomes stable. The output of FAST (x_f) exhibits bursting properties as long as the value of x_s exceeds θ.

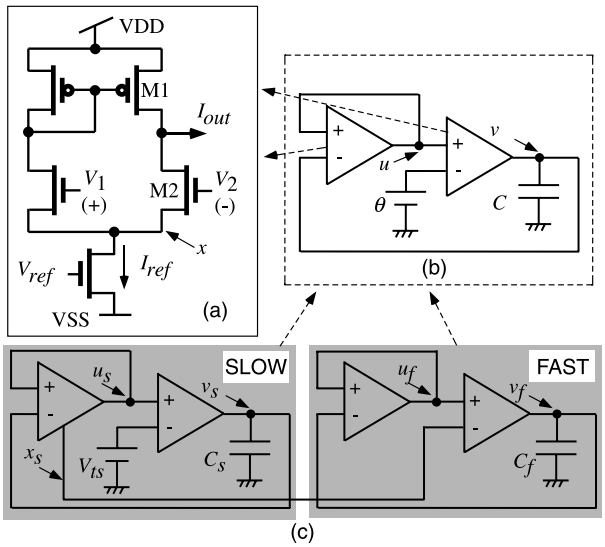

Fig. 1. Circuit configuration for bursting neural circuit; a) OTA, b) Oregonator circuit, and c) bursting neural circuit.

For the fast and slow oscillators, we here employ an oscillatory circuit based on the Oregonator that represents a model of Belousov-Zhabotinsky reaction. Depending on the system parameters, the Oregonator exhibits excitatory or oscillatory behavior [2, 4]. We constructed the Oregonater circuit using operational-transconductance amplifiers (OTAs) [Fig. 1 (a)]. Figure 1 (b) outlines the Oregonater circuit, which consists of one capacitor and two OTAs. When all the transistors are operated in the subthreshold region, the dynamics of this circuit can approximately be represented by

$$u = \begin{cases} \text{VDD} & (u - v \gg 0) \\ \frac{\kappa V_0}{2V_T}\,(u - v) & (u - v \approx 0) \\ \text{VSS} & (u - v \ll 0) \end{cases} \quad \text{and} \tag{1}$$

$$C\frac{dv}{dt} = I_{\text{ref}} \tanh \frac{\kappa(u-\theta)}{2V_T}, \tag{2}$$

where V_0 represents the early voltage of output transistors (M1 and M2), κ represents the effectiveness of the gate potential, and $V_T \equiv kT/q = 26$ mV at room temperature (k is Boltzmann's constant, T the temperature, and q the charge of an electron). If C is constant, I_{ref} is treated as the rate constant

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of (2). The operation speed of this circuit increases as I_{ref} increases and the value of u and v are restricted within the range of [VDD:VSS]. Thus, when θ = VDD (or VSS), the value of $(u-\theta)$ always becomes positive (or negative); i.e., dv/dt becomes positive (or negative) and never change from positive to negative (negative to positive). Therefore, the value of v becomes VDD or VSS as time passes, and the circuit becomes stable. When VSS $\ll \theta \ll$ VDD, the value of dv/dt can change from positive to negative (negative to positive) depending on $(u-\theta)$. Thus, the circuit becomes oscillatory.

Figure 1 (c) has the configuration for the bursting neural circuit. The value of x in SLOW (x_s) is treated as a parameter of FAST. The value of V_{ref} in FAST (V_{rf}) must be larger than the value of V_{ref} in SLOW (V_{rs}).

3 Results

The Oregonator circuit [Fig. 1 (b)] was simulated with SPICE using the model parameters for the 1.5 μm CMOS process. The supply voltages were set at VDD = 5 V and VSS = 0 V. The parameters (external inputs) were set at θ = 3.5 V, and V_{ref} = 0.4 V in Figs. 2 (a) and (b) or 0.9 V in Fig. 2 (c). We used the gate capacitance of an nMOS (W= 36 μm, L = 36 μm) transistor instead of capacitor C. Figure 2 (a) shows the value of u when V_{ref} = 0.4 V. Figure 2 (b) shows the value of x when V_{ref} = 0.4 V and figure 2 (c) shows the value of u when V_{ref} = 0.9 V. When V_{ref} = 0.4 V, the interspike interval (ISI) was about 13 ms. When V_{ref} = 0.9 V, the ISI was about 0.7 ms. The operation speed of this circuit changed depending on V_{ref}.

We then simulated the bursting neural circuit [Fig. 1 (c)]. The supply voltages were set at VDD = 5 V and VSS = 0 V. The parameters were set at V_{ts} = 3.5 V, V_{rf} = 0.9 V, and V_{rs} = 0.4 V. The value of u_f through two inverters (driver) is in Fig. 2 (d). The interburst interval (IBI) was about 13 ms, which is as same value as the ISI which obtained from Fig. 2 (a). The ISI during the burst was about 0.7 ms, which was the same value as the ISI obtained from Fig. 2 (c).

We fabricated a bursting neural circuit using a 1.5-μm CMOS process. Figure 2 (e) shows the measurement results for the bursting neural circuit. The supply voltages were set at VDD = 5 V and VSS = 0 V. The parameters were set at V_{ts} = 3.5 V, V_{rf} = 0.9 V, and V_{rs} = 0.2 V. The IBI was about 3.2 s and the ISI during the burst was about 60 ms. This circuit exhibited bursting properties and Fig. 3 shows a micrograph of it. Total size of the circuit was 90 $\times$ 90 μm^2 and it consisted of 22 MOS transistors.

4 Conclusion

We proposed a bursting neural circuit and demonstrated its temporal properties. The results showed that our circuit exhibited desired bursting properties although the circuit consisted of quite few number of MOS transistors, which implies that the circuit is suitable for implementing bursting neurons on VLSI and allows us to construct a large scale bursting neural networks.

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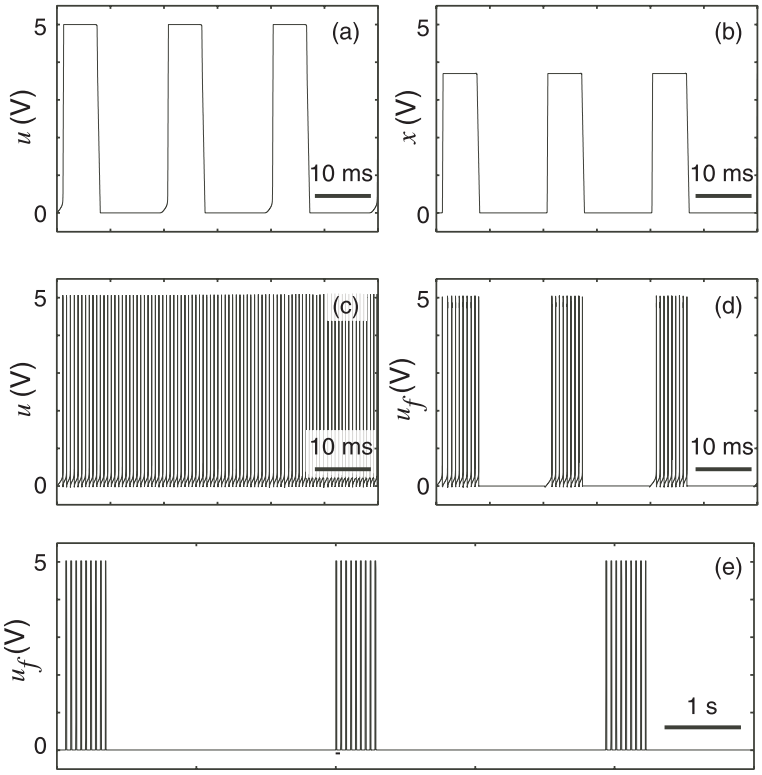

Fig. 2. Temporal properties of proposed circuits; a) value of u in the Oregonator circuit ($V_{ref} = 0.4$), b) value of x in the Oregonator circuit ($V_{ref} = 0.4$), c) value of u in the Oregonator circuit ($V_{ref} = 0.9$), d) simulation results for bursting neural circuit, and e) measurement results for bursting neural circuit.

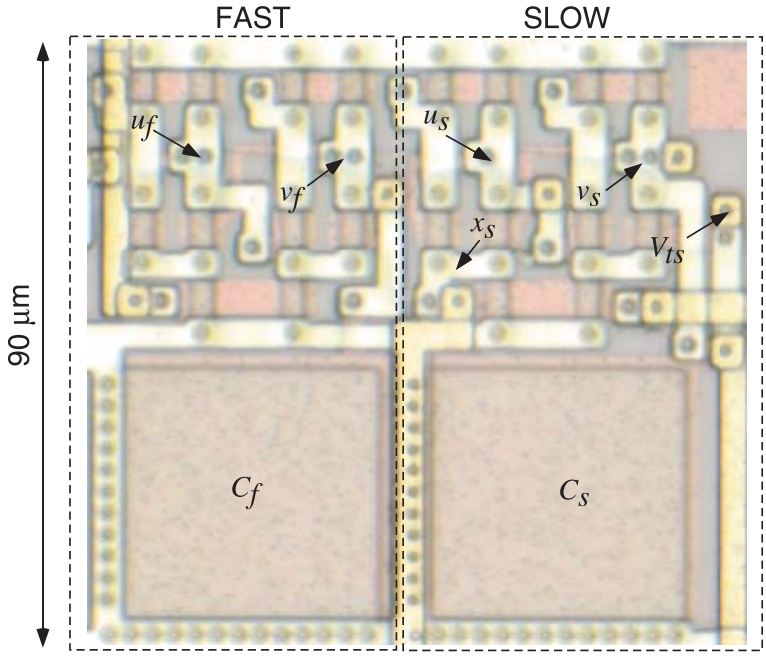

Fig. 3. Micrograph of bursting neural circuit.

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