A Novel Retina Chip with Simple Wiring for Edge Extraction

Hitoshi Ikeda, Kiyotaka Tsuji, Tetsuya Asai, Hiroo Yonezu, and Jang-Kyoo Shin

***Abstract*—A novel silicon retina chip based on the information processing in the vertebrate retina was designed and fabricated. The chip has a novel wiring structure in which all pixels are connected through the channel of MOS transistors, which simplifies a wiring structure compared with conventional resistive networks. The proposed structure minimizes the pixel area and certainly increases a fill factor since each pixel consists of only two photodiodes and three MOS transistors. Experimental results showed that the chip could extracted the edge of input images successfully. Furthermore, it was shown that the chip could operate over a wide range of light intensities by adjusting its spatial resolution.**

***Index Terms*— Image edge analysis, integrated circuit design, resistive circuits, visual system.**

I. Introduction

THE VERTEBRATE retina is a neuronal image-processing system that makes a preprocessor of the brain. Most processings done here, such as photoinput sensing, motion detection and so on, are performed by spikeless and analog neuronal interactions. Among those retinal functions, the edge extraction of input images is the most important feature since it is believed to be necessary for the aggregation processes of the neuronal information in the brain. In the vertebrate retina, three types of cells are important processing elements for performing the edge extraction, that are photoreceptors, horizontal and bipolar cells, respectively. The bipolar cells receive the information formed by the interactions of the photoreceptors and the network of interconnected horizontal cells [1]–[3].

In order to realize a superior image-processing system artificially, a number of retinomorphic hardwares using an analog VLSI technology has been proposed in the literature [4]–[7], which may promise the realization of a high-performance real-time image processing system. Recently, several silicon retina chips have been proposed for implementing the retinal edge extraction system. In those chips, a spatial smoothing task of the input images, which is performed by the horizontal cells, has been realized by a resistive network [4]. The network is composed of resistive circuits which are formed by passive resistors using several MOS transistors [4]–[6] or resistors of a diffusion layer [7]. However, it is very hard to connect a pixel with a variable conductance since those resistive networks require a complicated wiring structure and occupy a large chip area. Our proposed silicon retina chip simplifies the wiring between pixels with a variable conductance, which enables the chip to operate over a wide range of light intensity by adjusting its resolution to maintain the sensitivity to the light [8].

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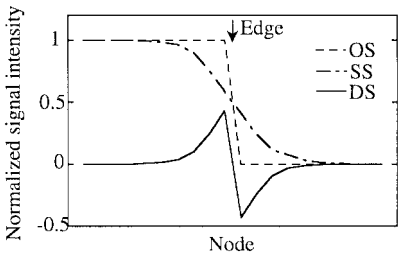

Fig. 1. Edge extraction mechanism in the retina. The edge is extracted as a zero-crossing differential signal (DS) which is obtained from subtracting the smoothed signal (SS) from the optical signal (OS).

II. Chip Architecture and Operational Principles

The fundamental edge extraction mechanism in the retina is shown in Fig. 1. The horizontal and vertical axes represent the one-dimensional (1-D) space of the retinal sheet, where we discretely express the position of nodes, and normalized signal intensities of the retinal cells, respectively. The photoreceptor perceives the light (optical signal) and transforms it into an electrical signal which reflects the intensity of the light. The edge is represented at the node where the optical signal changes remarkably. The transformed optical signal (OS) is spatially smoothed by the horizontal cell, while the bipolar cell yields the differential signal (DS), which is the difference between OS and the smoothed signal (SS). Thus, the absolute value of the output signal of the bipolar cell becomes large near the edge, while the signal becomes weak as the node leaves from the position of the edge. In this way, the edge of the input image is extracted.

According to the extraction mechanism mentioned above, we proposed and fabricated a prototype chip that contains photoelectronic conversion, the smoothing and differential calculation elements, as shown in Fig. 2. Fig. 2(a) shows the top view of the chip. Each pixel is located with hexagonal layout. Fig. 2(b) shows the cross-sectional view of the chip cut along the dotted line in Fig. 2(a). The layout and equivalent circuit of the pixel are shown in Fig. 2(c) and (d).

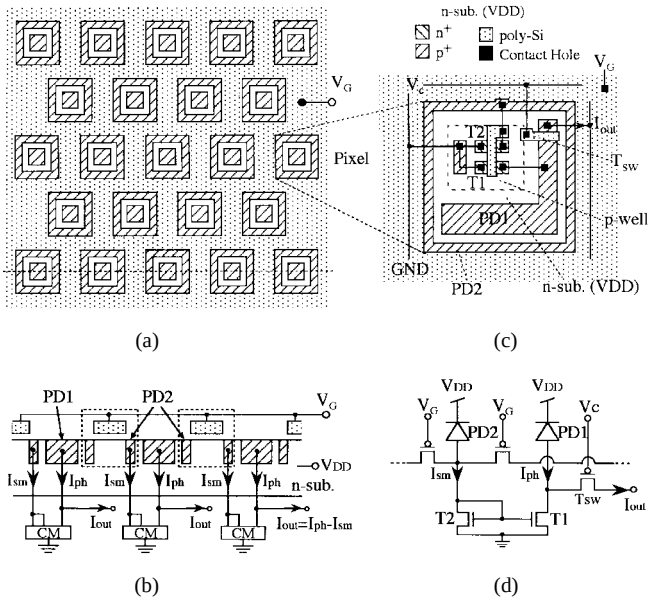

Fig. 2. Structure of the proposed retina chip. (a) Top view. (b) Cross-sectional view. (c) Layout of the pixel. (d) Equivalent circuit of the pixel. Each pixel consists of two photodiodes and three MOS transistors. The area between pixels is covered with poly-Si which acts as a gate of pMOS transistor.

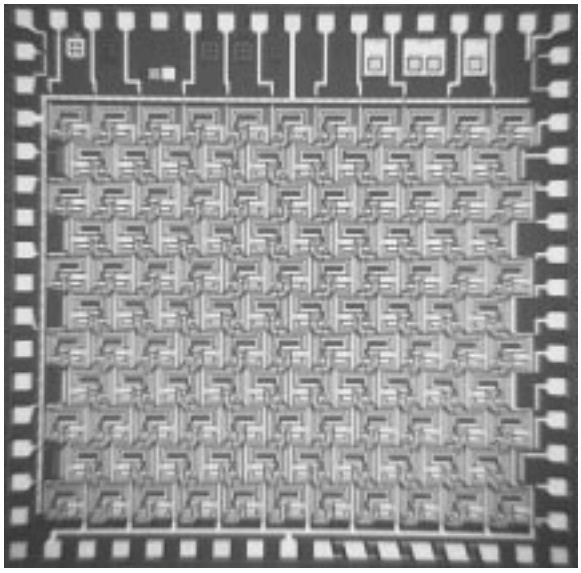

Fig. 3. Photomicrograph of the fabricated chip. The chip contains 116 pixels in a 5.1-mm × 5.1-mm chip area.

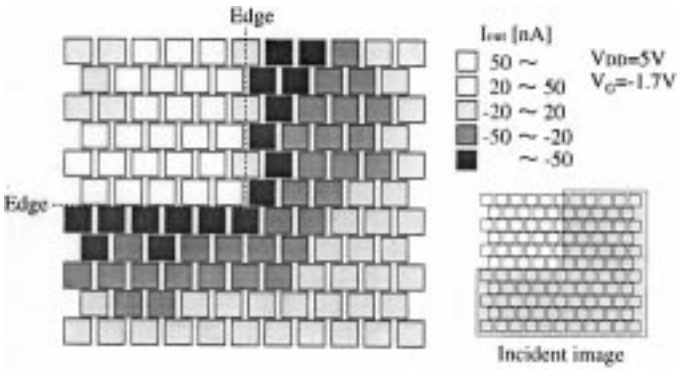

Fig. 4. Measured distribution of output currents $I_{\rm out}$ when the light was incident upon an upper left quarter of the chip. Large output currents with different signs were obtained only near the edge. Thus, the edge was extracted.

Each pixel corresponds to the photoreceptor and the bipolar cell, while the horizontal cell is realized by a MOS structure between the pixels. One pixel consists of two photodiodes (PD1 and PD2) and one current mirror circuit (CM). PD1 and PD2 generate the same photocurrents $I_{\rm ph}$ when the light is incident upon the pixel. The area between two PD2s surrounded by dotted lines in Fig. 2(b) forms a pMOS transistor whose source and drain regions are common to the p region of PD2. Thus, a spatially smoothed photocurrent $I_{\rm sm}$ can be obtained when $I_{\rm ph}$ generated in PD2 is diffused. The extent of the diffusion can be controlled by a voltage V_G which is given to the common poly-Si gate. On the other hand, PD1 outputs $I_{\rm ph}$ independently of $V_{\rm G}$ since PD1 is isolated from PD2. Then, the output current $I_{\rm out}$ is the differential current between $I_{\rm ph}$ and $I_{\rm sm}$ because $I_{\rm sm}$ is mirrored to the output node by CM consisting of two nMOS transistors ($T1$ and $T2$).

Each pixel includes a transistor $T_{\rm sw}$ which acts as a switch for detecting the output current selectively. The output current $I_{\rm out}$ of each pixel flows out of the pixel when a control voltage V_c is given to $T_{\rm sw}$. The drain of $T_{\rm sw}$ is common to the p region of PD1, which also makes the pixel area small.

III. Experimental Results and Discussion

The proposed retina chip shown in Fig. 2 was fabricated with 10-μm CMOS process in Toyohashi University of Technology. The chip photograph is shown in Fig. 3, where 116 pixels were implemented in a 5.1-mm × 5.1-mm chip area.

Fig. 4 shows the measured distribution of $I_{\rm out}$ when the light was incident upon a upper left quarter of the chip. A white fluorescent light was used for the light source with a power density of 680 μW/cm^2. The edge was located at a dotted line in the figure. It was shown that the pixels adjacent to the edge yielded salient output currents. Namely, large positive currents were obtained in the region where the light was applied, while large negative currents were obtained in the opposite region where no light was applied. The output currents of the pixels far from the edge were nearly zero. These results explicitly show that the edge is successfully detected as the large output currents with different signs.

Fig. 5 shows the measured distribution of $|I_{\rm out}|$ between nodes 6 and 9 in logarithmic scale when the light was incident upon an upper half of the chip. The nodes were numbered along a row vertical to the edge, as shown in the figure. When V_G was low, all $I_{\rm out}$ were large as a whole because of the increased channel conductance of the pMOS transistors. $I_{\rm ph}$ generated by PD2 extends to farther nodes and then the slope of SS shown in Fig. 1 becomes gentle. Thus, the number of nodes which yield large absolute output currents is increased around the edge. When V_G is increased, the channel conductance decreases and then the slope of SS becomes steep. Therefore, only the pixels which are close to the edge output the large absolute currents.

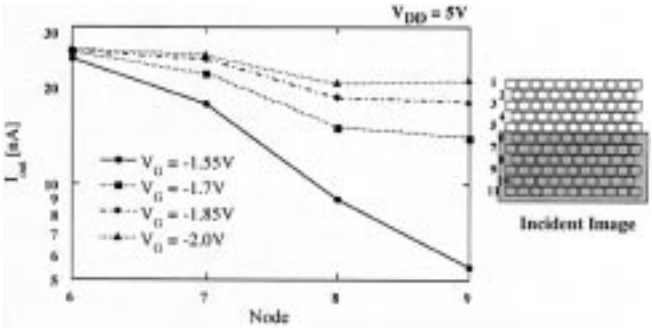

Fig. 5. Measured distribution of output currents $|I_{\rm out}|$ between nodes 6 and 9 in logarithmic scale when the light was incident upon an upper half of the chip. The nodes were numbered along a row vertical to the edge, as shown in the inserted drawing. Absolute gradients between nodes are large (small) as a whole when V_G is large (small).

These results indicate that a spatial resolving power is low when V_G is low, while the resolving power is certainly improved by increasing V_G. Thus, the spatial resolution can be controlled by adjusting V_G depending on the input light intensity. When the input light intensity is high, the spatial resolving power can be raised by increasing V_G because $I_{\rm out}$ is sufficiently large near the edge. When the input intensity is low, a certain level of $I_{\rm out}$ can be obtained by reducing V_G at the expense of the spatial resolving power. In this way, the proposed chip could adapt to a wide range of light intensity as in the vertebrate retina.

The chip was contrived structurally to minimize the pixel area and to increase the fill factor, as explained in Fig. 2. When a 0.5-μm double-poly-Si and double-metal CMOS process is applied, it is estimated that the pixel occupies an area of 12 μm $\times$ 14 μm and a fill factor is 31.4%. Then 6×10^5 pixels could be integrated in a chip with an area of 1 cm $\times$ 1 cm.

IV. Conclusion

A novel silicon retina chip without conventional wiring between pixels was designed and fabricated for performing the edge extraction tasks. The proposed chip has several merits in the integration process. First, all pixels are connected by the channel of MOS transistors, which omits a complicated wiring structure between pixels. Secondly, each pixel consists of only two photodiodes and three MOS transistors. Thirdly, the source and drain of those transistors are common to the p region of photodiodes, which makes the pixel area small. This structure certainly increases the fill factor as well. Experimental results showed that the proposed chip performed successfully the edge extraction over a wide range of light intensity by adjusting its spatial resolution.

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