A MOS Circuit for a Nonmonotonic Neural Network with Excellent Retrieval Capabilities

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Abstract—**A MOS (metal-oxide semiconductor) circuit is proposed for implementing a nonmonotonic transfer characteristic of a neural network. The present research is motivated by the recent results of theoretical studies showing excellent equilibrium properties of networks with the nonmonotonic neural units. These properties include enhancement of storage capacity and complete elimination of noise in associative memory recall. The simple form of the transfer characteristic enables one to implement it with a simple electric circuit of standard MOS transistors. SPICE simulation results are shown for the behavior of the neural units in associative memory recall.**

I. Introduction

ANALOG neural networks with symmetric connections and monotonically increasing transfer functions, which are usually assumed to be sigmoid functions, are of particular importance since these neural networks possess the Lyapunov functions [1]. Existence of the Lyapunov functions implies that the dynamics of neural networks is downhill motion toward minima (the retrieval states) of these functions and thereby ensures successful retrieval of memory contents.

Some aspects of neural networks with sigmoid transfer functions, however, are not attractive for applications aiming at associative memory. These aspects are i) small values of the storage capacity (an upper bound for the ratio of number of memory patterns to the size of neural network): statistical mechanical calculations revealed that the storage capacity of monotonic neural networks with random memory patterns embedded by the local Hebbian learning rule is ≈ 0.14 [2], [3], which are as small as that of the stochastic formal-neuron network [4] or ii) fully connected connections: all the neural units need to be mutually connected for attaining full retrieval ability by means of the network dynamics based on the meanfield-type interaction among the units. Recently it was shown, by using the self-consistent signal-to-noise analysis (SCSNA) in the limit N (= the number of neurons) $\rightarrow \infty$, that neural networks with nonmonotonic transfer functions in general have enhanced storage capacity, $\alpha_c \simeq 0.4$ [5]–[7] for the synaptic connections learned by the local Hebbian rule. This value is much larger than those for the sigmoid transfer functions. In particular, it was revealed that such neural networks have a newly-found phase of equilibrium states in which the noise in the local fields (we call the inputs to neurons the local fields) disappears in $N \rightarrow \infty$ [5], [6] even for an extensive number of stored patterns. This implies that the neural networks can perform errorless retrieval of stored patterns in the vanishing-noise phase which we call the super retrieval phase. It was also suggested that nonmonotonic neural networks have rather suppressed distributions of spurious states that are obstacles for memory retrieval [8]. These attractive features are confirmed by numerical simulations for the networks even with relatively small N, i.e., from a few to several hundred.

Having a small number of neural units is particularly desirable for practical realization of associative memory on neural chips. This is because enough room is not available for making the necessary connections among the neural units in large-scale networks. Eliminating the synaptic connections, however, implies loss of information on memory patterns carried by those connections and inevitably leads to the reduction of the storage capacity. Wiring dense connections therefore is an essential problem for implementing large-scale neural networks designed for associative memory machines. The network sizes should be restricted to small ones which are realizable with the present device-manufacturing technology.

In the present paper, we propose a possible MOS (metal-oxide semiconductor) circuit for the associative-memory neural network with nonmonotonic transfer function studied in [6]. The existence of the super retrieval phase for wide ranges of parameters makes the present transfer function particularly attractive among others [7] for practical purposes. Furthermore, the simple signal-transfer characteristic of the nonmonotonic transfer function enables one to implement the neural unit by a rather simple circuit. We show by SPICE simulations that the neural network with a small number of the units can still exhibit retrieval of memory patterns essentially in the same manner as was described by the SCSNA for the system with an infinite number of neurons. Further, we use a network of the nonmonotonic units in a more realistic application of character recognition to confirm that the proposed neural unit extends the applicability of small-size associative-memory models to real-world problems.

This paper is organized as follows. In Section II, after introducing the neural network with the nonmonotonic transfer function, we summarize the results obtained for its equilibrium properties by the SCSNA. Then in Section III, we propose a MOS circuit which yields the nonmonotonic transfer characteristic. Section IV shows the behavior of the neural network with 20 units simulated by SPICE at the transistor level for memory retrieval. Section V contains the application to character recognition and Section VI is devoted to summary.

Manuscript received January 27, 1994; revised March 17, 1995 and July 8, 1995.

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Publisher Item Identifier S 1045-9227(96)00177-4.

1045–9227/96$05.00 © 1996 IEEE

II. The Nonmonotonic Neural Network and Its Equilibrium Properties

Time evolution of activity $u_i\,(i = 1, \cdots, N)$ of an analog neural network having a transfer function $f(x)$ is described by the following:

$$\tau \frac{du_i}{dt} = -u_i + \sum_{j=1}^{N} J_{ij} f(u_j) \tag{1}$$

where $J_{ij}\,(i, j = 1, \cdots, N)$ represents the connection from neuron j to neuron i and the second term in the r.h.s. expresses the input to (or the local field of) neuron i. In the present paper, J_{ij} is assumed to be a symmetric Hebbian connection which is defined as

$$J_{ij} = \frac{1}{N} \sum_{\mu=1}^{p} \xi_i^{(\mu)} \xi_j^{(\mu)} \quad (i \neq j), \quad J_{ii} = 0 \tag{2}$$

for p random memory patterns $\xi_i^{(\mu)} = \pm 1\,(\mu = 1, \cdots, p)$ subjecting to the distribution

$$P(\xi) = \tfrac{1}{2}\,\delta_{\xi,+1} + \tfrac{1}{2}\,\delta_{\xi,-1}. \tag{3}$$

Usually $f(x)$ is taken to be a sigmoid function which ensures the existence of a Lyapunov function. Numerical simulations [8] and the detailed theoretical analysis [5]–[7], however, revealed that storage capacities are significantly enhanced if we use nonmonotonic transfer functions. Among the possible variation of nonmonotonic transfer functions, we consider the transfer function presented in Fig. 1

$$f(x) = \begin{cases} 1, & 0 < x < \theta \\ -1, & -\theta < x < 0 \\ 0 & \text{otherwise} \end{cases} \tag{4}$$

which is particularly simple and ensures excellent equilibrium properties.

The SCSNA was applied to nonmonotonic neural network with the above $f(x)$ and its equilibrium properties were extensively studied in [6]. We give a brief summary of the results obtained therein together with the general framework of the SCSNA.

The SCSNA describes the statistical properties of equilibrium states given by $du_i/dt = 0$ in terms of a set of equations for macroscopic order parameters. Let N and $p = \alpha N$ be infinitely large with keeping α finite and choose any one of the embedded random patterns, say ξ, as a reference pattern for retrieval. Then the equations for the pattern overlap $m = (1/N)\,\Sigma_i\,\xi_i f(u_i)$, the Edwards–Anderson like parameter $q = (1/N)\,\Sigma_i f(u_i)^2$ and the sensitivity U of $f(u_i)$ to the noise z at equilibrium are given as [6]

$$m = \left\langle \int_{-\infty}^{\infty} \frac{dz}{\sqrt{2\pi}} \exp\left(-\frac{z^2}{2}\right) \xi Y(\xi, z) \right\rangle_{\xi}, \tag{5}$$

$$q = \left\langle \int_{-\infty}^{\infty} \frac{dz}{\sqrt{2\pi}} \exp\left(-\frac{z^2}{2}\right) Y(\xi, z)^2 \right\rangle_{\xi}, \tag{6}$$

$$U\sqrt{\alpha r} = \left\langle \int_{-\infty}^{\infty} \frac{dz}{\sqrt{2\pi}} \exp\left(-\frac{z^2}{2}\right) z Y(\xi, z) \right\rangle_{\xi} \tag{7}$$

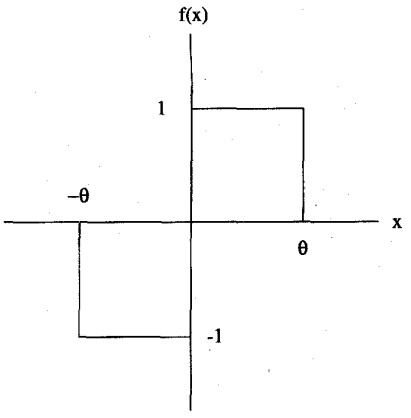


Fig. 1. The nonmonotonic transfer function which was discussed in [6]. This transfer function has not only a simple shape desirable for the realization by a MOS circuit, but also an equilibrium phase diagram particularly attractive for practical purposes.

where the function $Y(z)$ is obtained from the original transfer function (4) through an implicit relation

$$\begin{aligned} Y(\xi, z) &= f[\xi m + \sqrt{\alpha r} z + \Gamma Y(\xi, z)], \\ r &= \frac{q}{(1-U)^2}, \\ \Gamma &= \frac{\alpha U}{1-U}. \end{aligned} \tag{8}$$

We may call Y the renormalized transfer function. In the above expressions, $\langle \cdots \rangle_{\xi}$ stands for an average over the reference pattern $\xi = \pm 1$ while averages over the remaining patterns is represented by the Gaussian integration over z.

Equations (5)–(8) allow one to study a phase diagram for equilibrium states. The retrieval states characterized by pattern overlaps with macroscopic sizes are given by the solutions with $m \neq 0$, $q \neq 0$. Spin-glass solutions with $m = 0$, $q \neq 0$ represent equilibrium states in which no memory patterns are retrieved. The "paramagnetic" solutions with $m = 0$, $q = 0$ will not appear for the present transfer function due to the jump at the origin (Fig. 1) with an infinitely large derivative. The critical storage capacities of neural networks are determined as the upper bounds for the storage ratio α above which the retrieval-state solutions cannot coexist with the spin-glass ones.

A complication in analysis of analog neural networks arises from the presence of the ΓY term in the definition (8) of the renormalized transfer function. In general, (8) admits more than one solution. The prescription for finding an available solution among multiple ones is stated as follows. Any solutions of (8) are expressed as the intersection points of the straight line $h = \Gamma Y + \xi m + \sqrt{\alpha r} z$ and the curve $h = f^{-1}(Y)$. Here the "inverse" function $h = f^{-1}(Y)$ is defined as the locus of points obtained from $Y = f(h)$ by reflection with respects to the $h = Y$ line. If more than one intersection point exists, the external one that also delimits the larger area enclosed between the two relevant curves must be selected. As far as monotonic transfer functions are concerned, the recipe is justified by the replica calculations since it is equivalent to choose a suitable solution for the saddle-point equations (the Maxwell rule).

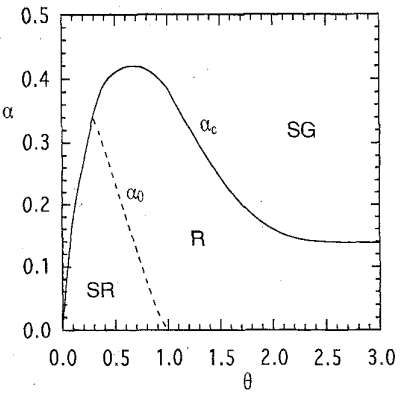


Fig. 2. The phase diagram for equilibrium states of analog neural networks with the nonmonotonic transfer function shown in Fig. 1. Ordinary retrieval, super retrieval, and spin-glass phases are denoted by R, SR, and SG, respectively. A particular feature of the present transfer function other than its simple shape is the presence of super retrieval phase with rather a wide area.

Solving (5)–(7) numerically yields correct phase boundaries of nonmonotonic neural networks for the whole parameter region of θ except for relatively small values ($\theta < 1$). The region of small θ's corresponds to highly-nonmonotonic transfer functions for which equilibrium states described by the retrieval solutions of the SCSNA can no longer be stable. Such instability of the equilibrium states can occur due to the absence of the Lyapunov function. Therefore, numerical simulations must be conducted for these small values of θ to complete the evaluation of the critical boundary of the retrieval states.

Fig. 2 shows the phase diagram of the present neural network [6]. The solid curve represents the critical storage capacity α_c. We see that the α_c takes an optimal value ≈ 0.4 for $\theta \approx 0.6$ and decreases gradually to the well-known value of 0.138 [4] as θ goes to infinity. It is found that α_c is significantly increased when θ takes appropriate values.

A quite new and important feature which was revealed by the SCSNA for the neural network with nonmonotonic transfer function (4) is the existence of the super retrieval phase, or the region below the dashed curve in Fig. 2. In this phase, the noise generated by random patterns other than ξ, i.e., the patterns which are not retrieved at the moment, completely vanishes. Disappearance of the noise was known for the nonlocal pseudoinverse learning rule [9] but not for the local learning rule of Hebb type adopted in the present paper. This surprising phenomenon with extensive numbers of memory patterns and network size ensures that the memory patterns are retrieved with no errors in this phase. The existence of the super retrieval phase for wide ranges of θ and α makes the present neural network particularly attractive for practical purposes, although the effects on the performance of a small-size network, like the present one, are not very significant.

III. A MOS Circuit for the Nonmonotonic Neural Unit

As shown in Fig. 3, the transfer function discussed in the preceding section can be realized by a small number of differential pairs and current mirrors of the MOS transistors. Both input and output, which we denote as V_{in} and V_{out}, respectively, of the unit are given in voltages. The maximum and minimum of the output, which are given, respectively, by ± 1 in (4), are set at voltages $\pm V_m$. Then the threshold θ in the mathematical model corresponds to $V_{th} = \theta V_m$ in the electrically implemented transfer function. Since the present nonmonotonic transfer function is essentially piecewise linear, the circuit structure becomes as simple as that for the sigmoid transfer function [10].

We show that the MOS circuit in fact has the desired nonmonotonic voltage-current characteristic. It is noted that the transfer function $f(x)$ in (4) can be expanded into a linear combination of four step functions

$$f(x) = H(x) - H(-x) + H(-x+\theta) - H(x+\theta),$$
$$H(x) = \begin{cases} 1, & x > 0 \\ 0, & x \le 0. \end{cases} \tag{9}$$

Step-function-like characteristics can be most conveniently obtained by using differential pairs of MOS transistors. In the MOS circuit, transistors M_1 and M_2 are responsible for giving the step-function-like characteristic, which is represented by the first and second terms in (9), at the origin $V_{in} = 0$ of the differential input voltage. Similarly, transistors M_3 and M_6 are responsible for giving similar characteristics, which are represented by the third and fourth terms in (9), at $V_{in} = \pm V_{th}$. The currents flowing into transistors M_4 and M_5 are not used to give any of the step functions appearing in (9). The current I_b of transistor M_b is given by the sum of the currents of M_1 and M_6, while the current I_d of M_d is the sum of those of M_2 and M_3. Thus the current flowing through the well resistance R is given by $I_b - I_d$, and input–output voltage characteristic $V_{out}(V_{in}) = R[I_b(V_{in}) - I_d(V_{in})]$ represents the desired nonmonotonic transfer function (9).

In the simulations, we use the value of parameters listed in Table I for the transistors. Those values of the transistor width and length can be easily realized in the modern device-manufacturing technology. The well resistance R is set at $10\,(k\Omega)$.

IV. Circuit Simulations for the Associative-Memory Network

In this section, we conduct circuit simulations for the network shown in Fig. 5 of the proposed neural units. Since it is of importance in applications to examine the network performance with rather a small N, N is set to as small as 20. The threshold θ was fixed at 0.4 which is found to give a storage capacity of $\alpha_c \approx 0.4$ (see Fig. 2) for an infinitely large network. The memory patterns were assumed to be random ones. All the results were obtained by SPICE.

We show that the network comprising the proposed neural units and the Hebb connection matrix exhibits excellent performance in memory retrieval task. Despite that N is quite small, the memory retrieval properties can be qualitatively understood by the SCSNA results obtained for an infinitely large system. It is easily shown that the circuit given in Fig. 5

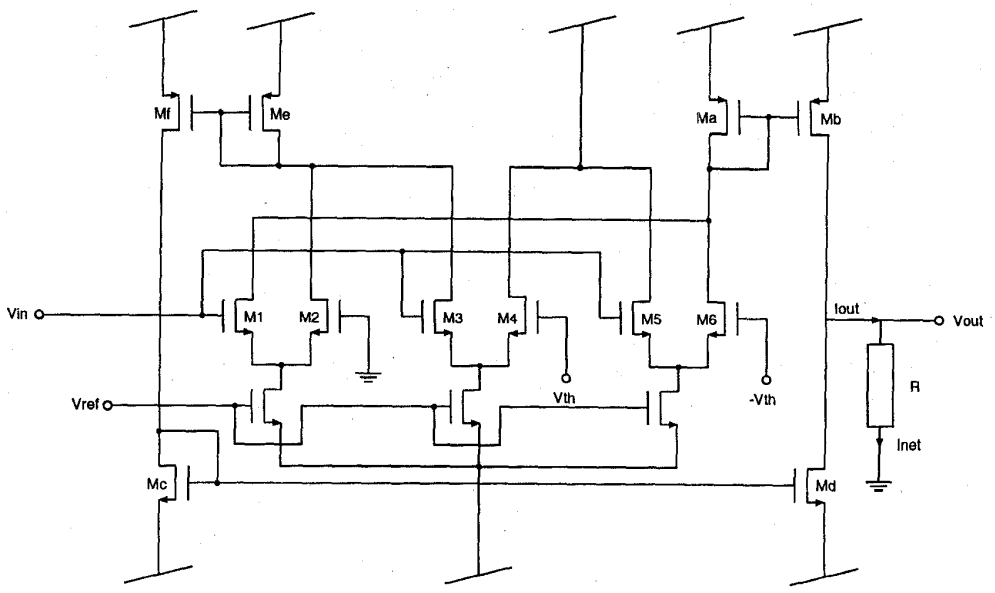


Fig. 3. The MOS circuit for a single neural unit which yield an approximate transfer characteristic of that shown in Fig. 1.

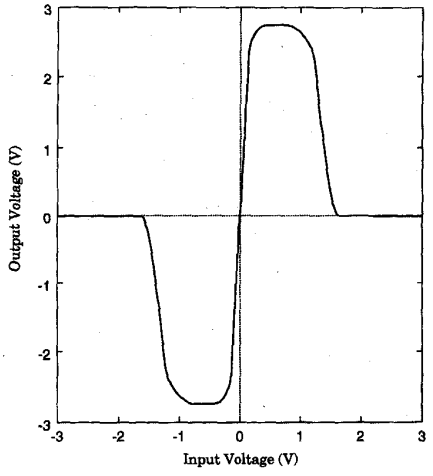


Fig. 4. Simulated input–output characteristic of the single neural unit shown in Fig. 3. The circuit constants and the physical parameters used in the simulations are listed in Table I.

TABLE I
THE CIRCUIT CONSTANTS AND PHYSICAL PARAMETERS ASSUMED IN THE SIMULATIONS. DEFAULT VALUES OF THE SPICE SIMULATOR WERE USED FOR OTHER PHYSICAL PARAMETERS NOT LISTED HERE

	$M_1 \sim M_6$	M_a	M_b	M_c	M_d	M_e, M_f	others
$W(\mu m)/L(\mu m)$	35/2	20/2	200/2	10/2	100/2	50/2	25/2
V_{t0} (V)	1.0	-1.0	-1.0	1.0	1.0	-1.0	1.0
K_p $(\mu m/V^2)$	31	15.6	15.6	31	31	15.6	31

V_{t0} : Zero-bias threshold voltage.
K_p : Transconductance parameter ($\cong \mu C_{ox}$)

is equivalent to the original system described by the differential (1) when $u_i(t)$ and $f[u_i(t)]$ are read as the input voltage $V_{in,i}(t)$ and output voltage $V_{out,i}(t)$ of unit i, respectively.

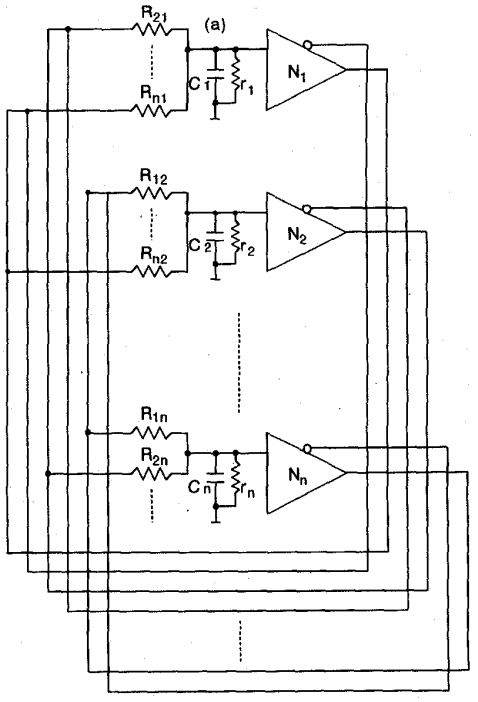


Fig. 5. Associative memory neural network represented by an electric circuit. Each of $N_1, N_2, \cdots, N_n$ represents the neural unit given in Fig. 3.

The current I_1 which flows into node (a) of unit 1 from units 2, 3, $\cdots$, n is expressed as

$$I_1 = -V_{in,1} \sum_{j \neq 1} \frac{1}{R_{j1}} + \sum_{j \neq 1} \frac{\varepsilon_{j1} V_{out,j}}{R_{j1}} \qquad (10)$$

where $\varepsilon_{j1} = \pm 1$ stands for the effect of the wide-range transconductance amplifiers in unit j. If the element J_{j1} of

connection matrix calculated by (2) is negative, the output of the inverting neural unit is to be supplied for unit 1. This means $\varepsilon_{j1} = -1$.

Since the input impedance of each neural unit can be assumed to be infinitely large in the present MOSFET (MOS field effect transistor) implementation, I_1 must be equated to the sum of currents flowing through capacitor C_1 and resistor r_1

$$I_1 = C_1 \frac{dV_{in,1}}{dt} + \frac{V_{in,1}}{r_1}. \tag{11}$$

Similar equations hold for other units and the circuit in Fig. 5 is found to describe a system governed by (1) with

$$\begin{aligned} \tau &= C_i R, \\ J_{ij} &= \frac{\varepsilon_{ji} R}{R_{ji}}, \\ \frac{1}{R} &\equiv \frac{1}{r_i} + \sum_{j \neq i} \frac{1}{R_{ji}}. \end{aligned} \tag{12}$$

We can determine C_i and r_i so as to make the time constant τ unit-independent. In the circuit simulations, τ was taken to be of order 10 (ns).

Some points must be noted when the MOS circuits presented Section III are integrated into a neural circuit such as used in Sections IV and V. In this electrically implemented neural network, the net current $I_{net,i}$ flowing into the well resistance of the ith unit consists of the external current $I_{ex,i} = \Sigma_{j \neq i} \varepsilon_{ji} (V_{in,j} - V_{out,i})/R_{ji}$ from other units and the output current $I_{out,i}$ of the ith unit. This $I_{ex,i}$ reduces or increases the output voltage $|V_{out,i}|$ of the ith unit, since $V_{out,i}$ is given by the product of the well resistance and $I_{net,i}$. When $|I_{net,i}|$ is increased by $I_{ex,i}$, no practical difficulty arises since $V_{out,i}$ is to be saturated with the supply voltage. When $I_{net,i}$ is reduced, however, there can be at least two potential sources that may affect the performance of the electric neural network: i) an increase of V_{th} relative to V_{out}, which implies an effective increase of θ and can result in reducing the storage capacity of the network and ii) V_{out} is negligibly small compared to the supply voltage and the response of an unit is essentially regarded as zero, which corresponds to the extreme case where $f \equiv 0$.

On the present simulations, the transistor dimensions W/L of output transistors M_B and M_D of current mirror circuits were fixed at relatively large values so that the magnitude of $I_{out,i}$ relative to that of $I_{ex,i}$ becomes sufficiently large and the influences of $I_{ex,i}$ on $V_{out,i}$ can be negligibly small. Taking those transistor dimensions larger is a standard technique in fabricating large-scale MOS circuits including neural networks [11].

Further, the value of the well resistance should be smaller than those of the resistances that determine the weights for the connections. This is because our transfer function has vanishing output regions for $|V_{in}| > V_{th}$, where $I_{out,i} = 0$ and hence, $I_{ex,i}$ directly determines $V_{out,i}$. Therefore the well resistance must be sufficiently small so that $|V_{out,i}| \ll V_m$ for $|V_{in}| > V_{th}$. It is to be noted that small nonvanishing values of $V_{out,i}$ for $|V_{in}| > V_{th}$ will not change both qualitative and quantitative features of the memory retrieval of the present neural network, as was shown analytically for the related mathematical model [5].

It is worth remarking that the above-mentioned adjustment of the transistor dimensions and well resistance is unnecessary if the connection weights are implemented by MOS vector multipliers such as discussed in [12], since $I_{ex,i} \equiv 0$ for this type of electrically implemented weight circuits.

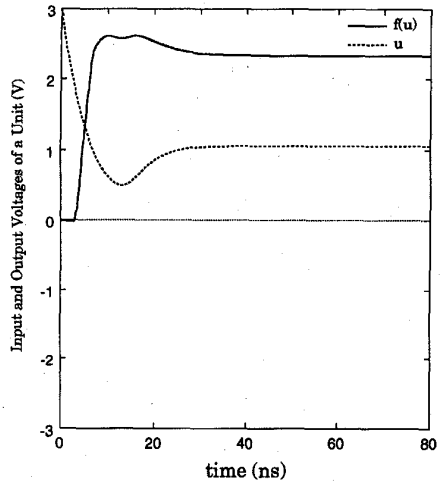
We are interested in the behavior of the network in retrieving memory patterns from initial states representing an incomplete memory pattern including some errors. The initial states of the network are given through input voltages of neural units by $V_{in,i}(0) = \varepsilon_i \xi_i^r V_{dd}$ for a reference pattern $\{\xi_i^r\}$ and $\varepsilon_i = \pm 1$. Setting $\varepsilon_i = -1$ implies that unit i is initially in a "flipped" state, i.e., number of error bits n_{err} in initial states is that of -1 in $\{\varepsilon_i\}$. We examined the time evolution of the network during the pattern retrieval within $6 \leq p \leq 9$ and $0 \leq n_{err} \leq 6$.

We found, within the present simulations, that the network exhibits good performance as long as $n_{err} \leq 5$ when $p = 6\,(\alpha = 0.3)$. For $n_{err} = 6$, the network frequently shows incomplete retrieval of memory patterns. As p is increased, the basins of attraction for memory retrieval are reduced and so does the maximal n_{err} that ensures complete retrieval of memory patterns. For $p = 9$, even initial states with $n_{err} = 1$ end with unsuccessful memory retrieval. Time evolution of neural units with $\xi_i^r = 1$ (the dashed curves) is shown in Fig. 6(a) and (b) for successful memory retrieval when $p = 6$ and $n_{err} = 6$. The unit in Fig. 6(a) starts from a nonflipped initial state while that in Fig. 6(b) from a flipped one. We see in Fig. 6(b) that the output of the unit (the solid curves) is inverted to give the correct values within the time course of a few τ as $u_i(t)$ gradually changes from negative values to positive ones.

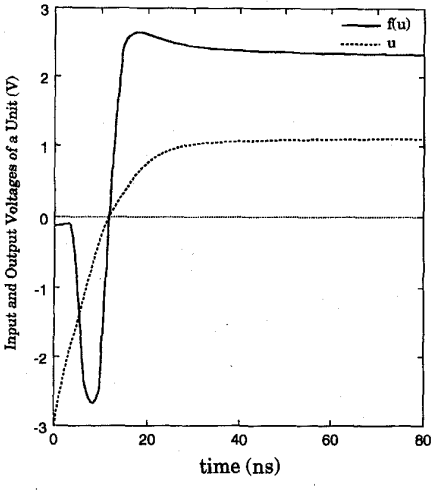
Note that $V_{in,i}(t) \to \xi_i^r V_{th}$ as $t \to \infty$, which coincides with the SCSNA results [6] for equilibrium states, that is, $u_i(t \to \infty) \approx \xi_i^r \theta$. This proves that the present MOS circuit indeed represents the original nonmonotonic neural network. Similar quantities are shown in Fig. 6(c) for a unit with $\xi_i^r = 1$ in the case of unsuccessful memory retrieval with $p = 6$ and $n_{err} = 6$. The unit is seen to fail to retrieve the desired state.

The behavior of network in the above cases of successful and unsuccessful memory retrieval is shown in Fig. 7, in which the behavior of pattern overlap $m_\mu = 1/N \Sigma_i \xi_i^\mu V_{out,i}(t)$ is plotted. In unsuccessful memory retrieval, the network finally settles in the state with a vanishing pattern overlap. This implies that the half of bits carry errors in the final state.

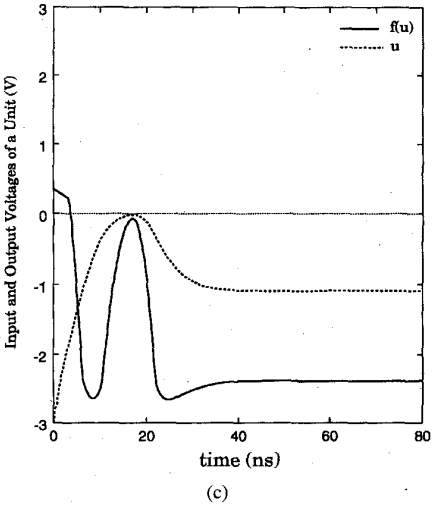
With $N = 20$, increasing or decreasing θ or V_{th} from the optimal value does not rapidly degrade the stability of retrieval states in a manner suggested by the phase diagram in Fig. 2. In general small system size makes any phase transition phenomena obscure since notion of phase transition is explicitly valid only when system size is infinitely large. It is found, however, that the maximal value of n_{err} which ensures successful memory retrieval is sensitively reduced with increasing or decreasing V_{th}.



(a)



(b)



(c)

Fig. 6. Time evolution of neural units in successful (a), (b), and unsuccessful (c) memory retrieval for $p = 6$ and $n_{err} = 6$. The units shown in the figures were loaded with $\xi_i^r = 1$ of the reference pattern and started from initial states $V_{in,i}(0) = \xi_i^r V_{dd}$ (a) and $V_{in,i}(0) = -\xi_i^r V_{dd}$ (b), (c), respectively.

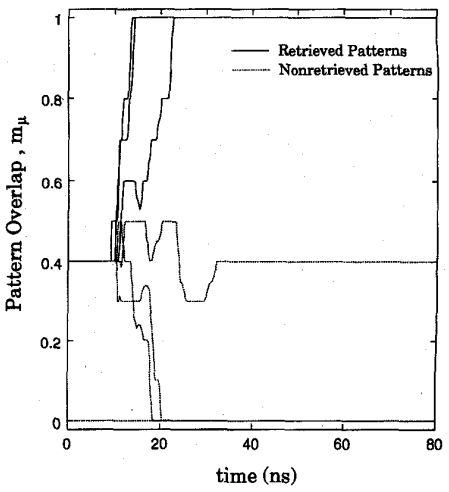


Fig. 7. Time evolution of pattern overlaps in successful and unsuccessful memory retrieval. In the successful memory retrieval, $V_i(t)$ for each neuron takes a value slightly less than unity due to the small decrease in the output of the transfer function near $V_{in} \approx \pm V_{th}$. This results in reducing the value of m_μ $(t \to \infty)$ slightly from unity in the successful memory retrieval.

V. Application: A 35-Neuron Network for Character Recognition

The analog neural networks with monotonic transfer functions are in general not very attractive from applicational points of view, since i) their storage capacities are rather small and ii) the retrieval performance of the networks is poor when real-world memory patterns such as characters are given to them instead of random memory patterns. In this section, we show, by taking character recognition as an example, that a small-size network of the nonmonotonic neural unit can exhibit excellent retrieval properties with realistic nonrandom memory patterns.

In the simulations, 35 neurons were employed to process 7×5 two-dimensional images. The memory patterns are given by 10 digits (0, $\cdots$, 9) represented as 7×5 resolution images, as shown in Fig. 8. The connection matrix was given by (2), in which $\{\xi_i^\mu\}_{\mu=1,\cdots,10}$ now represent these two-dimensional images. Hence, α is approximately given by 0.29. The threshold θ and the number n_{err} of the error bits were fixed at 0.4 and 7, respectively. Noisy patterns which are obtained by flipping n_{err} bits in memory patterns, were given to the neural network as initial states. To examine the performance of the network for an ensemble of the initial states, 50 variations of such noisy patterns were generated from each memory pattern. It is said that the network exhibits a perfect memory-recall if ith memory pattern is always retrieved from all the noisy variations of that memory pattern.

The confusion matrix $\hat{Z}$ was introduced to evaluate the retrieval ability of the neural network, since the perfect memory-recall is, in general, not achieved. Element Z_{ij} of this matrix represents the number of trials in which the steady states evoked from noisy versions of the ith memory pattern are classified as the jth memory pattern. Therefore diagonal element Z_{ii} represents the number of successful memory-recall for the ith memory pattern. In the case of the perfect memory-

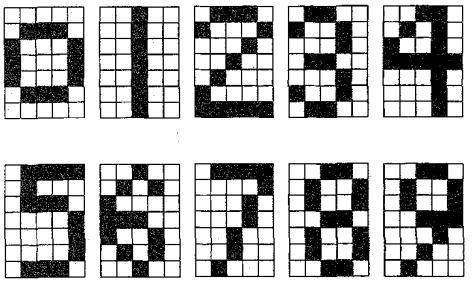


Fig. 8. The 7 × 5 resolution images used as memory patterns in the character recognition task.

TABLE II
THE CONFUSION MATRIX OBTAINED BY SIMULATIONS OF THE 35-NEURON NETWORKS, WITH (a) MONOTONIC AND (b) NONMONOTONIC TRANSFER FUNCTIONS, STORING THE DIGITS SHOWN IN FIG. 8

Retrieved Pattern \ Initial Pattern	0	1	2	3	4	5	6	7	8	9
0	43	0	4	0	0	2	0	1	1	0
1	0	0	0	0	0	0	0	0	0	0
2	4	48	46	12	5	48	1	48	48	50
3	0	0	0	26	0	0	0	0	0	0
4	0	0	0	0	0	0	0	0	0	0
5	0	0	0	0	0	0	0	0	0	0
6	3	2	0	12	45	0	49	1	1	0
7	0	0	0	0	0	0	0	0	0	0
8	0	0	0	0	0	0	0	0	0	0
9	0	0	0	0	0	0	0	0	0	0

(a)

Retrieved Pattern \ Initial Pattern	0	1	2	3	4	5	6	7	8	9
0	46	0	0	0	0	0	0	0	0	0
1	0	40	0	0	0	0	0	0	0	0
2	0	6	48	2	0	5	0	4	0	0
3	0	0	1	45	0	0	0	0	0	0
4	0	0	0	0	44	0	0	0	0	0
5	0	0	0	0	0	45	0	0	0	0
6	4	1	1	3	6	0	50	1	0	0
7	0	3	0	0	0	0	0	45	1	0
8	0	0	0	0	0	0	0	0	49	0
9	0	0	0	0	0	0	0	0	0	50

(b)

recall, it should coincide with the total number of trials, or that of the variations of the noisy patterns per memory pattern, and $Z_{ij}(i \neq j)$ should be zero.

With the large value of α assumed here, monotonic neural networks cannot function as a character recognizer. For the sake of later comparison, however, the confusion matrix was calculated in Table II(a) for a neural network with a sigmoidal transfer function. When the target pattern was not retrieved, the evoked pattern in general did not coincide with any of the memory patterns. In calculating the confusion matrix, we classified such an evoked pattern as one of the memory patterns which has a maximum pattern overlap with it. It is seen that characters "0," "2," and "6" have the attraction basins of finite sizes, while others do not have such basins. The confusion matrix obtained by the simulations of the nonmonotonic neural network is shown in Table II(b). In most of the cases where a target memory pattern was retrieved, the pattern was evoked without errors. It is seen that the diagonal elements are significantly larger than the off-diagonal ones, which implies that each memory pattern has finite basins of attraction unlike the case for the monotonic neural network. This proves that the nonmonotonic neural network exhibits an excellent retrieval ability in the present character recognition task.

VI. CONCLUSION

We have proposed a MOS circuit representing an analog neural processing unit with a nonmonotonic transfer function and conducted circuit simulations of associative memory networks comprising a few tens of the nonmonotonic neurons. The transfer function discussed in this study is of particular importance since analytic studies in the limit of an infinite number of neurons have revealed its excellent equilibrium properties: they include the enhancement of storage capacity, the presence of the super retrieval phase for wide ranges of the model parameters, and the suppression of spurious-state distribution. In the present circuit simulations of small-scale neural networks storing a small number of memory patterns or characters, the last two properties are unlikely to take part in improving the performance of the neural networks. In large-scale networks with hundreds or thousands of neurons, they can be significant for improving the quality of retrieved patterns and enlarging the basins of attraction. From applicational points of view, however, more important is the fact that employing nonmonotonic transfer functions drastically improves the performance of associative memory neural networks even for rather small number of neurons. In fact, the results of character recognition with 10 digits have suggested the usefulness of nonmonotonic transfer functions in solving real-world problems with small-scale neural networks. Since available space on a chip for the hardware implementation of neural circuits is limited, the smallness of required network size is the great advantage of using nonmonotonic transfer functions.

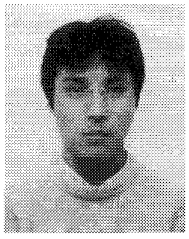
ACKNOWLEDGMENT

The authors very much benefited from a fruitful discussion with Dr. T. Matsumoto of Waseda University and Dr. H. Kobayashi of Teratec Corporation. The authors also thank them for carefully reading this manuscript. The comments from Dr. T. Kanungo of Washington University were very useful for designing the model application to character recognition. Cooperation of K. Satoh of Tokai University was indispensable for completing the present research.

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