A Highly Sensitive Thermosensing CMOS Circuit Based on Self-Biasing Circuit Technique

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A thermosensing CMOS circuit that changes its internal voltage steeply at a critical temperature was developed. The circuit is based on a self-biasing circuit technique and uses the temperature-sensitive characteristics of MOSFETs operating in the subthreshold region. To develop this sensor device, a method to analyze self-biasing circuits, which is different from a conventional one, was employed. This method is useful for understanding the self-biasing circuit operation. A temperature sensor device makes use of a MOSFET resistor’s transition from a strong inversion to a weak-inversion or subthreshold operation. The temperature at which the transition occurs can be set to a desired value by adjusting the parameters of MOSFETs in the circuit. The sensor LSI can be made using a standard CMOS process and can be used as over-temperature and over-current protectors for LSI circuits. © 2009 Institute of Electrical Engineers of Japan. Published by John Wiley & Sons, Inc.

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1. Introduction

A promising area of research and development in solid-state microelectronics is exploring ultralow-power analog LSIs that can be used for new applications. To further advance such LSIs, we have developed sensor LSIs that consist of subthreshold MOSFETs, or MOSFETs operating in a weak-inversion region[1–4]. We herein propose a temperature switch sensor LSI based on a self-biasing circuit technique. A self-biasing circuit can be used as a temperature sensor by making use of the temperature characteristics of its current and voltage.

Safe and stable operation of electrical products is one of the most important requirements that must be addressed during the design phases. To ensure the stable operation of electrical products, thermally sensitive resistor sensors, or thermistors, are widely used to monitor the temperature of various products and detect any undesirable, or dangerous increases in temperature[5]. A critical temperature resistor (CTR) thermistor is widely used for this purpose because it exhibits a sharp change in resistance at a threshold temperature and is suitable for sensing overheating[6]. Therefore, CTR thermistors are often used in overheating detectors, over-current protectors, and temperature-compensation devices. The sharp change in their resistance is caused by a phase transition of its conductive ceramics. However, because a CTR thermistor is made of ceramics, they are incompatible with silicon LSIs. In addition, it is difficult to set a threshold temperature over a wide range. These problems, however, can be solved by developing a temperature detection system consisting of monolithic LSI circuits. Although such a system can be constructed by combining a conventional temperature sensor (e.g. diode, or bipolar devices) with an AD converter and a microprocessor, the system requires several integrated circuits and is, therefore, impractical due to its high-cost and high-power consumption.

A temperature sensor LSI consisting of only MOSFETs was proposed in the literature[7,8]. The circuit is a highly sensitive thermosensing CMOS circuit by using the temperature characteristics of MOSFETs operating in a subthreshold region. This circuit -which we call a critical temperature switch (CTS) circuit- is based on a self-biasing circuit technique and shows a sharp transition of its internal voltage, similar to that of CTR thermistors. However, operation principle of the circuit was not clear in the literature, and the critical temperature for switching could not be estimated theoretically. In this paper, a method to analyze a self-biasing circuit, which is different from a conventional one, is employed to solve these problems. The analysis method is useful to understand the mechanisms of the temperature switching function of the CTS circuit. Theoretical critical temperature for switching is also established in this paper. This device is free from the limitations inevitable in CTR thermistors. The paper is organized as follows: the method to analyze
self-biasing circuits is described in Section 2, a CTS core circuit and entire circuit configuration are presented in Sections 3 and 4, respectively, experimental results are shown in Section 5, and we conclude the paper in Section 6.

2. Self-Biasing Circuit

Self-biasing circuits are widely used to generate a reference voltage and current in LSIs because of their simple and stable operation [6,7]. Because the reference current and voltage of the circuit are determined by device parameters, these references are temperature sensitive and, therefore, can be used as a temperature sensor signal.

In this section, we outline the method to analyze a self-biasing circuit and highlight the differences from a conventional one. The method we employed enables better understanding of the physical operation principle of a self-biasing circuit. First, a conventional analysis method is described, and then the method employed in this work is presented, focusing on a beta multiplier reference (BMR) circuit as a typical example of self-biasing circuit [6].

Figure 1(a) shows a BMR circuit. The circuit consists of NMOS transistors (M1–M4), a resistor (R), and a PMOS current mirror (M3–M4). We set the aspect ratios of the transistors such that $K_2/K_1 = k > 1$ and $K_3 = K_4$, where $K_i$ ($i = 1–4$) is the aspect ratio of transistors M$i$.

2.1. Conventional analysis method The circuit in a conventional analysis method is divided into two subcircuits as follows:

(1) diode-connected transistor subcircuit (M1);
(2) source-degenerated transistor subcircuit (M2–R); and
(3) PMOS current mirror (CM) subcircuit (M3–M4).

These subcircuits operate as a current-to-voltage ($I_1 - V_1$) conversion subcircuit, a voltage-to-current ($V_1 - I_2$) conversion subcircuit, and a current-to-current ($I_2 = I_1$) conversion subcircuit, respectively. The BMR circuit can be considered as a feedback connection of these subcircuits, as shown in Fig. 2(b). The $I_1 - V_1$ subcircuit generates a voltage, $V_1$, from current $I_1$ and applies the voltage to the $V_1 - I_2$ subcircuit. The $V_1 - I_2$ subcircuit generates current $I_2$. The CM subcircuit is used to make the current of $I_2$ equal the current of $I_1$.

The operating point of the BMR circuit can be determined from the transfer characteristics of these subcircuits. Figure 3(a)
The analysis also shows that the zero point of the circuit is not the operating point. As shown in Fig. 3(b), current $I_2$ in the low current level region is larger than current $I_1$ by a current gain factor of $K$. The feedback in the circuit in this region is positive, and the circuit will drive itself out of this state. Therefore, the circuit has only one operating point. However, this does not mean that a start-up circuit is unnecessary for the circuit implementation. The circuit could not operate quickly in the low-current level region due to its low driving current. Therefore, it takes time to settle in the operating point. A start-up circuit is required because the circuit is required to operate immediately once the power is turned on.

### 3. Critical Temperature Switch Circuit

By using temperature characteristics of the self-biasing circuit, a CTS circuit can be constructed. At low temperatures, the circuit has two possible operating points. At temperatures greater than the critical temperature, the circuit loses one of its operating points because each current transfer curve has different temperature characteristics. The CTS circuit utilizes this loss of operating point as a switching operation.

#### 3.1. Circuit configuration and its operation

Figure 4(a) shows a proposed CTS circuit. This circuit is based on a BMR circuit and uses a MOSFET resistor $M_1$ instead of an ordinary resistor $R$. To generate higher gate voltages for $M_1$, we adapted a cascode configuration of nMOSFETs. The aspect ratios of transistors were set such that $K_1 > K_2$, $K_3 = K_4 = K_5$, and $K_6 = K_7$. All MOSFETs in the circuit were operated in a subthreshold region, except for $M_5$. The current mirror circuit, consisting of $M_6$ and $M_7$, makes the current of $I_1$ equal the current $I_2$. The circuit shows a switching operation such that node voltage $V_s$ changes drastically from a higher value to a lower one at a critical temperature ($T_C$). The detailed operation is discussed below.

The circuit operation can be analyzed using the transfer curves for the left ($M_5 - M_6$) and right ($M_2 - M_3 - M_4$) branches, as shown in Fig. 4(b). Current $I_1$, in the left branch, flows through transistors $M_2$ and $M_4$ and generates voltage $V_s$, and current $I_2$, in the right branch, is controlled by voltage $V_s$. Because, $I_1$ and $I_2$ equal each other because of the PMOS current mirror, we can find the operating point of the circuit by observing the point at which the two transfer curves, $I_1 = V_s$ and $V_s - I_2$ curves, of the circuit intersect. The results are

![Fig. 2](image_url)

Fig. 2 (a) Three subcircuits for BMR circuit analysis, and (b) circuit’s feedback connection

![Fig. 3](image_url)

Fig. 3 (a) Transfer curves of BMR circuit, and (b) its partial enlarged view
illustrated in Fig. 5(a)–(c) in which $I_1$ and $I_2$ are plotted as a function of voltage $V_{b}$ at different temperatures. At low temperatures, the two curves intersect at points A and B, as shown in Fig. 5(a). Point A is a stable operating point, while point B is an unstable point. Point B can be an operating point of the circuit in this analysis. However, if there will be a small noise or a disturbance, the circuit operating at point B will change the internal voltage and current to higher or lower values than that of point B. After losing the operating point from point B, the circuit cannot operate at the same operating point of B. This is because the generation process of internal current and voltage in the circuit changes at the boundary point of B, due to the two curves of $I_1 - V_b$ and $V_b - I_2$ in Fig. 5. This phenomenon can be described as follows: Once the voltage of $V_b$ in the circuit becomes higher than the voltage of point B, the voltage generates a larger current than that of point B from the transfer curve of $V_b - I_2$. The generated current also generates a larger voltage than that of point B from the curve of $I_1 - V_b$. The circuit repeats the above process, and settles into the stable point A. In contrast, once the voltage of $V_b$ is lower than B, the voltage generates a smaller current than point B from the curve of $V_b - I_2$. The generated current also generates a smaller voltage than that of point B from the curve of $I_1 - V_b$. The circuit repeats the above process, and then settles into the zero. Therefore, the circuit changes its settling points at the boundary point of B. The circuit has two possible operating points— one is point A, and the other is zero (therefore, $I_1 = I_2 = 0$, and $V_b = 0$) —based on its initial condition.

As the temperature increases, the intersection points of A and B approach each other because the temperature characteristics of the two transfer curves are different from each other (Fig. 5(b)). At the critical (or threshold) temperature, the intersections of A and B overlap each other. At temperatures that exceed critical temperature $T_c$, the two curves do not intersect as shown in Fig. 5(c). Therefore, the circuit operates at a zero point ($I_1 = I_2 = 0$, and $V_b = 0$). The CTS circuit shows a switching operation at a critical temperature because the operating point of the circuit transits from A to zero.

3.2. Critical temperature The critical temperature can be calculated theoretically. The CTS circuit we developed uses the characteristic of a MOSFET operating in a subthreshold region. The subthreshold drain current, $I_D$, through a MOSFET is an exponential function of gate-source voltage $V_{GS}$ and is given by

$$I_D = I_0 \exp \left( \frac{V_{GS} - V_{TH}}{\eta V_T} \right)$$

where $I_0$ is a process-dependent parameter, $V_T (= k_BT/q)$ is the thermal voltage, $k_B$ is the Boltzmann constant, $T$ is the absolute temperature, $\eta$ is the sub-threshold slope factor, and $V_{TH}$ is the threshold voltage of the MOSFET [8–10].

In the CTS circuit shown in Fig. 4(a), gate-source voltage $V_{GS2}$ in transistor M2 must equal the sum of gate-source voltage $V_{GS3}$ in M3 and drain-source voltage $V_D$ in M1.

$$V_{GS2} = V_{GS3} + V_D.$$  \hspace{1cm} (2)

Because the current through transistor M2 and current through transistor M1 are equal, (2) can be rewritten as

$$V_D = \eta V_T \ln (K),$$  \hspace{1cm} (3)

where $K$ is the ratio between aspect ratios $K_2$ and $K_3$ in M2 and M3; that is, $K = K_2/K_3$. Because transistors M2 and M3 are connected in a cascode configuration, gate voltage $V_b$ of M1 can be made higher than the threshold voltage of M1. At this condition, transistor M1 operates in a strong inversion and triode region. Current $I$ in transistor M1 is expressed as

$$I = \beta_1 \left( (V_b - V_{TH}) V_D - \frac{1}{2} V_D^2 \right).$$  \hspace{1cm} (4)

where $\beta_1$ is the current gain factor of M1. The last term in (4) can be ignored because transistor M1 operates in deep triode region. Therefore, from (1), (3) and (4), current $I$ and gate voltage $V_b$ are given by

$$I = \beta_2 (V_b - V_{TH}) \eta V_T \ln (K),$$

$$V_b = 2V_{TH} + 2\eta V_T \ln \left( \frac{I}{I_0} \right).$$

From these equations, current $I$ and voltage $V_b$ in the circuit are determined by each other.
The temperature dependence of threshold voltage \( V_{\text{TH}} \) and mobility \( \mu \) are expressed as

\[
V_{\text{TH}} = V_{\text{TH0}} - \kappa T
\]

\[
\mu = \mu_0 \left( \frac{I}{I_0} \right)^m
\]

where \( V_{\text{TH0}} \) is the threshold voltage in an absolute zero temperature, \( \kappa \) is the temperature coefficient of the threshold voltage, \( \mu_0 \) is the mobility at temperature \( T_0 \), and \( m \) is the temperature exponent factor of mobility[15]. From (5)–(8), we find that temperature coefficient \( (T_C)_I \) of the current is given by

\[
(TC_I) = \frac{1}{T} \frac{dI}{dT} = \frac{1}{T} \frac{d(V_b - V_{\text{TH}})}{dT} + \frac{1}{T} \frac{dV_T}{dT}
\]

\[
= \frac{1 - m}{T} \frac{V_b - V_{\text{TH}}}{V_b - V_{\text{TH}}} \times \left( -\kappa + 2\eta V_T \left( \ln \left( \frac{I}{I_0} \right) + \frac{dV_T}{dI} \frac{1}{T_0} \right) \right)
\]

Equation (9) can be rewritten,

\[
(TC_I) = \frac{1}{T} \frac{dV_b}{dT} - \frac{2\eta V_T}{V_b - V_{\text{TH}}} \left( \ln \left( \frac{I}{I_0} \right) - (2 - m) \right)
\]

\[
= \frac{T}{V_{\text{A}}} (V_b - V_{\text{TH}} - 2\eta V_T)
\]

\[
V_{\text{A}} = (1 - m)(V_b - V_{\text{TH}}) - \kappa T + 2\eta V_T \left( \ln \left( \frac{I}{I_0} \right) - (2 - m) \right)
\]

For a standard CMOS process, the numerator and denominator in (10) are a negative and a positive, respectively. Therefore, current \( I \) decreases with temperature. The denominator in (10) also decreases with temperature. At the critical temperature, the denominator becomes zero and the slope of the current with temperature decreases toward negative infinity. This phenomenon produces a sharp change in current \( I \) and voltage \( V_b \) and a switching operation of the circuit. From (10), the threshold condition of the circuit is given by

\[
V_b - V_{\text{TH}} - 2\eta V_T = 0
\]

From this condition, the critical temperature for the sharp change can be given by

\[
T_C = \frac{V_{\text{TH}}}{2\eta \left( \frac{1}{d\ln(K)} \right) - \ln(K)}
\]

where \( M \) is the ratio of aspect ratio in \( M_1 \) and \( M_2 \) \( (M = K_1/K_2) \). The critical temperature can be controlled by changing the circuit parameters.

### 3.3. Simulation results

Operation of the CTS circuit in Fig. 4(a) was confirmed by using a SPICE simulation with a set of 0.35 \( \mu \)m CMOS parameters and an 1.5 V power supply. Figure 6 shows the change in \( V_b \) as a function of increasing and decreasing temperature with three different parameters \( K \). The ratio of the aspect ratios of \( M_2 \) and \( M_3 \) was set to 1.2–2.0 as a parameter. The aspect ratio of \( M_1 \) was set to 0.05. Voltage \( V_b \) decreases as the temperature increases, and then drops suddenly at the critical temperature. Changing parameter \( K \) can set the critical temperature. When the circuit operates at temperature higher than the critical temperature, voltage \( V_b \) drops down to a lower voltage. However, voltage \( V_b \) once dropped, does not return to a high voltage even if the temperature decreases below the critical temperature again because the \( V_b \) is smaller than unstable point B. This characteristic of the CTS circuit is also shown in Fig. 6. The unstable operating point creates two possible operating points for voltage \( V_b \) below a critical temperature. Figure 7 shows critical temperature as a function of \( K \), with the channel width of \( M_1 \) as a parameter. Theoretical critical temperatures calculated from (12) are also plotted. These results show that the critical temperature can be set over a wide range from 20 to 100 °C by simply changing the circuit parameters.
Because the temperature characteristics of the circuit are determined by transistors M1, M2, M3, and M4 as discussed previously, the temperature characteristics of the other transistors have an insignificant effect on the circuit operation. However, the variation of the threshold voltage have significant impact on the circuit operation, especially for critical temperature $T_C$ as shown in (12), $V_{TH1}$ which is related to the threshold voltage of a MOSFET, critical temperature $T_C$ will change directly with the threshold voltage variation. The parameter $V_{TH1}$ in (12) originates from the threshold voltage of transistor $M_1$. Therefore, if the gate bias voltage is generated so that the voltage monitors the threshold voltage variation, the accuracy in (12) can be improved. We are now developing such system by using the reference voltage circuit which monitors the threshold voltage of a MOSFET in an LSI chip [14].

4. Circuit Configuration

The CTS circuit performs a switching operation by monitoring voltage $V_b$, which changes from a higher (strong-inversion bias condition for $M_1$) to a lower voltage (subthreshold bias condition for $M_1$) with temperature. However, the CTS circuit shows different behaviors when it operates with decreasing temperature after increasing temperature as shown in Fig. 6. This phenomenon is due to the unstable operating point B shown in Fig. 5. When the circuit operates at temperature higher than critical temperature, voltage $V_b$ drops down to a lower voltage. However, voltage $V_b$, once dropped, does not return to a high voltage even if temperature decreases again below the critical temperature because $V_b$ is smaller than the unstable point B.

To cancel the effect of the unstable operating point B, we used a subcircuit to reset voltage $V_b$ periodically to a higher voltage (higher than the unstable operating point voltage). This resetting enabled transistor $M_1$ to be returned to a strong-inversion region at temperatures less than the critical temperature. Figure 8 shows the total system including the resetting subcircuit. The subcircuit consists of a ring oscillator, a frequency divider, and a resetting transistor, $M_{RST}$, connected to the CTS circuit. We used a nanoampere-current source [11], and by this current the ring oscillator is driven and produces a square wave and produces a resetting pulse (RST) and sampling pulse (SMP). Transistor $M_{RST}$ accepts the resetting pulse and periodically sets $V_b$ to a high voltage, and as a result, sets $M_1$ to a strong-inversion region periodically. Voltage $V_b$ is sampled periodically with an SMP and is retrieved as an output voltage, $V_{OUT}$, on the capacitance, $C_C$, and then it is output as a digital signal ($D_{OUT}$) after through a current-source inverter and a current-limited inverter.

We confirmed the resetting operation by using a SPICE simulation. A CTS circuit with a critical temperature of 77.6°C was used, and temperature was assumed to be 75 and 80°C. At temperatures lower than the critical temperature ($T = 7°C$), the CTS circuit should produce a high voltage output. However, because of the effect of the unstable operating point, the CTS circuit produced a low-voltage output when the initial output was low. This was corrected by the resetting operation. The results are shown in Fig. 9(a). The initial voltage of $V_b$ was set at 0 V; therefore, the initial output was 0, an incorrect output for a temperature ($T = 75°C$) lower than the CTS threshold condition ($T_C = 77.6°C$). After the first resetting pulse was applied to the CTS circuit, voltage $V_b$ was set at a voltage greater than the unstable operating point voltage. As a result, voltage $V_b$ operated at the correct voltage output and, after that, maintained its correct output. At temperatures greater than the critical temperature ($T = 80°C$), the CTS circuit should produce a low-voltage output. The results are shown in Fig. 9(b). The initial voltage of $V_b$ was also set to 0 V. With a resetting pulse, voltage $V_b$ was set to higher voltage but, because the circuit no longer had any operating points at this temperature, decreased to a lower voltage. The sampling pulse correctly retrieved the low voltage of $V_b$ and output in $D_{OUT}$ low digital signal, correctly.

5. Measurement Results

To verify the circuit operation, we performed a measurement of the CTS core circuit shown in Fig. 4(a) by using a discrete MOSFETs: nMOSFET (2SK1398) and pMOSFET (2SJ184)[12]. Figure 10 shows measurement setup including a DC bias generator, thermostatic chamber, and its measurement board. In the measurement, transistor widths for $M_2$ - $M_7$ were

![Fig. 8 CTS circuit with resetting subcircuit](image-url)
controlled by connecting transistors in parallel and the ratio of \( K = (K_3/K_2) \) was set to 2. Power supply voltage was set at 5 V. The temperature was increased with time at the rate of 1.1 \(^\circ\)C/min.). Figure 11 shows the results of the output voltage of \( V_b \) in the temperature range of 20–120\(^\circ\)C. To avoid the effect of unstable operating point B, the output voltage of \( V_b \) was initialized to the higher voltage of supply voltage at the beginning. The output voltage decreased as the temperature increases, and then dropped steeply at the critical temperature about 90\(^\circ\)C. The CTS circuit operation was confirmed by experimental results using a discrete MOSFETs.

In this measurement, we showed and confirmed the CTS circuit operation, which was discussed in the previous sections, by using a commercial discrete MOSFETs. However, we are now planning to fabricate a monolithic LSI chip including a CTS core circuit and a resetting circuit by using a standard CMOS technology.

Fig. 9 Reset operation of circuit. Initial voltage of \( V_b \) was set to 0 V. Simulated at temperature of (a) 75\(^\circ\)C (critical temperature of CTS circuit was 77.6\(^\circ\)C), and (b) 80\(^\circ\)C

Fig. 10 Left: measurement setup. Right: measurement board

Fig. 11 Measurement results of the output voltage of \( V_b \) in the temperature range of 20–120\(^\circ\)C.
A HIGHLY SENSITIVE THERMOSENSING CMOS CIRCUIT

6. Conclusion

A thermosensing CMOS circuit—CTS circuit—consisting of subthreshold MOSFET circuit was developed capable of changing its internal voltage steeply at a critical temperature. The circuit is based on a self-biasing circuit technique and uses the temperature-sensitive characteristics of MOSFETs operating in the subthreshold region. To develop a sensor LSI, we employed a method to analyze self-biasing circuits that is different from a conventional one. The temperature for the transition can be set to a desired value by adjusting the parameters of MOSFETs in a circuit. The sensor LSI can be made using a standard CMOS process and be used as over-temperature and over-current protectors for LSI circuits.

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References


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