A Digital Vision Chip for Early Feature Extraction with Rotated Template-Matching CA

Masayuki Ikebe, and Tetsuya Asai

Graduate School of Information Science and Technology, Hokkaido University
Kita 14, Nishi 9, Kita-ku, Sapporo 060-0814, Japan
E-mail: ikebe@ist.hokudai.ac.jp
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We discuss a cellular-automata (CA) LSI core that extracts early features of objects in images, such as sizes and skeletons. A CMOS-image sensor with a CA core enables high-speed image processing. We propose an efficient CA algorithm based on rotated template matching. Each cell circuit in the proposed CA is implemented by a digital circuit, and transistors in each cell circuit number 198 in full customized design. The CA LSI consists of a large number of cell circuits operating in parallel to ensure fast, efficient object extraction as the number of cells increases. With a 0.25-μm CMOS process, the total area of each cell circuit is $30\times30\mu m^2$. Simulation results indicated that image processing with 320×240 cells operates at up to 25MHz.

Keywords: cellular automata, high-speed image processing, rotated erosion, CMOS image sensor, feature extraction

1. Introduction

This article discusses a cellular automata (CA) LSI core that enables high-speed parallel image processing. Advances in broadband communication with the dissemination of computers enable comparatively large amounts of data to be processed and images to be exchanged, but this places a heavy load on systems. Digital cameras are widely used for obtaining image data and are components of almost all cellphones. The heart of the digital camera is a CCD or CMOS image sensor specifically developed for portable applications, monitoring, and in-vehicle use. CMOS image sensors are used in image-processing hardware thanks to integrated peripheral circuits using the CMOS process. In real-time image-processing applications, image quality enhancement, compression, and recognition are important. In image quality enhancement and compression, the frame rate is fixed by specified standards, but not for image recognition. Manufacturers constantly seek new and better ways to meet frame rate and power consumption requirements. If processing is fast, we can develop applications while considering column and fully parallel architecture.

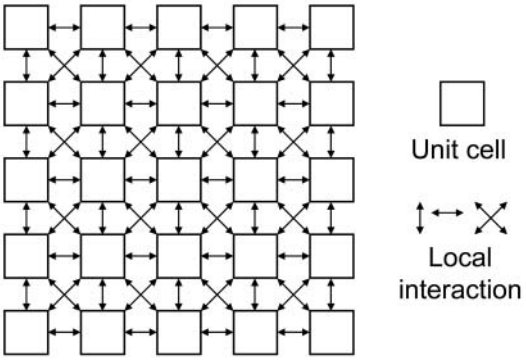


Fig. 1. CA.

We focus on image recognition to implement an LSI core that conducts high-speed processing to obtain early features of images. We used a fully parallel CA architecture, and describe an LSI core that skeletonizes and extracts objects and sizes from images.

Section 2 generally describes CA and the size extraction. Section 3 details processing algorithms for executing special erosion for binary images. Section 4 proposes implementing a cellular circuit for the algorithms. Section 5 simulates circuits to demonstrate their ability to process images at high rates.

2. Image Processing on CA

We introduce a general description of CA (detailed in Refs.[1, 2]). CA have a parallel, distributed architecture. CA are configured as a matrix of unit cells that mutually interact (**Fig.1**). Each unit cell assumes a binary, ternary, or higher state that changes synchronously with all cells at each step in time. Each subsequent cell state is determined by its current state and those of its neighboring cells. Images are processed by setting up interactions between current and neighboring cells states (**Figs.2(a)-(c)**).

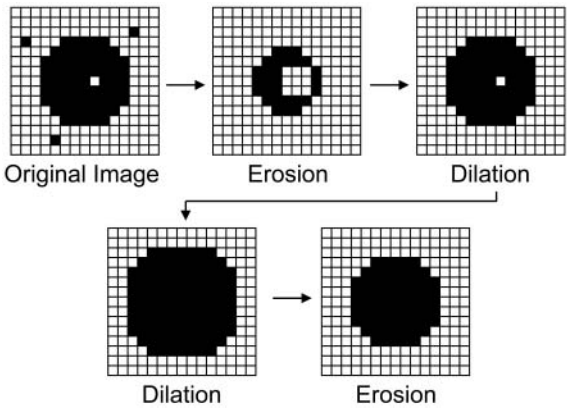
CA is effective in image processing, such as Mathematical Morphology [3] and Discrete Time Cellular Neural Network [4], done performed only by neighboring pixels, but not for operation requiring coordinate information on pixels such as object rotation and expansion. CA ex-

Current state	State of 8neighbor cells	Next state
1	Any states different from those shown below	0
	:0 :1	1
0	Any state	0

(a)

Current state	State of 8neighbor cells	Next state
0	Any states different from those shown below	1
	:0 :1	0
1	Any state	1

(b)



(c)

Fig. 2. Example of image processing by CA; (a) templates for erosion, (b) templates for dilation and (c) noise reduction using dilation and erosion.

tends operation to processing multilevel images. We previously proposed CA-LSI for Differential of Gaussian filtering [5]. Noise removal, edge detection, edge enhancement (with noise removal), and motion detection are possible using the above architecture, but binary images are processed assuming applications the amount extraction of features for image recognition.

We discuss size extraction of multiple objects using CA. We easily extract the size of single object by projecting it onto Cartesian coordinates, but projection cannot be used to extract the size of multiple objects in an image, so we propose extracting the size of multiple objects using the erosion and dilation (**Fig.3**). First, we binalize images. An image is the initial input i) in **Fig.3** for CA. As time passes, objects are reduced in size by erosion. Here, we assume that a small object becomes a dot at $t = \Delta t1$ ii) in **Fig.3**, while a large object becomes a dot at $t = \Delta t1 + \Delta t2$ iii) in **Fig.3**. At iii), a large object leaves a mark. Erosion time thus implicitly indicates object size. Here we focus on large objects and start dilation at iii). When $\Delta t1 + \Delta t2$ passed after dilation starts, the mark grows to the same

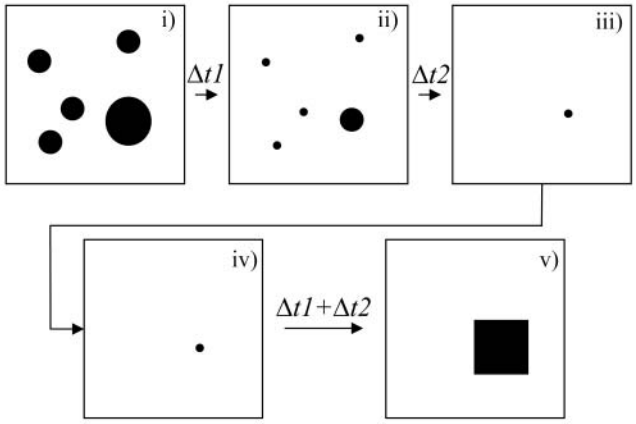


Fig. 3. Concept of size and position extraction for multiple objects by CA. In the sequence i)-ii)-iii), circular objects are reduced by erosion as time steps proceed, while in iv)-v), the minimized dot in iii) is expanded by dilation.

size as the original object, showing the same size and position of the original object because it is evenly contracted and expanded in every direction. We thus use it to extract windows and, by controlling processing time, can handle different sized objects.

3. Rotated Template Matching for CA

Based on rotated template matching, we propose a CA model for VLSI. To imitate erosion that produces a dot representing a contracted object (sometimes called "shrinking," but here referred to as "rotated erosion"), we used templates as shown in **Fig.4(a)**.

We consider "erosion" applied to interrelations between eight neighboring cells. Because all cells in an automaton operate in parallel, it is difficult to transform objects whose width is an even number of pixels into one-pixel-size central points. (An object erased evenly from both sides eventually disappears.) Erosion is thus done by successively changing templates. We discuss template modification through rotation below. Templates in erosion are obtained by sampling states of the eight neighboring cells to deform objects by moving in one direction over the top, bottom, left, and right cells. By rotating each template 90° for each erosion step, we gradually contract objects of a certain thickness from four directions which thus contracts features of any size.

By partially modifying templates for rotated erosion, we apply them to applications such as skeletonization (**Fig.4(b)**). In skeletonization, two templates are alternately selected from four templates for each time step as A,B $\rightarrow$ C,D. A Voronoi diagram is generated using the above operations by partitioning a plane with n points into n convex polygons so each polygon contains exactly one point and every point in a given polygon is closer to its central point than to any other.

Current state	State of 8 neighboring cells	Next state
1	Any states different from those shown below	1
	At each step of the processing 4 templates are rotated 90 degrees counter clockwise	0
0	Any state	0

(a)

Current state	State of 8 neighboring cells	Next state
1	Any states different from those shown below	1
	A) B) At each step of the processing 1 templates group is alternately selected from above and below groups. They are rotated 90 degrees counter clockwise each selected period. C) D)	0
0	Any state	0

(b)

Fig. 4. (a) templates for rotated erosion, (b) templates for skeltonization.

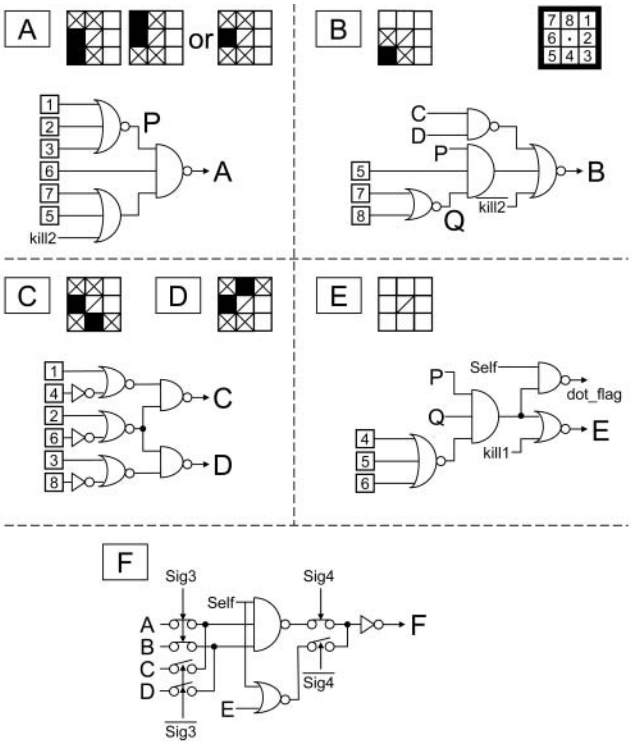


Fig. 6. Logic circuits for template matching circuits.

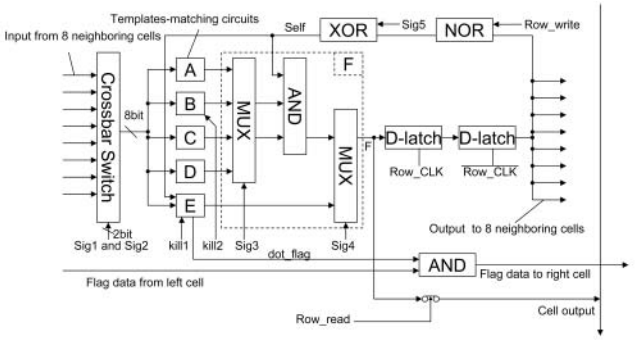


Fig. 5. Cell circuits for rotated template matching.

4. Hardware CA

Figure 5 shows a cell circuit with four subcircuits: i) crossbar switches for changing input signals, ii) logical circuits for template matching, iii) multiplexers for changing the direction of data transfer, and iv) cell-state-memory (D-latch) circuits.

Templates are rotated by shifting inputs from the eight neighboring cells 90° using crossbar switches. By changing sel1 and sel2 each cycle, input signals are rotated each cycle step (**Fig.6**). Logical circuits for template-matching circuits extract dots, rotate erosion and dilation, skeletonize, and generate Voronoi diagram. To reduce noise and increase processing speed, we use erosion and dilation without rotation making the applicable template from the dot extraction template (E). Inputs for five types of template-matching circuit are provided from the crossbar switch and outputs of the other template-matching circuits. Template-matching circuits all operate in parallel and determine the states of the eight neighboring cells. Outputs of template-matching circuits and the feedback signal (self) from cell circuit output are applied to an AND gate. Output (F) of the multiplexer corresponds to the state taken by the cell in the next processing step. Cell states also change in response to clock signals (Row_CLK) applied to cell-state-memory (D-latch) circuits. Multiplexers consist of MOSFET switches for changing operation. Using Row_CLK, Row_read, Row_write, we read and write cell circuit data at each row. Transistors of the cell circuit number 198 with a full customized design.

Figure 7 diagrams the system, which consists of five blocks: i) a CMOS-image sensor array, ii) a 2D cell-circuit array, iii) flag collection circuits, and iv) a controller, and v) a decoder. The CMOS-image sensor array [6] makes a binarized image from an original image using any threshold. After receiving a binarized image from the image sensor array, the cell-circuit array acts as a rotated erosion processor to extract dots of contracted objects and as a dilation processor to reconstruct windows of objects used for image recognition. In the above operations, all cells work synchronously as CA. The controller generates control signals, manages these blocks, and creates feature information on objects from erosion time steps and results of other operations such as skeletonization. Flag collection circuits, which consist of AND gates, determine whether dots exist in each cell circuit.

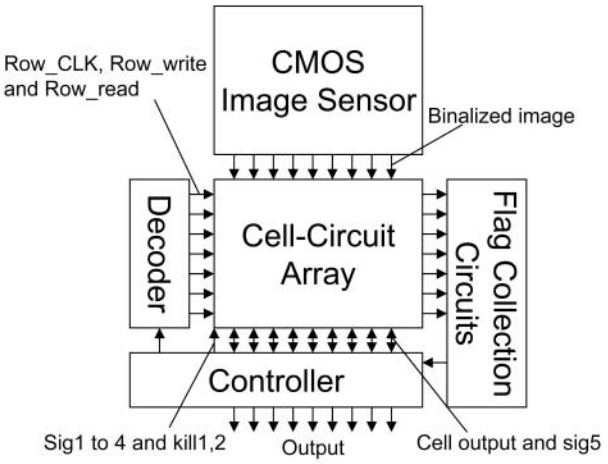


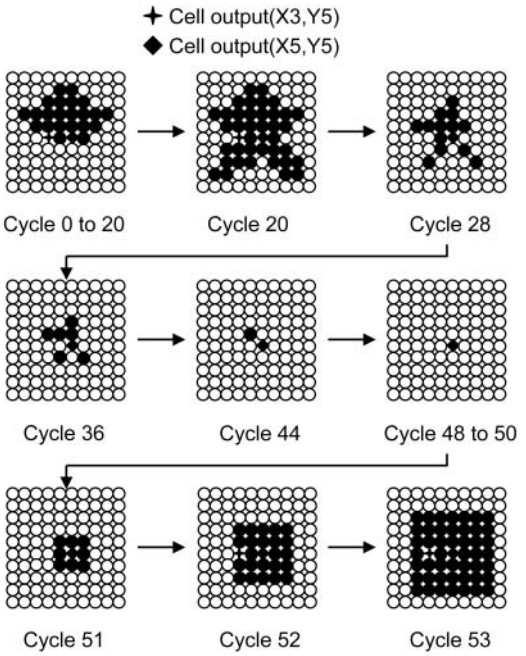
Fig. 7. Block diagram of high-speed image processing that extracts early features of objects in images.

Ishikawa [7] arrayed small general-purpose PE as an example of massive parallel architecture. The above circuitry conducts general-purpose operations for neighboring pixels by repeating 1-bit operations. We assumed that intelligent image sensors are for specialized market use, and designed circuitry on this assumption limiting applications and processing and designing practical templates. Using this circuitry, template matching with many inputs can be done in 1 cycle. For future applications, however, we will use a system that chooses combinations of processing from a single control for programming.

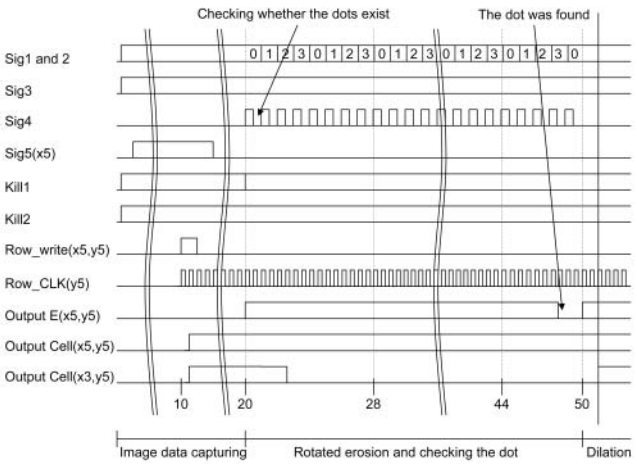
5. Simulation Examples

We built CA LSI by assembling the cell circuits in section 5 and tested their action through simulation. In simulation, cell circuits were arrayed and connected in a matrix configuration. After applying certain initial values to all cells, we observed changes in cell states that were determined from the output of cell circuits. **Fig.8(a)** shows a 10×10 cell array framed by 44 bias cells (having a fixed state) on the array perimeter. To check rotated erosion characteristics, we observed changes in states of cells during each time step. Initial values were applied to each cell – in this case, during data capture (cycle 0 thorough 20) – cells were initialized as shown in cycle 20 of **Fig.8(a)**, and peripheral bias cells were assigned the fixed 0 state). **Fig.8(b)** shows timing charts of control signals and appropriate cell states – locations of cells are indicated in the diagram in **Fig.8(a)**.

The initial pattern was processed first based on erosion. When this was completed, operation was switched to dilation by changing the control signal. Changes in cell states caused by these actions are shown in **Fig.8(a)** (cycle 20 through 53). The initial pattern in cycle 20 is contracted step by step. Dot extraction is completed by cycle 48 and no contraction takes place after that. Upon completion



(a)



(b)

Fig. 8. Example of proposed CA LSI; (a) cell state transition (10×10 cells), and (b) timing chart for proposed CA LSI.

of step 50, operation was switched to dilation, starting pattern growth based on switched functions and modified graphic patterns.

CA LSI speed is restricted by connecting AND gates cell to cell. If we assume a 0.25-μm CMOS process for the proposed circuits, the delay in the minimum-sized AND gate would be 0.11ns. Assuming that CA LSI is constructed using 320×240 cell circuits, the total delay of dot flag transfer in each row is 35.2ns ($0.11\text{ns} \times 320$), so CA operates at 25MHz.

We numerically simulated a 320×240 pixel image by quantizing a natural image (**Fig.9(a)** and **(b)**) and inputting it to the proposed CA core. Simulation was as follows: 1. We transferred the input binary image (**Fig.9(b)**) to the cell circuit array and repeated "rotated erosion" af-

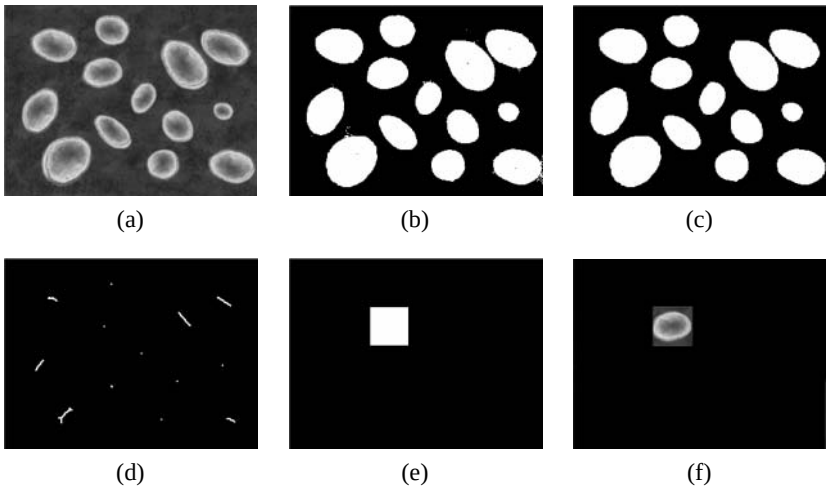


Fig. 9. Object extraction in an image (320×240 pixels); (a) original image, (b) binarized image given to CA LSI, (c) image with noise removed using erosion and dilation without rotation, (d) image contracted by rotated erosion, (e) quadrilateral window, and (f) extracted object.

Table 1. Breakdown of total cycle and total time at 25MHz.

Operation	Cycle per operation	Time (ns)
Quantization and data input to CA-LSI	720 $(= 240 \times 3)$	28800
Noise reduction (dilation and erosion)	12 $(= 6 + 6)$	480
Rotated Erosion, dots-detection and erasing	205 $(= 100 + 100 + 5)$	8200
Non-dots erasing	240	9600
Dilation	25 $(= 100/4)$	1000
Total	1202	48080

ter reducing noise (**Fig.9(c)** and **(d)**) using dilation and erosion without rotation. The number of erosion processes was counted and if dots were found, the peripheral controller stored the number. 2. The number indicating the expected size is checked in the controller. 3. If the number does not match the expected size, the cell-circuit array erases only dots and rotated erosion is repeated. 4. When the number matches the expected size, the cell-circuit array erases everything except dots. 5. A quadrilateral window is generated through dilation until the window expands to the expected size (**Fig.9(e)**). 6. The original image corresponding to the above window is output by the CMOS image sensor (**Fig.9(f)**). The expected window was thus correctly extracted in this operation was 1,202 cycles (48,080ns at 25MHz). **Table 1** breaks down total cycles and total time. Quantization and data input included settling of output circuits of the image sensor, so these operations required three times cycles. In noise reduction, we repeated erosion and dilation 6 times. Simulation was assumed for obtaining an object 45 to 50 pixels in diameter, and we determined cycles of rotated erosion and dots detection. Erasing non dots required sequential operation on all lines.

We simulated skeletonization and computation of the Voronoi diagram (**Fig.10(a)** and **(b)**). As a measure of skeletonization accuracy, we defined the number of noisy branches and how much extracted lines coincided with

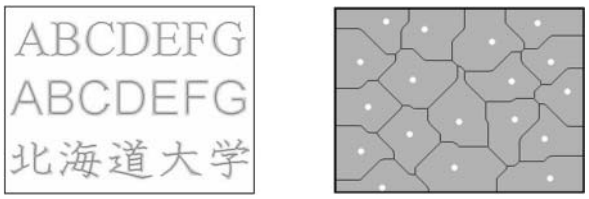


Fig. 10. Simulation results of skeletonization and computation of Voronoi diagram; (a) extracted skeletons of objects and (b) Manhattan-Metric Voronoi diagram.

center lines of original graphic features. Results were different little from existing algorithms [8–12]. For the Voronoi diagram, **Fig.10(b)** shows a Manhattan-Metric algorithm [13–16] because i) the borderlines are generated by rotated erosion edges colliding, and ii) our erosion proceeds in a square.

6. Summary

We have designed CA LSI to extract features of objects from binary images. LSI was configured from a large array of cell circuits operating in parallel, ensuring fast, efficient information extraction. Each cell circuit

in the proposed CA is implemented as a digital circuit, and transistors for each cell circuit numbered 198 for full customized design. If we assume a 0.25-μm CMOS process for the proposed circuits, the total area of each cell circuit is about $30 \times 30\mu m^2$ and image processing with 320×240 cells operates at 25MHz. Among the most important application targets for the proposed CA core are white line extraction and object extraction. Features are conventionally extracted from images sequentially, making it difficult to apply high-speed image processing. The proposed LSI enables high-speed production of efficient features from binary images suitable for image recognition.

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Name:
Masayuki Ikebe

Affiliation:
Associate Professor, Graduate School of Information Science and Technology, Hokkaido University

Address:
Kita 14, Nishi 9, Kita-ku, Sapporo 060-0814, Japan

Brief Biographical History:
2000 Joined Dai Nippon Printing Co., Tokyo, Japan
2004- Associate Professor at Hokkaido University

Main Works:
• M. Ikebe, and Y. Amemiya, "*v*MOS Cellular-automaton circuit for picture processing," in T. Miki Ed., "Brainware: Bio-Inspired Architecture and its Hardware Implementation," Chapter 6, pp. 123-162, World Scientific, Singapore, 2000.

Membership in Learned Societies:
• The Institute of Electronics, Information and Communication Engineers (IEICE)

Name:
Tetsuya Asai

Affiliation:
Associate Professor, Graduate School of Information Science and Technology, Hokkaido University

Address:
Kita 14, Nishi 9, Kita-ku, Sapporo 060-0814, Japan

Brief Biographical History:
1999- Research Associate at Hokkaido University
2001- Associate Professor at Hokkaido University

Main Works:
• "Towards reaction-diffusion computing devices based on minority-carrier transport in semiconductors," Chaos, Solitons & Fractals, Vol.20, No.4, pp. 863-876, 2004.

Membership in Learned Societies:
• The Institute of Electrical and Electronics Engineers (IEEE)
• Japanese Neural Network Society (JNNS)
• The Japan Society of Applied Physics (JSAP)