サブスレッショルド VLSI ニューロン回路による ノイズシェーピング パルス密度変調

Noise shaping pulse-density modulation in inhibitory neural networks with subthreshold VLSI neuron circuits

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Abstract—An inhibitory network model that performs noise-shaping pulse-density modulation [1] was implemented with subthreshold analog MOS circuits, aiming at the development of ultralow-power $\Sigma\Delta$ -type AD converters. Through circuit simulations, we evaluate the effects of the noise shaping produced by the network circuit.

Keywords—VLSI, pulse density modulation, noise shaping, chaotic neural networks

1 Model and Method

The network consists of N integrate-and-fire neurons (IFNs) with all-to-all inhibitory connections [1]. A common analog input is given to all the IFNs, while 1-bit digital output is given by the sum of firing events of the IFNs. Static and dynamic noises are introduced into the analog input and the reset potential of IFNs after each firing, respectively. Since the wiring complexity of the network; i.e., $O(N^2)$ in [1], can be reduced to O(N) by introducing a global inhibitor [2], we designed a network circuit as shown in Fig. 1. The static and dynamic noises are given to the circuit as device mismatches of current sources (I_i) and external random (Poisson) spikes, respectively.

Similarly, instead of applying dynamic noises to the circuits externally, we tried to use neuron's intrinsic noises by using chaotic neuron units based on 3variable Lotka-Volterra system [3]. The network dynamics are given by

$$\begin{aligned} x_{1,i}^{\cdot} &= (h - x_{1,i} - c \ x_{2,i} - k \ y_i) x_{1,i}, \\ x_{2,i}^{\cdot} &= (a \ h - b \ x_{1,i} - x_{2,i} - y_i) x_{2,i}, \\ \dot{y_i} &= (-r \ h + \alpha \ k x_{1,i} + \beta \ x_{2,i}) y_i, \\ h &= I_i - \frac{w}{N} \sum_{i=1}^N x_{1,i}, \end{aligned}$$

where w represents the weight strength and h the input to neurons (cf. [3] and [4] for the rest parameters).



(b) inhibitory neural network with three neuronsFig. 1 Circuit structure of neuron and network.

2 Simulation Results

Figure 2 shows simulation results of a network circuit shown in Fig. 1 (N = 3, $I_i = [1:1.2]$ nA, amplitudes of the Poisson spikes: 1 nA, the width: 10 μ s, the mean and variation: 5000). When IFNs were uncoupled (K = 0: mirror rate of a pMOS current mirror in the network circuit), inter-spike intervals (ISIs) of the output spike trains looked almost random (upper left in Fig. 2), whereas they were almost uniform when the IFNs were coupled with K = 3 (upper right in Fig. 2). Figure 2 (bottom) shows a histogram of ISIs for K = 0 and 3. As expected in [1], the coupled network produced a Gaussian-like distribution of ISIs, while the uncoupled one had a broad distribution. Figure 3 shows the power spectrum of the coupled and uncoupled network with sinusoidal inputs $(I_i = I_0 + A\sin(2\pi ft), I_0 = 1 \text{ nA}, A = 50 \text{ pA}, f = 100$ Hz). A measured SNR of the uncoupled network was 10.2 dB, while that of the coupled one was 18.1 dB, which indicated that the network reduced the noises significantly, although noise-sensitive (but low-power)



Fig. 2 Output spikes of the network circuit (top) and the histogram of ISIs (bottom)



Fig. 3 Power spectrum of sum of output spikes.

subthreshold CMOS devices were used in the circuit. The cutoff frequency was able to be increased by decreasing capacitances or by increasing the magnitudes of input currents.

A raster plot of the Lotka-Volterra chaotic neural network is shown in Fig. 4 (N = 10, w = 4, $I_i = 0.5 \ i/N + A \sin(2\pi f t), A = 0.05, \text{ and } f = 0.1).$ The top (\sum) represents the sum of x_1 's. Since the sum inhibits all the neurons, the number of active neurons decreased as the weight strength (w) increased. Figure 5 shows a histogram of ISIs for w = 0 and 4 (A = 0). In contrast to the result of Fig. 2, ISIs of the coupled chaotic network was broadly distributed compared with that of the uncoupled network. The power-spectrum density was calculated for both uncoupled and coupled chaotic networks. The background noise was attenuated as a whole by the inhibitory coupling, however, the signal power was enhanced, as shown in Fig. 6. This result encourage us to develop a low-power AD converter VLSI because the 3-variable Lotka-Volterra circuit has already been developed and implemented on subthreshold analog VL-SIs by the authors [4].



Fig. 4 Raster plot of chaotic neural network.



Fig. 6 Power spectrum of sum of output spikes.

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