A 300 nW, 7 ppm/°C CMOS Voltage Reference Circuit based on Subthreshold MOSFETs

Ken Ueno†, Tetsuya Hirose‡, Tetsuya Asai†, and Yoshihito Amemiya†

†Department of Electrical Engineering Hokkaido University, Sapporo 060-0814, Japan
‡Department of Electrical and Electronics Engineering, Kobe University, Kobe 657-8501, Japan
E-mail: k_ueno@sapiens-ei.eng.hokudai.ac.jp

***Abstract*— An ultra-low power CMOS voltage reference circuit has been fabricated in a 0.35-μm standard CMOS process. The circuit generates a reference voltage based on threshold voltage of a MOSFET at absolute zero temperature. Theoretical analyses and experimental results showed that the circuit generates a quite stable reference voltage of 745 mV on average. The temperature coefficient and line sensitivity of the circuit were 7 ppm/°C and 20 ppm/V, respectively. The power supply rejection ratio (PSRR) was –45 dB at 100 Hz. The circuit consists of subthreshold MOSFETs with a low-power dissipation of 0.3 μW or less and a 1.5-V power supply. Because the circuit generates a reference voltage based on threshold voltage of a MOSFET in an LSI chip, it can be used as an on-chip process monitoring circuit and as a part of the on-chip process compensation circuit systems.**

I. Introduction

One of the promising areas of research in microelectronics is the development of ultra-low power LSIs that operate in the subthreshold region of MOSFETs (for our previous work, see [1]). Such LSIs will be suitable for use in mobile devices, implantable medical devices, smart sensor networks, and so on. To step toward such LSIs, we first need to develop an ultra-low power voltage reference circuit that can operate at several tens of nanoamperes or lower. Many low-power CMOS voltage reference circuits have been reported in recent works [2]-[4]. However, these circuits are unsuitable for use in ultra-low power LSIs because of their large power consumption of several microwatts or more, and poor temperature or supply voltage characteristics of the output voltage.

To solve these problems, we developed a temperature and supply voltage compensated CMOS voltage reference circuit that operates with a sub-microwatts power dissipation [5]. The circuit generates a reference voltage based on threshold voltage of a MOSFET in an LSI chip with little temperature and supply dependence. The reference voltage can be used for an on-chip process monitoring and therefore for a part of the on-chip process compensation systems. The following sections describe the circuit in detail.

II. Circuit Configuration

Figure 1 shows voltage reference circuit we developed. The circuit consists of a current source subcircuit, a bias-voltage subcircuit, and an operational amplifier. The current source subcircuit is based on a β multiplier self-biasing circuit and uses a MOS resistor $\mathrm{M_{R1}}$ instead of an ordinary passive resistor. The bias-voltage subcircuit accepts the current through pMOS current mirrors and generates the reference voltage. The bias-voltage subcircuit consists of a diode-connected transistor ($\mathrm{M_4}$) and two differential pairs ($\mathrm{M_3}$-$\mathrm{M_6}$, $\mathrm{M_5}$-$\mathrm{M_7}$) and is based on the translinear principle. We operate all MOSFETs in the subthreshold region except for MOS resistor $\mathrm{M_{R1}}$, which is operated in the strong-inversion and deep triode region. An

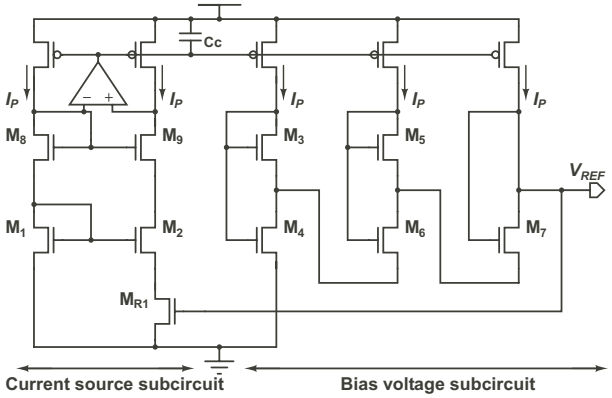

Fig. 1. Schematic of proposed voltage reference circuit.

operational amplifier and nMOS current mirror ($\mathrm{M_8}$, $\mathrm{M_9}$) are used to improve the power supply rejection ratio (PSRR) and line sensitivity of the circuit.

The subthreshold MOS current I_D can be expressed as $I_D = KI_0 \exp\left((V_{GS}-V_{TH})/\eta V_T\right)$, where K is the aspect ratio (=W/L) of transistors, $I_0(=\beta(\eta-1)V_T^2)$ is the process-dependent parameter, $V_T(=k_BT/q)$ is the thermal voltage, V_{TH} is the threshold voltage of a MOSFET, and η is the subthreshold slope factor. In the circuit in Fig.1, the current I_P flowing in the circuit is determined by the ratio of $\mathrm{M_1}$ and $\mathrm{M_2}$ and the resistance of MOS resistor $\mathrm{M_{R1}}$, and it is given by I_P=$\beta(V_{REF}-V_{TH})\eta V_T \ln(K_2/K_1)$, where β is the current gain factor. In the bias-voltage subcircuit, gate-source voltages of transistors (V_{GS3} through V_{GS7}) form a closed loop with the reference voltage V_{REF}, so we find that

$$\begin{aligned} V_{REF} &= V_{GS4}-V_{GS3}+V_{GS6}-V_{GS5}+V_{GS7} \\ &= V_{GS4}+\eta V_T \ln\left(\frac{2K_3K_5}{K_6K_7}\right). \end{aligned} \tag{1}$$

The reference voltage can be expressed by the sum of gate-source voltage $V_{GS4}(=V_{TH}+\eta V_T \ln(3I_P/K_4I_0))$ and thermal voltage V_T scaled by the transistor sizes. Because these voltages have negative and positive temperature dependence, respectively, a constant voltage reference circuit with little temperature dependence can be constructed by adjusting the size of the transistors. Note that the threshold voltages of the transistors in the source-coupled pairs ($\mathrm{M_3}$-$\mathrm{M_6}$, $\mathrm{M_5}$-$\mathrm{M_7}$) are canceled each other by source-coupled circuit configuration.

The temperature dependence of the threshold voltage can be given by $V_{TH}=V_{TH0}-\kappa T$, where V_{TH0} is the threshold voltage at absolute zero, and κ is the temperature coefficient of the threshold voltage. On the condition where $V_{REF}-V_{TH0} \ll \kappa T$, temperature coefficient of reference voltage

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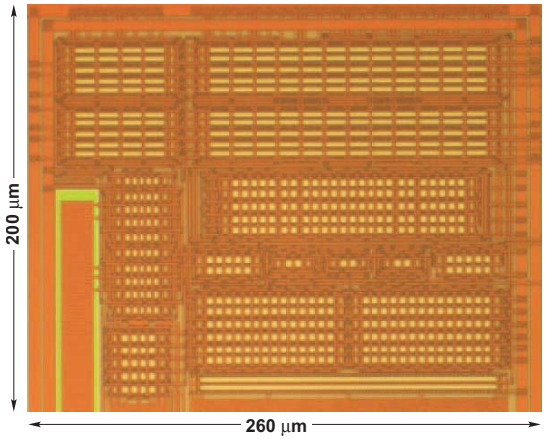

Fig. 2. Chip micrograph. Area was 0.052 mm^2.

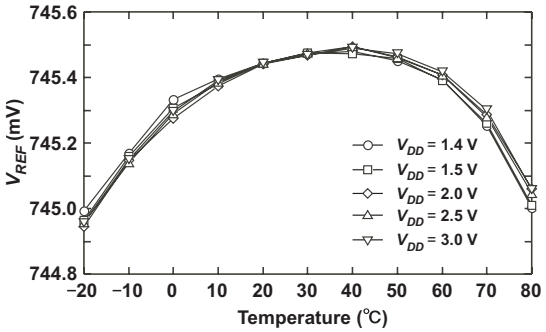

Fig. 3. Measured results of output voltage V_{REF} as a function of temperature with different power supply. Temperature coefficient and line sensitivity were 7 ppm/℃ and 20 ppm/V, respectively.

V_{REF} in Eq.(1) is given by

$$\frac{dV_{REF}}{dT} = -\kappa + \frac{\eta k_B}{q} \ln\left\{ \frac{6q\eta\kappa}{k_B(\eta-1)} \frac{K_{R1}K_3K_5}{K_4K_6K_7} \ln\left(\frac{K_2}{K_1}\right)\right\}. \quad (2)$$

We can obtain a constant voltage with a zero temperature coefficient by setting the aspect ratios such that $dV_{REF}/dT = 0$ in Eq.(2). From Eqs.(1) and (2), the output voltage V_{REF} is given by

$$V_{REF} = V_{TH0}. \quad (3)$$

Therefore, the circuit generates the threshold voltage of MOSFET (M_4) at absolute zero temperature.

III. Experimental Results

We fabricated a prototype chip using a 0.35-μm, 2-poly, 4-metal standard CMOS process. Figure 2 shows a chip micrograph of our prototype chip. The area was 0.052 mm^2. Figure 3 shows measured output voltage V_{REF} as a function of temperature from –20 to 80℃ with a different power supply V_{DD}: 1.4, 1.5, 2, 2.5, and 3 V. The average output voltage was about 745 mV. The temperature variation and temperature coefficient were 0.48 mV and 7 ppm/℃, respectively. The circuit operated correctly with a power supply more than 1.4 V, and the line sensitivity was 20 ppm/V in the supply range of 1.4 to 3 V. A constant reference voltage with quite little temperature and power supply dependence was obtained. Figure 4-(A) shows the power supply rejection ratio (PSRR) at room temperature with 1 pF on-chip filtering capacitor and at a 2-V power supply. The PSRR was –45 dB at 100 Hz. Figure 4-(B) shows the current I_P as a function of temperature with a different power supply. The current I_P was extremely low, about 36 nA at room temperature, and the maximum current

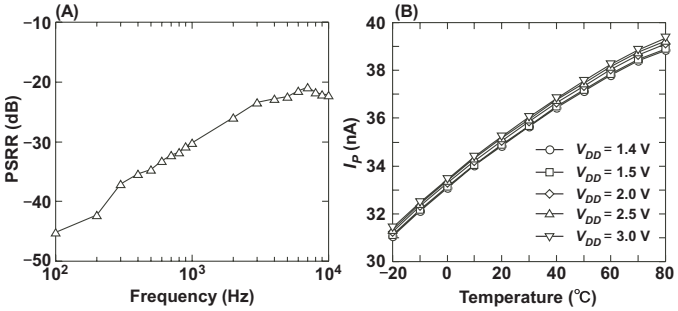

Fig. 4. Measured results of (A) PSRR at room temperature with 1 pF filtering capacitor and with 2-V power supply, and (B) output current I_P as a function of temperature with different power supply.

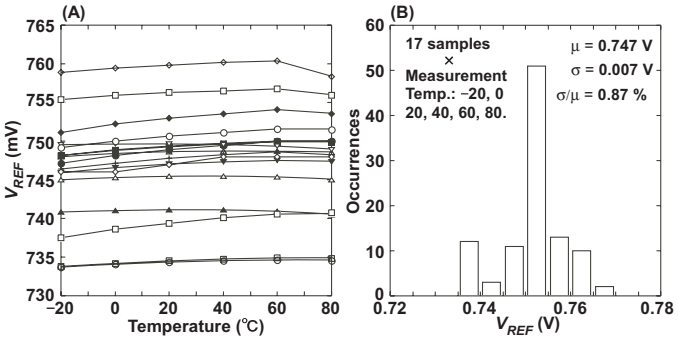

Fig. 5. Measured results of output voltage. (A) temperature dependence in 17 samples, and (B) distribution in 17 samples with different temperatures. Temperature coefficient was less than 45 ppm/℃.

TABLE I
Comparison of Reported CMOS Voltage Reference Circuits

	This work	[2]	[3]	[4]
Process	0.35-μm	0.35-μm	0.6-μm	1.2-μm
Temp.	–20 - 80℃	0 - 80℃	0 - 100℃	–25 - 125℃
V_{DD}	1.4 - 3 V	0.9 - 4 V	1.4 - 3 V	1.2 V
$\overline{V_{REF}}$	745 mV	670 mV	309.3 mV	295 mV
Power	0.3 μW	0.036 μW	29.1 μW	4.3 μW
TC	7 ppm/℃	10 ppm/℃	36.9 ppm/℃	119 ppm/℃
Line sens.	20 ppm/V	2700 ppm/V	800 ppm/V	N.A.
PSRR	–45 dB (@100 Hz)	–47 dB (@100 Hz)	–47 dB (@100 Hz)	N.A.
Chip area	0.052 mm^2	0.045 mm^2	0.055 mm^2	0.23 mm^2

I_P was 39 nA at 80℃. The total power dissipation of the circuit was 0.3 μW at room temperature with a 1.5-V power supply. Figure 5-(A) shows measured output voltage V_{REF} with 17 samples as a function of temperature. The variation of the output voltage was 25 mV, and the temperature coefficients were within 45 ppm/℃, in our samples. Figure 5-(B) shows the distribution of the output voltage V_{REF} in 17 samples at different temperatures: –20, 0, 20, 40, 60, and 80℃. The coefficient of variation (σ/μ) was 0.87% in this measurement.

Table I summarizes the performance of the circuits and compares the performance of reported low-power CMOS voltage reference circuits [2]-[4]. Compared to the other CMOS voltage reference circuits, the proposed circuit shows the best temperature coefficient and line sensitivity performance.

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