A 46-ppm/℃ Temperature and Process Compensated Current Reference with On-Chip Threshold Voltage Monitoring Circuit

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Abstract— **A CMOS current reference circuit has been developed in 0.35-μm CMOS process. The circuit consists of a voltage reference circuit, a noninverting amplifier, and an output MOS transistor. The circuit generates a reference current independent of temperature and process variations. Temperature- and process-compensation were achieved by utilizing the zero temperature coefficient bias point of a MOSFET. Theoretical analyses and experimental results showed that the circuit generates a quite stable reference current of 18.4 μA on average. The temperature coefficient, load sensitivity, and process sensitivity (σ/μ) of the circuit were 46-ppm/℃, 1.5%/V, and 4.4%, respectively. The circuit can be used as a current reference circuit for high precision analog circuit systems.**

I. Introduction

Current reference circuits are one of the important building blocks for analog and mixed-signal circuit systems in microelectronics. The circuits generate a reference current for numerous analog circuits such as operational amplifiers, analog buffers, oscillators, AD/DA converters, and so on. Because performances of these circuits are determined mainly by their bias currents, a current reference circuit tolerant to process, supply voltage, and temperature (PVT) variations is required to ensure circuit operation that is stable and highly precise.

Several current reference circuits have been reported in recent works [1] - [6]. In [1] and [3], the zero temperature coefficient (ZTC) bias point of a MOSFET was used to generate a temperature compensated current. The temperature characteristics of the ZTC bias point were analyzed on the assumption that the temperature exponent of the carrier mobility m [7] and the carrier mobility degradation factor α [8] are close or equal. However, these values of m and α are not equal in general and change in accordance with the CMOS process technology. Moreover, because the ZTC bias point depends on the threshold voltage of a MOSFET, the performance of the reference current will be degraded with the threshold voltage variation. Therefore, a temperature and process compensated current reference circuit cannot be obtained with these reference circuits.

To solve these problems, in this paper, we propose a CMOS current reference circuit tolerant to temperature and process variations. The circuit consists of an on-chip threshold voltage monitoring circuit [9], a noninverting voltage amplifier, and an output transistor. Temperature compensation is performed by combining the threshold voltage monitoring circuit, the noninverting amplifier, and the ZTC characteristics of a MOSFET. The variation in the threshold voltage is compensated by using an on-chip threshold voltage monitoring circuit. The circuit generates a temperature- and process-compensated reference current. This paper is organized as follows: the temperature characteristics of the drain current and the ZTC bias point are described in Sect. II, proposed circuit configuration and simulation results are described in Sect. III, and Sect. IV, respectively, and the measured results and concluding remarks are presented in Sect. V. Note that a set of 0.35-μm standard CMOS process parameters was used in this work.

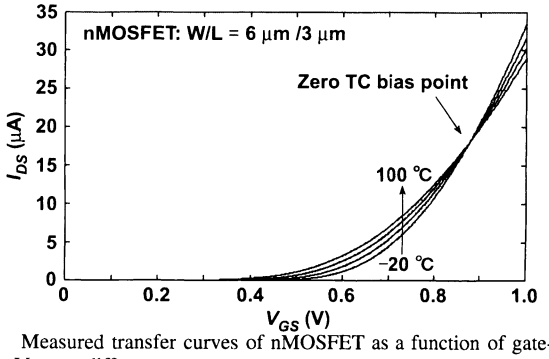

Fig. 1. Measured transfer curves of nMOSFET as a function of gate-source voltage V_{GS} at different temperatures.

II. Temperature Characteristics

Figure 1 shows the measured transfer curves of nMOSFET at different temperatures from –20℃ to 100℃. The ZTC bias point of the drain current can be found in the gate-source voltage of 0.87 V. The temperature characteristics of the ZTC bias point of a MOSFET can be analyzed as follows.

The drain current I_{DS} of a MOSFET operated in the strong inversion and saturation region is given by

$$I_{DS} = K(V_{BIAS} - V_{TH})^{\alpha}, \quad (1)$$

where $K(\sim(W/L)\mu C_{OX})$ is the current gain factor, V_{BIAS} is the gate-source voltage, μ is the carrier mobility, C_{OX} is the gate-oxide capacitance, V_{TH} is the threshold voltage, and α is the mobility degradation factor [8]. The temperature characteristics of the threshold voltage and the mobility can be given by $V_{TH} = V_{TH0} - \kappa T$, $\mu = \mu_0(T_0)\,(T_0/T)^m$, respectively, where V_{TH0} is the threshold voltage at absolute zero temperature, κ is the temperature coefficient of the threshold voltage, $\mu(T_0)$

is the carrier mobility at room temperature T_0, and m is the temperature exponent of the mobility. For a fixed gate-source voltage V_{BIAS} with temperature, the temperature coefficient TC_I of the current is given by

$$TC_I = \frac{1}{I_{DS}}\frac{dI_{DS}}{dT} = \frac{1}{\mu}\frac{d\mu}{dT} + \frac{1}{(V_{BIAS}-V_{TH})^{\alpha}}\frac{d(V_{BIAS}-V_{TH})^{\alpha}}{dT} = -\frac{m}{T} + \frac{\alpha\kappa}{V_{BIAS}-V_{TH}}. \quad (2)$$

Therefore, the condition for a zero temperature coefficient of the current ($TC_I = 0$) can be given by

$$V_{BIAS} = V_{TH0} + \left(\frac{\alpha}{m} - 1\right)\kappa T. \quad (3)$$

Because the bias voltage V_{BIAS} is a fixed voltage with temperature (Eq. (2) is derived from the fixed gate-source bias voltage condition), the value of α/m in Eq. (3) should be equal to 1. Therefore, V_{BIAS} and TC_I can be rewritten as

$$V_{BIAS} = V_{TH0}, \quad TC_I = \frac{\alpha - m}{T} = 0. \quad (4)$$

Equation (4) shows that temperature compensated current can be obtained if two conditions are satisfied: if the bias voltage for the output transistor is V_{TH0} and if the value of α/m is equal to 1. However, the temperature exponent of the mobility m and the carrier mobility degradation factor α generally are not equal. In standard CMOS process parameters, these values of m and α are 1.5 and 2, respectively. Therefore, the output current increases as the temperature increases because $(\alpha - m)$ is greater than 0.

Considering the above discussion from another point of view, by using the threshold voltage at absolute zero temperature V_{TH0} as a bias voltage for the output transistor, a current that has a temperature coefficient of $TC_I = (\alpha - m)/T$ can be obtained. The temperature coefficient of the current will never be zero with the bias voltage of V_{TH0}. However, from Eq. (2), a larger voltage than V_{TH0} can modify the temperature coefficient of the output current. From this concept, a current reference circuit was developed. The details of the circuit are as follows.

III. Circuit Configuration

Figure 2 shows current reference circuit we proposed. The circuit consists of a voltage reference circuit [9], a noninverting voltage amplifier, and an output transistor. The voltage reference circuit generates a constant reference voltage V_{REF} that is based on the threshold voltage of a MOSFET at absolute zero temperature in an LSI chip. The noninverting voltage amplifier is used to generate an appropriate bias voltage V_{OUT}, which is larger than V_{REF}, for the output transistor. The output transistor accepts the voltage V_{OUT} and generates reference current I_{REF} independent of temperature and process variation.

A. Threshold Voltage Monitoring Circuit

The left of Fig. 2 shows the voltage reference circuit we used [9]. The circuit consists of a current source subcircuit, a bias-voltage subcircuit, and an operational amplifier, and generates a reference voltage that is the threshold voltage of

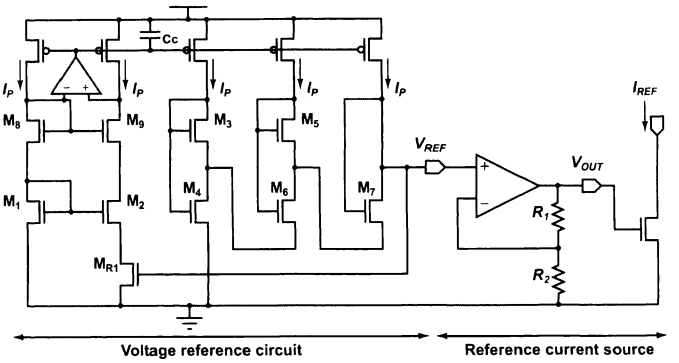

Fig. 2. Proposed current reference circuit. Voltage reference circuit generates a voltage based on the threshold voltage of a MOSFET.

transistor M_4 at absolute zero temperature. All MOSFETs are operated in the subthreshold region except for MOS resistor M_{R1}, which is operated in the strong-inversion and deep triode region. In the bias-voltage subcircuit, the gate-source voltages of transistors (V_{GS3} through V_{GS7}) form a closed loop with the reference voltage V_{REF}, so we find that

$$V_{REF} = V_{GS4} - V_{GS3} + V_{GS6} - V_{GS5} + V_{GS7} = V_{GS4} + \eta V_T \ln\left(\frac{2S_3S_5}{S_6S_7}\right), \quad (5)$$

where S is the aspect ratio ($=W/L$) of the transistors. The reference voltage can be expressed by the sum of the gate-source voltage $V_{GS4}(= V_{TH} + \eta V_T \ln(3I_P/S_4I_0))$ and thermal voltage V_T scaled by the transistor sizes, where $I_0(= \beta(\eta-1)V_T^2)$ is the process-dependent parameter. Because these voltages in Eq. (5) have negative and positive temperature dependence, respectively, a constant voltage reference circuit with little temperature dependence can be constructed by adjusting the size of the transistors. On the condition where $V_{REF} - V_{TH0} \ll \kappa T$ and $\eta V_T \ll \kappa T$, the temperature dependence of the reference voltage V_{REF} in Eq. (5) is rewritten as

$$\frac{dV_{REF}}{dT} = -\kappa + \frac{\eta k_B}{q}\ln\left\{\frac{6q\eta\kappa}{k_B(\eta-1)}\frac{S_{R1}S_3S_5}{S_4S_6S_7}\ln\left(\frac{S_2}{S_1}\right)\right\}, \quad (6)$$

where k_B is the Boltzmann constant. By setting the aspect ratios S such that Eq. (6) is equal to 0, a constant reference voltage of a zero temperature coefficient can be obtained. From Eqs. (5) and (6), the output voltage V_{REF} is given by

$$V_{REF} = V_{TH0}. \quad (7)$$

Therefore, the circuit generates a threshold voltage of a MOSFET at absolute zero temperature. Because the output voltage of V_{REF} depends on the threshold voltage of a MOSFET (M_4) in an LSI chip, the output voltage shows linear dependence with die-to-die threshold voltage variation and can be used as an on-chip process monitoring signal.

B. Operation of Current Reference

To generate an appropriate bias voltage for the output transistor, the noninverting voltage amplifier is used. The output voltage of the noninverting amplifier V_{OUT} can be expressed as

$$V_{OUT} = V_{TH0}\left(1 + \frac{R_1}{R_2}\right). \quad (8)$$

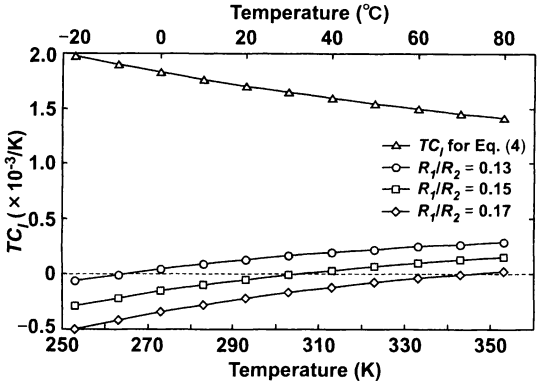

Fig. 3. Calculated TC_I of the proposed current reference circuit.

The output transistor accepts the voltage V_{OUT} and generates a reference current. The reference current I_{REF} is given by

$$I_{REF} = K\left\{V_{TH0}\left(1+\frac{R_1}{R_2}\right) - V_{TH}\right\}^{\alpha}. \tag{9}$$

The TC_I of the current in Eq. (9) is given by

$$TC_I = -\frac{m}{T} + \frac{\alpha\kappa}{V_{TH0}\left(1+\frac{R_1}{R_2}\right) - V_{TH}}. \tag{10}$$

Therefore, the condition for a zero temperature coefficient ($TC_I = 0$) can be written as

$$\frac{R_1}{R_2} = \left(\frac{\alpha}{m} - 1\right)\frac{\kappa T}{V_{TH0}}. \tag{11}$$

Equation (11) shows that the ratio of the resistors can be designed so that TC_I is equal to 0 at room temperature. Figure 3 shows the calculated TC_I as a function of temperature with the ratio of resistors as a parameter. A zero TC_I can be obtained at $R_1/R_2 = 0.15$ at room temperature. The TC_I for Eq. (4) is also depicted for comparison. This way, we can obtain a zero temperature coefficient current by setting the appropriate resistor ratio R_1/R_2.

Next, we discuss in detail the effect of the process variation on the output reference current. From Eq. (9), the process variation of the current I_{REF} can be given by

$$\frac{\Delta I_{REF}}{I_{REF}} = \frac{1}{I_{REF}}\left(\frac{\partial I_{REF}}{\partial \mu}\Delta\mu + \frac{\partial I_{REF}}{\partial V_{TH0}}\Delta V_{TH0} + \frac{\partial I_{REF}}{\partial V_{TH}}\Delta V_{TH} + \frac{\partial I_{REF}}{\partial (R_1/R_2)}\Delta(R_1/R_2)\right). \tag{12}$$

Because the variation in the output voltage ΔV_{TH0} in the threshold voltage monitoring circuit is equal to the variation in the threshold voltage ΔV_{TH} of a transistor in an LSI ($\Delta V_{TH0} = \Delta V_{TH}$) and the variation in the resistor ratio is small [7], the process variation in the current in Eq. (12) can be rewritten as

$$\frac{\Delta I_{REF}}{I_{REF}} = \frac{\Delta\mu}{\mu}. \tag{13}$$

Therefore, we can obtain a reference current that is independent of the threshold voltage variation. The variation in the mobility still exist in Eq. (13), but it is small enough compared to that of the threshold voltage [7].

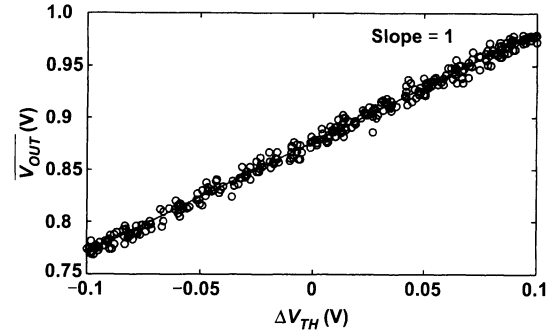

Fig. 4. Scatter plot of the output voltage in the noninverting amplifier as a function of the D2D threshold voltage variation ΔV_{TH} from 300-point Monte Carlo simulations. The output voltage shows a linear dependence on the variation of the threshold voltage $\left(\Delta\overline{V_{OUT}}/\Delta V_{TH} \approx 1\right)$.

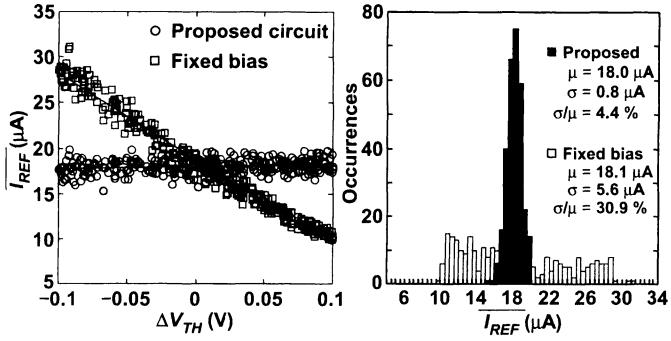

Fig. 5. (a) Scatter plots of the currents as a function of the D2D threshold voltage variation ΔV_{TH} from 300-point Monte Carlo simulations. (b) Distribution of the output reference currents.

IV. Simulation Results

We confirmed the operation of the circuit by a SPICE simulation. The supply voltage of the circuit and the drain-source voltage of the output transistor were set to 1.5 V and 1 V, respectively. To verify the stability of the circuit operation with process variations, Monte Carlo simulations assuming both die-to-die (D2D) variations (the parameters were varied with a uniform distribution: e.g., $-0.1\ \text{V} < \Delta V_{TH} < 0.1\ \text{V}$) and within-die (WID) mismatch variations (the parameters were varied with a Gaussian distribution: e.g., $\sigma_{V_{TH}} = A_{V_{TH}}/\sqrt{LW}$) in all MOSFETs and poly resistors [10]–[12] were performed by using the parameters provided by the manufacturer. In this work, larger transistor sizes were used so that the WID variation could be ignored. To evaluate the process sensitivity, currents generated by the proposed circuit and the fixed bias (V_{GS}=880 mV) were examined.

Figure 4 shows a scatter plot of the average output voltage $\overline{V_{OUT}}$ of the noninverting amplifier in the temperature range of –20 to 80℃ as a function of the D2D variation in the threshold voltage ΔV_{TH}. The output voltage shows a linear dependence on the D2D threshold voltage variation (Slope = 1), because the circuit monitors the threshold voltage of a MOSFET in an LSI chip as shown in Eq. (7). Figure 5 (a) shows a scatter plot of the average reference currents $\overline{I_{REF}}$ generated by the proposed circuit and the fixed bias voltage. The output current with the fixed bias voltage changes broadly with process variation, while the output current with the proposed circuit shows little dependence on the D2D

TABLE I

COMPARISON OF REPORTED CMOS CURRENT REFERENCE CIRCUITS

	This work	Serrano [2]	Bendali [3]	Lee [4]	Sansen [5]	Pappu [6]
Process	0.35-μm, CMOS	0.5-μm, CMOS	0.18-μm, CMOS	2-μm, CMOS	3-μm, CMOS	0.18-μm, BiCMOS
Temperature range	–20 - 80 ℃	0 - 80 ℃	0 - 100 ℃	0 - 75 ℃	0 - 80 ℃	N.A.
V_{DD}	1.4 - 3 V	$\geq$ 2.3 V	1 V	N.A.	$\geq$ 3.5 V	N.A.
$\overline{I_{REF}}$	18.4 μA	16 - 50 μA	144 μA	0.287 μA	0.774 μA	200 μA
Process sensitivity(σ/μ)	4.4 % (M.C. Sim.)	N.A.	N.A.	N.A.	2.5 % (90 samples)	4 % (40 samples)
TC	46 ppm/℃	116 ppm/℃	185 ppm/℃	226 ppm/℃	375 ppm/℃	N.A.
Load sensitivity	1.5%/V	$\leq$ 1%/V	N.A.	N.A.	0.04%/V	N.A.

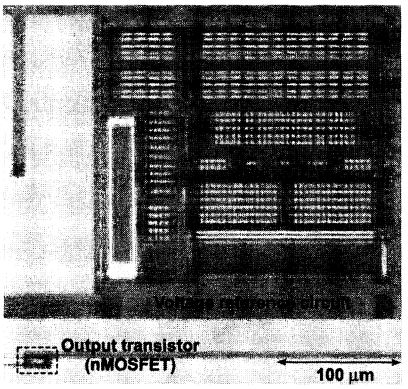

Fig. 6. Chip micrograph of the voltage reference circuit and output transistor. The noninverting amplifier consisting of the operational amplifier and resistors were implemented as off-chip components.

threshold voltage variation. This is because the variation in the threshold voltage directly affects the output current when it is biased with fixed voltage, but the variation in the threshold voltage can be canceled between the output voltage of the threshold voltage monitoring circuit and the output transistor as shown in Eq. (13). Figure 5 (b) shows the distribution of the average output current $\overline{I_{REF}}$. The average current $\overline{I_{REF}}$ was about 18 μA. The effect of the threshold voltage variation ($\Delta V_{TH} = \pm 0.1$ V) on the output reference current can be suppressed within 0.8 μA. The process sensitivity (σ/μ) in 300 runs was 4.4%, and was improved about 85% by using the proposed circuit, compared to the process sensitivity of the fixed bias transistor.

V. EXPERIMENTAL RESULTS

We fabricated a prototype chip with a 0.35-μm, 2-poly, 4-metal standard CMOS process. For flexibility, the noninverting amplifier consisting of the operational amplifier (National Semiconductor: LMC6482) and resistors (metal-film resistor) were implemented as off-chip components. Figure 6 shows a chip micrograph of the voltage reference circuit and the output transistor. The ratio of the resistors (R_1/R_2) was set at 0.18 in this design.

Figure 7 shows the measured reference current I_{REF} as a function of temperature from –20 to 80℃. An almost constant reference current can be obtained. The average current $\overline{I_{REF}}$ was about 18.45 μA. The temperature variation and temperature coefficient of the current were 0.085 μA and 46 ppm/℃, respectively. The load sensitivity was 1.5%/V in the supply range of 1.4 to 3 V. A constant reference current with little

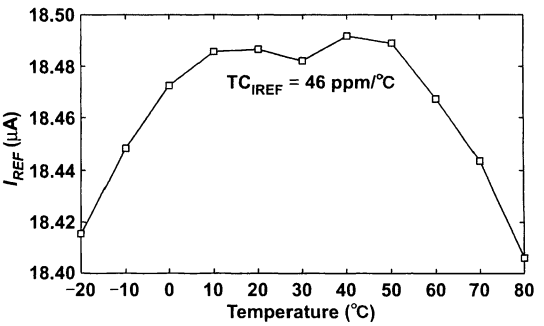

Fig. 7. Measured reference current I_{REF} as a function of temperature.

temperature dependence can be obtained.

Table I summarizes and compares the performances of the proposed circuits and reported CMOS current reference circuits [2]- [6]. The proposed circuit showed the best temperature coefficient performance compared to other CMOS current reference circuits. We are now designing a fully on-chip circuit configuration including resistors and an operational amplifier.

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