A 0.02-to-2-MHz Tunable Clock Reference Circuit for Intermittent Pulse Generators

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ABSTRACT

An ultra-low power clock reference generator has been developed using a 0.35-μm CMOS parameters. The circuit is based on a simple frequency-locked loop technique with no inductors, quartz resonators, and MEMS oscillators. Theoretical analyses and measurement results showed that the clock frequency could be controlled over a frequency range of 20 kHz - 2 MHz. The circuit showed a temperature coefficient of 170 ppm/℃, a line regulation of 1%/V, and a power dissipation of 3 μW, when operated at 200 kHz. A process sensitivity (σ/μ) was 5% without calibration technique. The proposed clock generator can be used as a reference clock for intermittent operation for use in subthreshold-operated, power-aware LSIs.

Keywords: *CMOS, Reference clock, Frequency-locked loop, Ultra-low power, Power-aware*

1. Introduction

The development of ultra-low power LSIs is one of the promising research areas in microelectronics. These LSIs will be useful for use in power-aware LSI applications such as smart sensor networks, portable mobile devices, and implantable medical devices [1], and they have to operate for a long time with limited energy resources such as microbatteries or energy-scavenging power sources [2]. As a step toward designing such LSIs, we are now developing a smart sensor device as shown in Fig. 1. The device consists of sensors [3]-[4], AD/DA converters, digital signal processors, memories, reference circuits [5]-[7], power supply circuits [8], and transceiver circuits. Microwatt operation requires that, all of the circuits in the LSI are operated in the subthreshold region of MOSFETs [9], and that the main system of the LSI is operated intermittently under the control of an on-chip reference clock circuit. Intermittent operation contributes to a drastic reduction in the power consumption of the LSI.

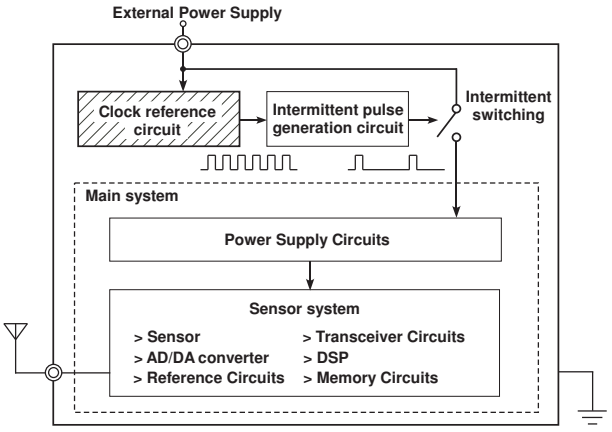

Fig. 1. Chip archtecture of microwatt power-aware smart-sensor LSI.

This paper focuses on a clock reference circuit for power-aware LSIs. Many clock reference circuits have been reported recently [10]-[12] but they are unsuitable for use in power-aware LSIs because of their large power dissipation (several milliwatts or more), large surface area (over 1 mm^2), and use of MEMS technology, which however is incompatible with standard CMOS processes. Therefore, modified low-power clock reference circuits with standard CMOS process have been reported [13]-[16]. However, these circuits have some problems. For example, their power dissipations are still large, they require high precise temperature-insensitive reference voltages and currents, and their clock frequencies are too high (over 2 MHz); these are inconvenient for use in ultra-low power LSIs. Moreover, the effect of the process variations on the reference clock was not showed in detail.

To solve these problems, we developed a clock ref-

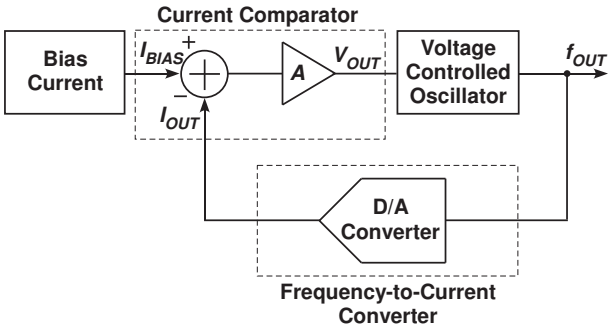

Fig. 2. Block diagram of our clock reference generator.

erence circuit that can be operated with microwatt-level power dissipation, and controlled over a wide frequency range of 20 kHz - 2 MHz. The circuit makes use of a frequency-locked loop and generates a clock frequency that is insensitive to temperature and the supply voltage.

2. Circuit configuration

Figure 2 shows a block diagram of our clock reference generator. The circuit generates a reference clock using a frequency-locked loop technique. It consists of a bias current circuit, a current comparator, a voltage-controlled oscillator (VCO), and a frequency-to-current converter, and these circuits form a feedback loop. The current comparator detects the difference between the reference current I_{BIAS} and the output current I_{OUT} of the frequency-to-current converter and generates the output voltage V_{OUT} proportional to the difference. The VCO accepts the output voltage V_{OUT} and produces oscillation pulses with a frequency f_{REF} dependent on V_{OUT}. The frequency-to-current converter accepts the oscillation pulses and generates the output current I_{OUT} proportional to f_{REF}. Then the current comparator again compares currents I_{BIAS} and I_{OUT} to produce a readjusted V_{OUT}. This feedback operation is repeated to make I_{OUT} equal to I_{BIAS}. The resulting clock frequency f_{REF} is independent of temperature and power supply voltage.

Figure 3 shows the entire circuit configuration of our clock generator including a intermittent pulse generation circuit. The following sections describe the operation of the generator in detail.

2.1 Bias Current Circuit

The bias current circuit consists of a pMOSFET and a resistor R_{REF}. A resistor is implemented as off-chip components with little temperature dependence to adjust the bias current I_{BIAS}. The reference current is given by

$$I_{BIAS} = \frac{V_{DD} - V_{GSP}}{R_{REF}}, \tag{1}$$

where V_{GSP} is the gate-source voltage of pMOSFET. Therefore, the bias current I_{BIAS} that is dependent on the resistor value can be obtained.

2.2 Current Comparator

The current comparator is a common-source circuit used to detect the difference between reference current I_{REF} and output current I_{OUT} of the frequency-to-current converter. It generates output voltage V_{OUT} proportional to the difference between the two. The capacitor C_C is added to stabilize the circuit operation.

2.3 Voltage Controlled Oscillator

The VCO consists of seven current-starved inverters connected in a ring that is operated in the subthreshold region of MOSFET. The circuit is used for producing oscillation pulses that are dependent on output voltage V_{OUT} of the current comparator. Oscillation frequency f_{REF} depends on applied current I_b and is given by

$$\begin{aligned} f_{REF} &= \frac{I_b}{2mAC_LV_{DD}} \\ &= \frac{I_0}{2mAC_LV_{DD}} \exp\left(\frac{V_{DD} - V_{OUT} - V_{TH}}{\eta V_T}\right), \end{aligned} \tag{2}$$

where m is the number of inverters in the oscillator, C_L is a load capacitance for each inverter, A is a delay fitting parameter [17], $I_0 (= (W/L)\mu C_{OX}(\eta - 1)V_T^2)$ is a process dependent parameter, V_T is the thermal voltage, V_{TH} is the threshold voltage of MOSFET, and η is the subthreshold slop factor [3]. Oscillation frequency f depends on V_{OUT}.

2.4 Frequency to Current converter

The frequency-to-current converter consists of a diode-connected pMOSFET and a switched-capacitor resistor. The circuit is used to produce output current I_{OUT} proportional to oscillation frequency f_{REF} of the VCO. The switched-capacitor resistor consists of capacitor C_S and two switches (sw1, sw2) driven with the oscillation pulses from

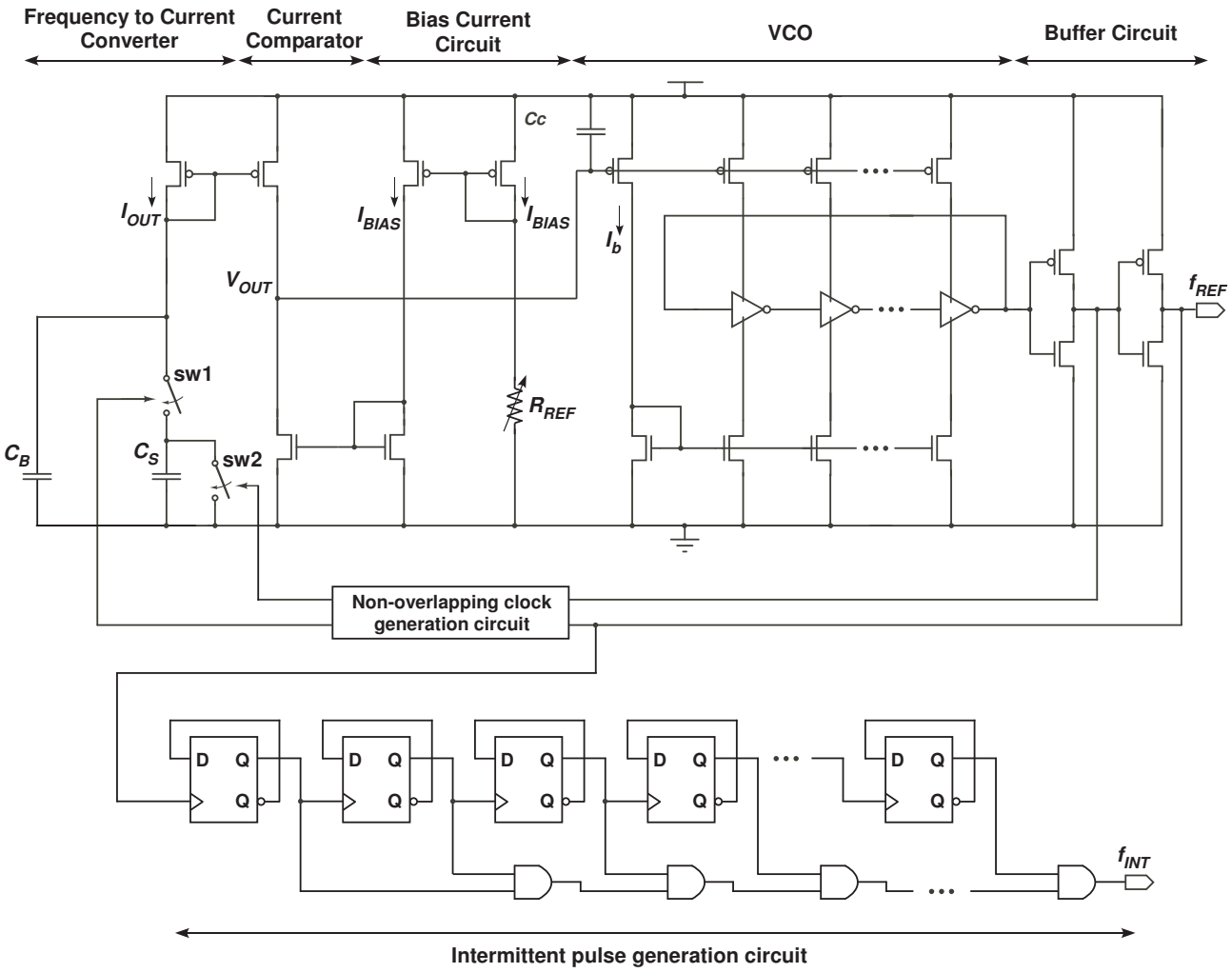

Fig. 3. Entire circuit of proposed clock reference generator.

the VCO, and operates as a resistor with a resistance of $(C_S \cdot f_{OUT})^{-1}$. Non-overlapping clock generator of the frequency-to-current converter is used to prevent switches (sw1-sw2) from simultaneously being turned on. The capacitor C_B removes high-frequency noise resulting from switching operation. Therefore, output current I_{OUT} of the frequency-to-current converter is

$$I_{OUT} = f_{REF} \cdot C_S \cdot (V_{DD} - V_{GSP}). \quad (3)$$

This current is copied into the current comparator through a current mirror. Because of the feedback operation, the circuit operates so that I_{OUT} will be equal to I_{BIAS} (i.e., Eq. (1) = Eq. (3)), and consequently, oscillation frequency f_{REF} will be

$$f_{REF} = \frac{1}{R_{REF} \cdot C_S}. \quad (4)$$

Because the off-chip resistor R_{REF} are little temperature dependence, output frequency f_{REF} is also insensitive to temperature, and by adjusting the resistor value, the oscillation frequency can be controlled.

This way, a constant reference clock with little dependence on temperature and supply voltage can be obtained.

2.5 Intermittent pulse generation circuit

The intermittent pulse generation circuit consists of a digital counter and "AND" logic circuits. The circuit accepts the reference clock f_{REF} and generates intermittent pulse f_{INT}. A duty ratio of the intermittent pulse depends on the number of the digital counter.

Therefore, adjusting the number of digital counter, a intermittent pulse with large duty ratio

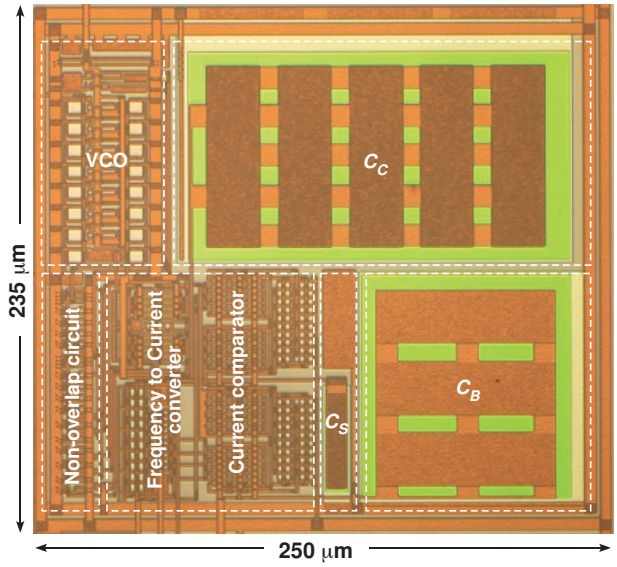

Fig. 4. Micrograph of prototype chip. Area is 0.06 mm^2 excluding intermittent pulse generation circuit.

can be obtained.

3. Experimental Results

We fabricated a prototype chip with a 0.35-μm, 2-poly, 4-metal standard CMOS process. For flexibility, the intermittent pulse generation circuit was implemented as off-chip components. Figure 4 shows a micrograph of our prototype chip. The chip area is 0.06 mm^2. The supply voltage was set to 3 V. The reference resistor R_{REF} consisting of an off-chip metal-film resistor with a low temperature coefficient was swept in a range from 1 MΩ to 100 MΩ. The results of the measurement are shown in the following.

Figure 5 shows the oscillation frequency as a function of the reference resistor. The output frequency was able to be adjusted by the reference resistor, and we found oscillation in the 20 kHz - 2 MHz frequency range at room temperature. Figures 6, 7 and 8 show an example with the resistor of 10 MΩ. Figure 6 shows measured output frequency as a function of temperature at a 3-V supply voltage. The average of the output frequency was 205 kHz. The temperature variation was 3.5 kHz in a temperature range from –20 to 80˚C. The temperature coefficient was 170 ppm/˚C. Figure 7 shows the oscillation frequency as a function of supply voltage. The circuit operated correctly with a supply voltage higher than 1.5 V. The variation in the frequency was 3.4 kHz, and the line regulation was 1%/V for a 1.5 - 3 V supply voltage. Therefore, a constant reference clock with little dependence on temperature and supply voltage could be obtained.

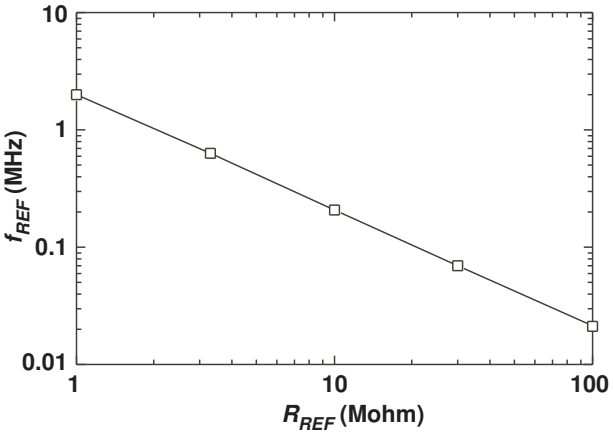

Fig. 5. Measured output frequency as a function of resistor value at room temperature. Tuning range of oscillation frequency was about 20 kHz - 2 MHz.

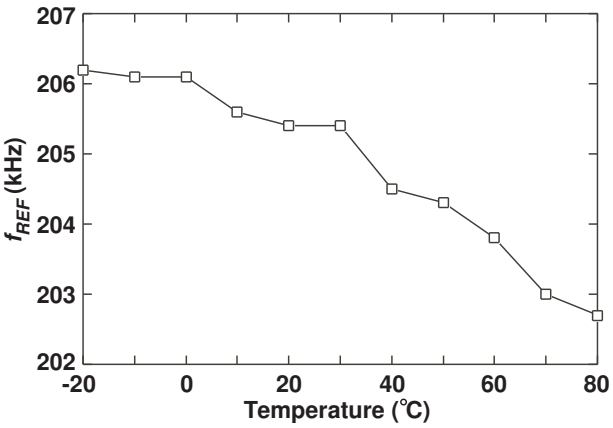

Fig. 6. Measured output frequency as a function of temperature. Temperature coefficient was 170 ppm/˚C.

To examine the process variations of our devices, we measured 20 samples, each on a different chips from same wafer. Figure 8 shows the distribution of oscillation frequency f_{REF} at room temperature. The coefficient of variation (σ/μ: μ is the mean value and σ is the standard deviation of the distribution) was 5%. The process variations of oscillation frequency f_{REF} are mainly determined by the variations of the capacitor C_S in switched capacitor resistor. Therefore, adjusting the resistor value, the output frequency can be calibrated.

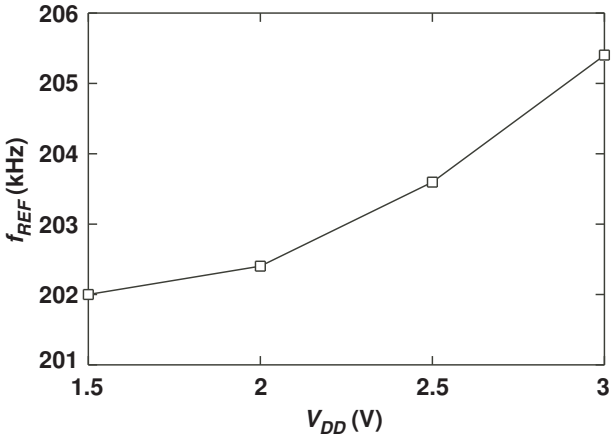

Fig. 7. Measured output frequency as a function of supply voltage. Line regulation was 1%/V.

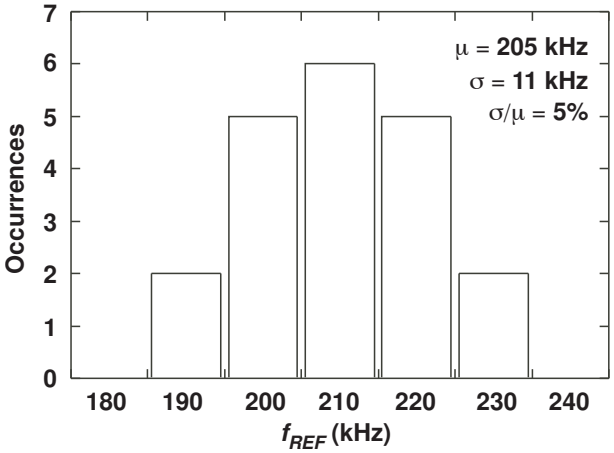

Fig. 8. Distribution of output frequency for 20 samples on different chips from same wafer measured at room temperature. Process sensitivity (σ/μ) was 5%.

Figure 9 shows an example of the output waveforms f_{REF} and f_{INT}. In this measurement, the intermittent pulse generation circuit consists of 6-bit digital counter, so the duty ratio of f_{INT} was 64 : 1. Therefore, adjusting the the number of digital counter, a intermittent pulse with large duty ratio can be obtained.

Table I summarizes the performance of our clock generator in comparison with other CMOS clock reference generator [12]-[14]. The power dissipation of the circuit with a 1.5-V power supply was 3 μW at a 200 kHz and varied from 0.5 to 30 μW at frequencies from 20 kHz to 2 MHz. Our circuit is superior to others in power consumption.

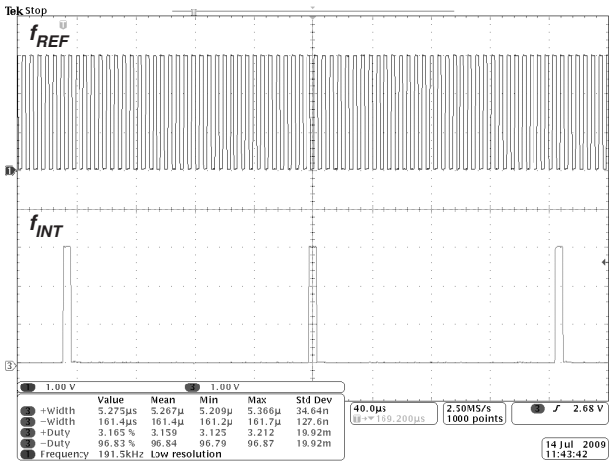

Fig. 9. Output waveforms f_{REF} and f_{INT} of our circuit at room temperature. Duty ratio of f_{INT} was 64 : 1.

4. Conclusions

A CMOS clock reference circuit was developed. A prototype chip with a 0.35-μm CMOS process was fabricated and its operation was demonstrated in this paper. The temperature coefficient and line sensitivity were 170 ppm/°C and 1%, respectively. The power dissipation was extremely low, about 0.5 to 30 μW. Our circuit would be useful for intermittent operation of power-aware LSIs that are required to operate with ultra-low-power dissipation.

Acknowledgment

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Table 1. Comparison of reported CMOS clock reference circuits

	This work	[13]	[14]	[12]
Process	0.35-μm, CMOS	0.13-μm, CMOS	65-nm, CMOS	0.25-μm, CMOS
Temperature range	–20 - 80℃	–35 - 85℃	0 - 120℃	–40 - 125℃
V_{DD}	1.5 - 3 V	1.8 - 2.5 V	1.2 V	2.4 - 2.75 V
$\overline{f_{REF}}$	20 kHz - 2 MHz	2 MHz	6 MHz	7 MHz
Power	0.5 - 30 μW (V_{DD}=1.5 V)	3 μW (V_{DD}=1.8)	66 μW (V_{DD}=1.2)	1.5 mW
Temperature Coefficient	170 ppm/℃	165 ppm/℃	86 ppm/℃	95 ppm/℃
Line regulation	1%/V	1.3%/V	N.A.	1.8%/V
Process sensitivity (σ/μ)	5% (w/o calibration) 20 samples	N.A.	0.8% (w/o calibration) 7 samples	0.13% (w/ calibration) 94 samples
Chip area	0.06 mm^2	0.015 mm^2	0.03 mm^2	1.6 mm^2

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