

A Neuromorphic CMOS Family and its Application

Tetsuya Asai, Yusuke Kanazawa, Masayuki Ikebe[†] and Yoshihito Amemiya

Department of Electrical Engineering, Hokkaido University, Sapporo, Japan

[†]Dai Nippon Printing Co., Ltd., Tokyo, Japan

Introduction

Silicon circuits that mimic the nervous systems of insects and other animals represent the future of neuro-computing. They can perform various neural functions because the microstructures of a nervous system are replicated on their silicon chips. Since recent functional models of spiking neural networks tend to use spiking neurons, neuromorphic engineers have developed CMOS neural systems with several types of spiking neural circuits to investigate the effect of spike timing and synchrony on the network's computational properties. In this report, we briefly review our recent collection of neuromorphic circuits, which we call a neuromorphic CMOS family, as well as its application to modern neural networks.

List of Present Neuromorphic CMOS Family

A. Spiking neuron circuit

We have developed several spiking neuron circuits consisting of a small number of MOS devices operating in their subthreshold region [1, 2]. A neuron circuit in [1] was designed to be equivalent to the well-known Volterra system where a simple nonlinear transformation of system variables enables designing a neural oscillator. The other neuron circuit [2] is equivalent to the Oregonator that represents a model of the Belousov-Zhabotinsky reaction and exhibits quite similar excitable behaviors to the Hodgkin-Huxley neurons.

B. Depressing and Facilitating synapse circuits

In addition to the spiking neuron circuits, we have designed a compact CMOS circuit for depressing and facilitating synapses to demonstrate useful applications of spiking neural networks; i.e., contrast-invariant pattern classification [3] and synchrony detection [3, 4]. Although the unit circuit consists of only five minimum-sized transistors, it well emulates fundamental properties of depressing synapses.

C. Bursting neuron circuit

Although the spiking neurons and depressing synapses required for implementing modern neural networks have been developed, bursting neural circuits that are suitable for CMOS implementation have not yet been fully developed. We proposed a novel bursting neuron circuit based on the Oregonator [4] to achieve compact and neuromorphic design for bursting neural circuits.

Applications of Neuromorphic CMOS Family

A. Neural Competition

Based on a model of neural competition [5], we have demonstrated that a network of the Volterra spiking neurons achieved robust and efficient neural competition on the basis of a novel timing mechanism of neural activity [1]. We showed, through both experiments and computer simulations, that the spiking neural network very efficiently achieved a robust form of neural competition that was based on spike timing rather than firing rates.

B. Contrast-Invariant Pattern Classification

Bugmann showed that the strength of a time-averaged current injected into the soma by using a spike train tends to be independent of its frequency, which implies that the response strength of a target neuron depends only on the number of active inputs [6]. To demonstrate this, we designed a network circuit in which four synapse circuits were connected to a neuron circuit, and compared the operation of the prototype circuit with nondepressed- and depressed circuit [3, 4].

C. Synchrony Detection

Senn showed an easy way to extract coherence information among cortical neurons by projecting spike trains through depressing synapses onto a postsynaptic neuron [7]. We demonstrated that the depressing synapse circuit was able to detect the synchrony in the burst times [4]. When the input bursts are not synchronized, the peak EPSPs evoked by nondepressed and depressed synapses were low. But, when the input bursts are synchronized, the peak EPSP evoked by depressed synapses was significantly larger than the nondepressed synapses.

References

- [1] T. Asai, Y. Kanazawa, and Y. Amemiya: IEEE Trans. Neural Networks **14** (2003) 1308.
- [2] T. Asai and Y. Amemiya: Proc. Int. Symp. on Multiple-Valued Logic (2003) p. 197.
- [3] Y. Kanazawa, T. Asai, and Y. Amemiya: J. Robotics and Mechatronics **15** (2003) 208.
- [4] Y. Kanazawa, T. Asai, Y. Amemiya, and M. Ikebe: Int J. Robotics and Automation (2004) in press.
- [5] T. Fukai: Biol. Cybern. **75** (1996) 453.
- [6] G. Bugmann: Biosystems **67** (2002) 17.
- [7] W. Senn, I. Segev, and M. Tsodyks: Neural Computation **10** (1998) 815.