A single-electron reaction-diffusion device for computation of a Voronoi diagram

Takahide Oya, Tetsuya Asai, and Yoshihito Amemiya

Graduate School of Information Science and Technology, Hokkaido University,
Kita 14, Nishi 9, Kita-ku, Sapporo, 060-0814 Japan
oya@sapiens-ei.eng.hokudai.ac.jp

Abstract. In this paper, we propose a novel single-electron device for computation of a Voronoi diagram (VD). A cellular-automaton model of VD formation [18] was used to construct the device that consisted of three layers of a 2-D array of single-electron oscillators. Through extensive numerical simulations, we show pattern formation on the proposed device and demonstrate the VD computation.

1 Introduction

Computation of a Voronoi diagram (VD) is one of the typical problems in computer science, and VDs are used in graphics, statistics, geography and economics [1] and [2]. The key feature of VD construction is a partition of two- or three-dimensional space on a sphere of influences generated from a given set of objects, points, or arbitrary geometrical shapes. Therefore, VDs are widely applied in data analysis; for example they have been used for identifying star and galaxy clusters [3], market analyses [2], and for modeling gravitational influences [4], cell and tissue growth [5, 6], ecological competition [7], crystal growth [8], molecules [9], animal skin pigmentation [10, 11], and geographical surfaces [12]. Its many computer science applications include pattern recognition via computation of a skeleton [13], path planning in the presence of obstacles [14], and computer graphics or computer-generated images [15]. Voronoi tessellation is also extensively used in the field of computational geometry where, it is applied to solve variations on the nearest neighbor problem [16, 17].

The reaction-diffusion (RD) algorithm (a cellular automaton (CA) model) for computation of a VD was first constructed in [18, 19]. The authors have proposed a single-electron device that is analogous to RD systems where electron-tunneling phenomena propagate on a 2-D array of single-electron oscillators [20]. This electrical RD device consists of a two-dimensional array of single-electron nonlinear oscillators that are combined with one another through diffusive coupling. In this paper, by employing the RD algorithm for the VD computation, we construct an architecture of low-power ultrafast VD computers by means of single-electron circuits.

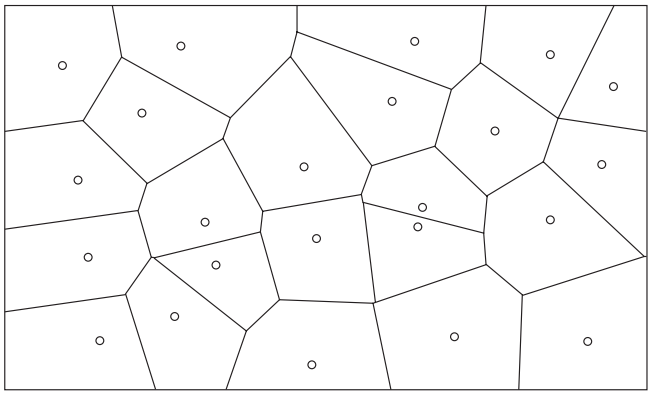

Fig. 1. Voronoi diagrams of planar points.

2 Voronoi Diagram

Given a non empty finite set $\mathbf{P}$ of planar points, a planar VD of the set $\mathbf{P}$ is a partition of the plane into such regions, that for any element of $\mathbf{P}$, a region corresponding to a unique point p contains all those points of the plane that are closer to p than to any other node of $\mathbf{P}$. A unique region

$$vor(p) = \{z \in \mathbf{R}^2 : \, d(p,z) < d(p,m) \forall m \in \mathbf{R}^2 \, m \neq z\}$$

assigned to point p is called a Voronoi cell. The boundary of the Voronoi cell of a point p is built of segments of bisectors separating the point p and its geographically closest neighbors from $\mathbf{P}$. The union of all boundaries of the Voronoi cells comprises the VD (Fig. 1):

$$VD(P) = \cup_{p \in \mathbf{P}} \partial vor(p).$$

The lower bound of a VD computation (of a d-dimensional set of n points) is $\Theta(n)$ and the worst-case complexity is $\Theta(n^{\lceil d/2 \rceil})$ [17]. The CA and RD algorithms exploit the natural parallelism of the problem; namely the distance between neighboring points is represented by the time of a wave-front traveling in space, therefore the time complexity of VD computation in the RD medium is determined by the maximum distance between two geographically neighboring points of a given set, which in turn is limited by a diameter D of the given planar set. That is, the worst-case complexity of RD computation of VD is $\Theta(D)$, independent of dimension or number of points. Assuming that we can pack given set preserving topological relationships between its elements, the computational lower bound will be $\Theta(\sqrt[d]{n})$, in the d-dimensional case.

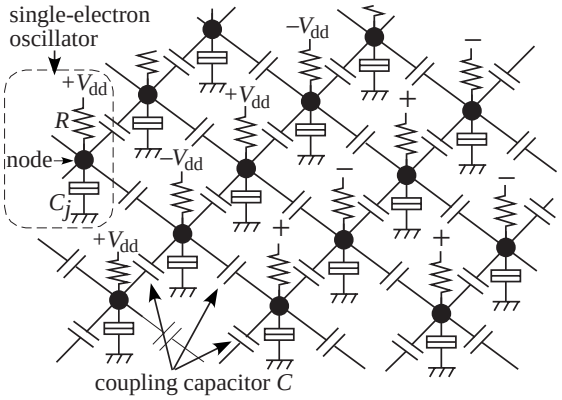

Fig. 2. Circuit configuration of single-electron reaction-diffusion device [20].

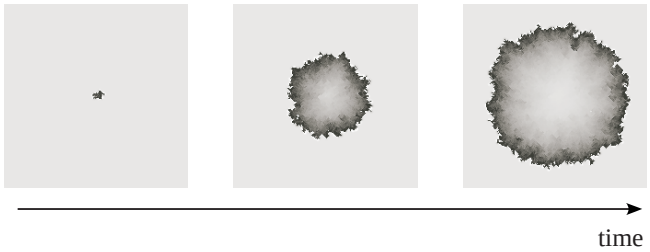

Fig. 3. Traveling nonlinear voltage wave that is generated by the original SERD device (simulated). The device has 100×100 oscillators. Simulated with parameters: tunneling junction capacitance $C_{\rm j} = 1$ aF, tunneling junction conductance $= 1$ μS, high resistance $R = 137.5$ MΩ, coupling capacitance $C = 1$ aF, bias voltage $V_{\rm dd} = 16.5$ mV, and zero temperature. In this figure, high voltage is bright and low voltage is dark [20].

3 Single-Electron Circuits for computation of Voronoi Diagram

To compute a VD, we propose the use of single-electron reaction-diffusion (SE-RD) devices. The original SE-RD device consists of arrayed single-electron oscillators and can imitate the operation of chemical RD systems [20]. For this paper, we have improved the structure of the SE-RD device for computing a VD and have simulated its operations.

Figure 2 shows the original SE-RD device. The main component is a single-electron oscillator that consists of a tunneling junction C_j and a high resistance R connected in series at a node and biased by a positive voltage $V_{\rm dd}$ or a negative one $-V_{\rm dd}$. It has voltage $V_{\rm node}$ of the node, and $V_{\rm node}$ shows the excitatory oscillation that is indispensable for imitating RD systems [20].

To compute a VD with RD systems, nonlinear waves that travel at a constant speed are necessary [18, 19]; i.e., the wave-fronts must be smooth and their

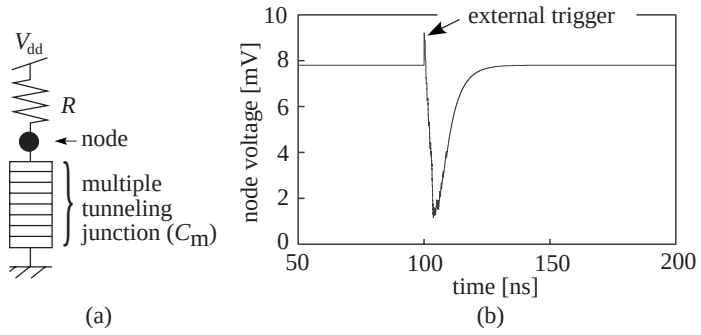

Fig. 4. Single-electron oscillator with multiple-tunneling junction. (a) circuit configuration and (b) its operation (simulated). Simulated with parameters: tunneling junction capacitance $C_{\rm m} = 10$ aF (500 aF/50 junctions), tunneling junction conductance = 5 μS, high resistance $R = 20$ GΩ, bias voltage $V_{\rm dd} = 7.8$ mV, and zero temperature.

speed must be constant. The original SE-RD device can generate nonlinear voltage waves. However, the original device is not suitable for computing a VD because the wave-fronts are not smooth and their speeds are not constant, as shown in Fig. 3. The tunneling probability of each electron at the oscillators is the reason why the waves can not travel at a constant speed. To make the wave fronts smooth and the speed of the waves constant, new oscillators in which the probability is averaged are necessary. In this paper, we propose using new oscillators with multiple-tunneling junction (MTJ) as shown in Fig. 4. The MTJ oscillator consists of a multiple-tunneling junction $C_{\rm m}$ that has n tunneling junctions and a high resistance R connected in series at the node and biased by $V_{\rm dd}$. It has a voltage $V_{\rm node}$ that shows the excitatory oscillation like the original oscillator does. There are many tunneling junctions in the oscillator, so the tunneling probability is averaged. As a result, $V_{\rm node}$ changes smoothly as shown in Fig. 4 (b). The improved SE-RD device has such oscillators.

Adjacent oscillators have to be coupled with a capacitor for the voltage waves to travel on the improved device. We simulated a one-dimensional chain of improved oscillators and confirmed its operation as shown in Fig. 5. The oscillators that in the figure are denoted by A1, A2,..., with their nodes represented by closed circles are connected to their adjacent oscillators through intermediary oscillators that are biased by a negative voltage $-V_{\rm dd}$ (these are denoted by B1, B2, ..., with their nodes represented by open circles) and coupling capacitors C (Fig. 5 (a)). When electron tunneling occurs in an oscillator in this structure, the node voltage of the oscillator decreases gently, and this induces electron tunneling in an adjacent intermediary oscillator. The induced tunneling changes the node voltage of the intermediary oscillator from low to high, and this induces electron tunneling in an adjacent oscillator. As a result, changes in node voltage that are caused by the electron tunneling are transmitted from one oscillator to another along the oscillator chain (Fig. 5 (b)). Note that the voltage waves travel

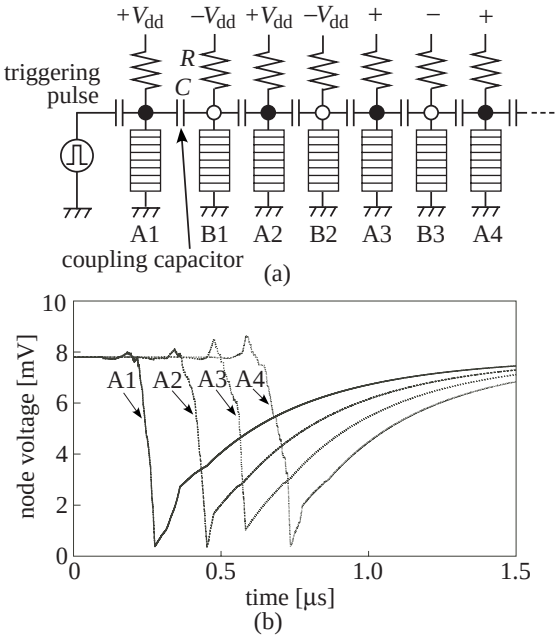

Fig. 5. One-dimensional chain of improved oscillators. (a) circuit configuration and (b) its operation (simulated). Simulated with parameters: tunneling junction capacitance $C_{\rm m} = 10$ aF (500 aF/50 junctions), tunneling junction conductance = 5 μS, high resistance $R = 20$ GΩ, coupling capacitance $C = 2.2$ aF, bias voltage $V_{\rm dd} = 7.8$ mV, and zero temperature.

at almost constant speed. This is because the tunneling probability is averaged over all oscillators.

An improved SE-RD device can be constructed by connecting oscillators into a network by means of intermediary oscillators and coupling capacitors as shown in Fig. 6. Each oscillator is connected to its four adjacent oscillators by means of four intermediary oscillators and coupling capacitors. Nonlinear voltage waves travel on the improved device at a constant speed as shown in Fig. 7. We can compute the VD by using information on collision points of the nonlinear waves for which we use CA model [18, 19] for finding collision points. According to Refs. [18, 19], in the CA model a cell that connects eight adjacent cells changes its state according to the states of the adjacent cells. The cell state transition rule is as follows:

$$x^{t+1} = \begin{cases} \beta, & \text{if } x^t = \bullet \text{ and } 1 \le \sigma(x)^t \le 4 \\ \alpha, & \text{if } x^t = \beta \text{ and } 1 \le \sigma(x)^t \le 4 \\ x^t, & \text{otherwise} \end{cases} \tag{1}$$

where x is the state of the middle cell, t is the time step, $\bullet$ is a resting cell, α is colored precipitate, β is reagent and $\sigma(x)^t$ is the number of β cells in the

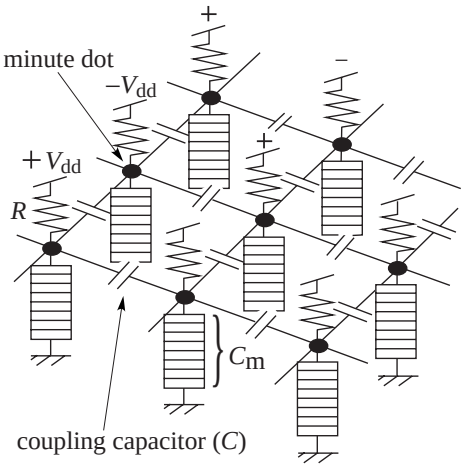

Fig. 6. Improved two-dimensional RD device consisting of network of improved single-electron oscillators. Each oscillator is connected with 4 neighboring oscillators by means of four intermediary oscillators and coupling capacitors.

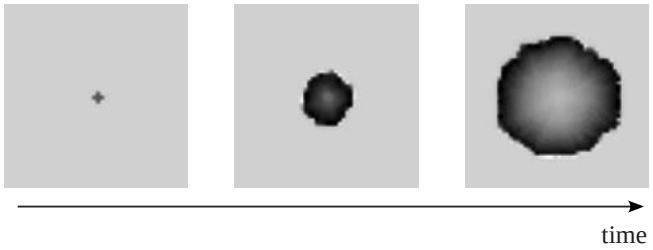

Fig. 7. Traveling nonlinear wave that is generated by the improved SE-RD device (simulated). 50 × 50 oscillators are placed in the device. This simulation used the same parameters as in Fig. 5 (b). In this figure, high voltage is bright and low voltage is dark.

eight adjacent cells. In this model, the collision points are memorized as the precipitate of reagents.

To apply this rule to our device, we consider the use of single-electron threshold detectors, specifically the single-electron boxes (SEB) that we have proposed as logic gate devices [21, 22]. The SEB consists of a single-electron trap (two identical tunneling junctions C_j, connected in series, a capacitor C_{L} and a bias voltage V_{dd}) as shown in Fig. 8 (a). This circuit has a hysteretic sawtooth function for V_{dd} as shown in Fig. 8 (b). We make use of this characteristic for threshold operation. Here we consider the threshold operation for computing a VD based on the CA model. We assume the threshold value that is the number of β cells in the eight adjacent cells to be 4.5; i.e., no electron tunneling occurs in the SEB when the node voltages of four or fewer adjacent oscillators are changed

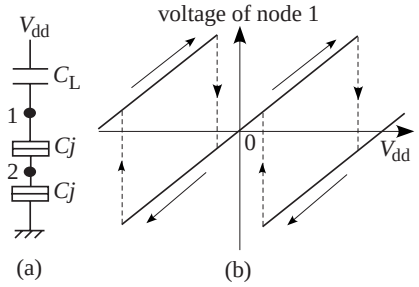

Fig. 8. Single-electron box. (a) Circuit configuration and (b) its operation [21, 22].

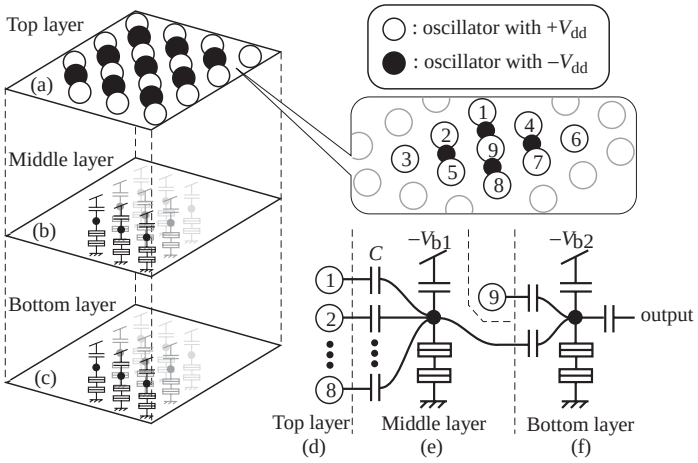

Fig. 9. Improved device that has three layers for computing a VD. The top layer is the device shown in Fig. 6. The middle layer is the first logic layer with SEB threshold detectors. The bottom layer is the second logic layer and it produces the VD.

by electron tunnelings in the oscillators. On the other hand, electron tunneling occurs in the SEB when the node voltages of five or more adjacent oscillators are changed. In addition, we can find the collision points by comparing the state of the center oscillator with the state of the SEB threshold detector. To compare the states, we use the SEB with the threshold set to 1.5; i.e., no electron tunneling occurs in the SEB when electron tunnelings occur in both the above SEB and the center oscillator.

Figure 9 shows an improved device with three layers for computing a VD. The top layer ((a) in Fig. 9) is the improved SE-RD device shown in Fig. 6. The middle layer ((b) in Fig. 9) is the first logic layer of SEB threshold detectors. Here, the SEB that is biased by the negative voltage $-V_{b1}$ ((e) in Fig. 9) are placed directly under the oscillators biased by $+V_{dd}$ (oscillator 9 in Fig. 9) and connects to the eight adjacent oscillators of the top layer (oscillators 1–8 in Fig. 9 (d)); i.e., the SEB accepts eight signals from the eight oscillators as inputs.

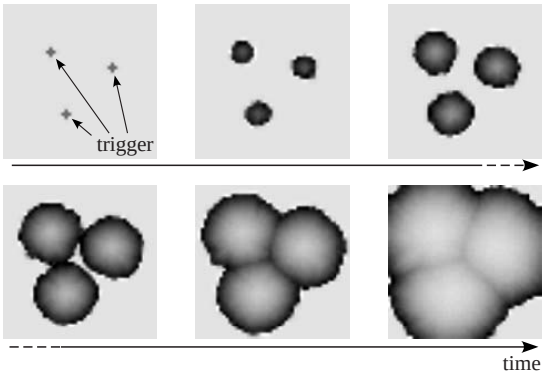

Fig. 10. Expanding circular pattern in the top layer of the device. Snapshots for six time steps. The simulation used the same parameters as in Fig. 5 (b) for the simulation.

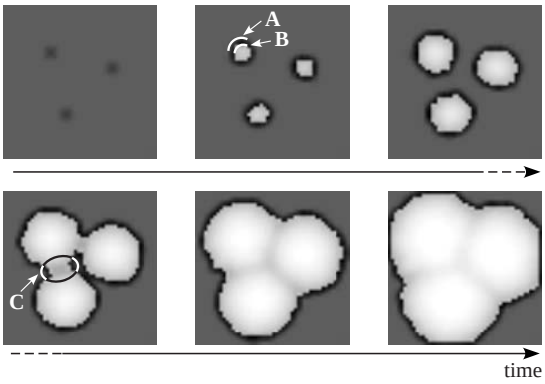

Fig. 11. Expanding circular pattern in the middle layer of the device. Snapshots for six time steps. Parameters: tunneling junction capacitance $C_{\rm j} = 20$ aF, tunneling junction conductance = 5 μS, bias capacitance $C_{\rm L} = 10$ aF, coupling capacitance $C = 2.2$ aF, bias voltage $-V_{\rm b1}$ = -26.5 mV, and zero temperature.

The bottom layer ((c) in Fig. 9) is the second logic layer. Here, the SEB that is biased by the negative voltage $-V_{\rm b2}$ ((f) in Fig. 9) connects to the oscillator 9 and the SEB in the second layer ((e) in Fig. 9); i.e., the second SEB accepts two signals from the oscillator 9 and the SEB in the second layer as inputs. The bottom layer produces the output; i.e., its output is used to draws the VD.

4 Simulation Results

We tested the device's operation by computer simulation. Figures 10, 11 and 12 show the simulation results. Figure 10 shows the density of node voltages on the top layer. A bright color means the node voltage is high. A dark color means the

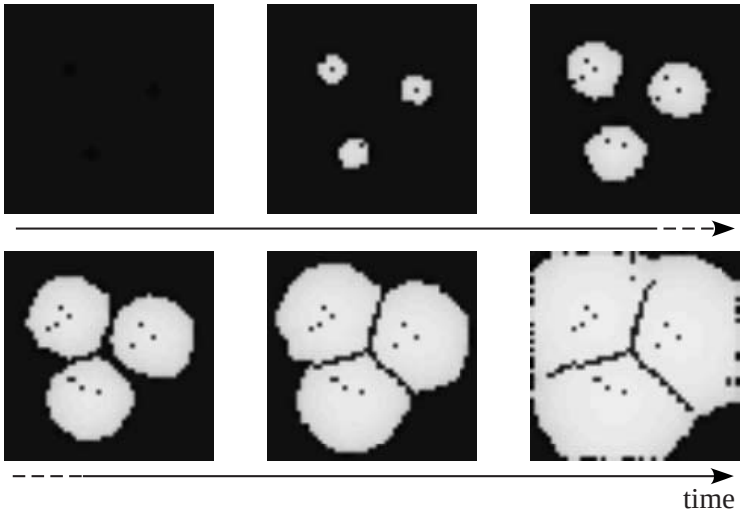

Fig. 12. Expanding circular pattern in the bottom layer of the device. Snapshots for six time steps. Traveling nonlinear waves in this layer construct a VD. Parameters are the same as in Fig. 11 without bias voltage $-V_{b2}$ = -18.5 mV.

node voltage is low. Figures 11 and 12 show the voltages on the middle layer and on the bottom layer. In Fig. 11, 'A' indicates the wave-front in the top layer, 'B' indicates the wave-front in the middle layer, and 'C' indicates collision points. In this simulation, we triggered three oscillators of the top layer as planar points for a VD. Nonlinear voltage waves traveled at a constant speed and gave the data to the middle and bottom layers. In the middle layer, the SEBs changed their node voltage when five or more oscillators of the upper eight oscillators changed their node voltage. Wave-fronts in the top layer had four or fewer oscillators that changed their voltages. As a result, traveling nonlinear waves in this layer (B in Fig. 11) followed the waves in the top layer (A). When wave 'A' collided with other waves in the top layer, the collision points had five or more oscillators that changed their voltages. Therefore, wave 'B' in this layer overtook 'A' and collided with other waves just like spanning a valley with a bridge (C). In the bottom layer, the SEBs changed their node voltages when both the voltage of the oscillators in the top layer and the SEBs in the middle layer are low. Namely, traveling waves that did not collide were memorized by the bottom layer as a high voltage. When the nonlinear waves of the top layer collided with each other, the voltages of the collision points in the top were low and the node voltages of the SEBs in the middle were high. As a result, the node voltages of the SEB in the bottom were kept low. Therefore, the bottom layer memorized the result of computing the VD. Figure 13 shows simulation results of computing a VD with five planar points by using proposed device. The results imply that we can compute a VD with any planar points on the device.

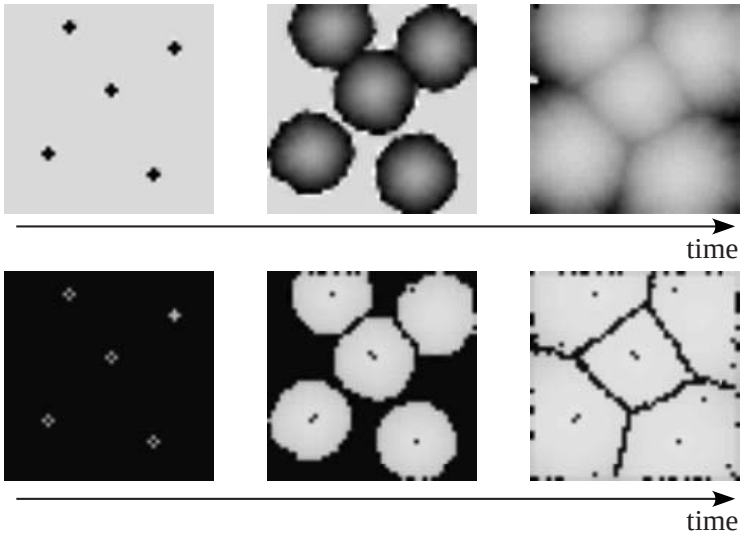

Fig. 13. Simulation results of computing a VD with five planer points by using proposed device. Upper three snapshots show the voltage density of the top layer, and the bottom three snapshots show the voltage density of the bottom layer.

5 Summary

We proposed a single-electron reaction-diffusion devices for computing a Voronoi diagram. The novel SE-RD device consists of three layers. The top layer is an improved SE-RD device in which nonlinear voltage waves are generated and travel, and the middle and bottom layer are threshold detectors. The operations of the middle and bottom layer are based on the CA model [18, 19]. The bottom layer outputs the results of computing a VD by using data from the top and middle layers.

In some simulations, the constructed VDs had noise, as can be seen in Fig. 12 and the bottom snapshots of Fig. 13. The reason may be the tunneling probability of the bottom layer or the way to apply the CA model to the middle and bottom layers. However, we were able to compute a whole VD with our device even though there was some noise.

Other points that we must consider are the size of the proposed device and the number of coupling capacitors between each layer. There are $i \times j$ oscillators with $+V_{\rm dd}$ and $(i-1) \times (j-1)$ oscillators with $-V_{\rm dd}$ in the top layer, and $i \times j$ SEBs in the middle and bottom layers, respectively. If we fabricated an oscillator, for example, measuring 100 nm $\times$ 100 nm [23], the top layer would be 0.01 ij μm^2. A top layer with 100 $\times$ 100 oscillators would be only 100 μm^2. The device would not take up a large amount of space it would be at most 3 $\times 0.01 \times ij$ μm^2. In addition, if we could construct the layers on top of one another, the area would be just 0.01 ij μm^2. On the other hand, there are eight

coupling capacitors per SEB between the top and middle layer. Therefore there are 8 ij capacitors between two layers. If the top layer had 100×100 oscillators, there would be 80000 capacitors. In this work, we have assumed that the size of such capacitors is zero, which is not realistic. Thus, we must consider a simpler structure as a future work.

Acknowledgments

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References

1. Klein, R.: *Concrete and Abstract Voronoi Diagrams*. Springer-Verlag, Berlin (1990).
2. Okabe, A., Boots, B., Sugihara, K., and Chiu S. N.: *Spatial Tesselations: Concepts and Applications of Voronoi diagrams*. John Wiley and Sons, Chichester (2000).
3. Pásztor L.: Partition based point pattern analysis methods for investigation of spatial structure of various stellar populations. Astronomical Data Analysis Software and Systems III, eds. Crabtree, D. R., Hanisch, R.J. and Barnes J. (ASP Conference Series) **61** (1994).
4. Drysdale, S.: Voronoi Diagrams: Applications from Archaology to Zoology. `http://www.ics.uci.edu/ eppstein/gina/scot.drysdale.html`.
5. Honda, H. and Eguchi, G. J.: How much does the cell boundary contract in a monolayered cell sheet. J. Theor. Biol. **84** (1980) 575–588.
6. Blackburn, C. G. and Dunckley, L.; The application of Voronoi Tessellations in the Development of 3D Stochastic Models to Represent Tumour Growth. Zeitschrift fur Angewandte Mathematik und Mechanik. **76** (1996) 335–338.
7. Barlow, G. W.: Hexagonal territories. Animal Behavior. **22** (1974) 876–878.
8. Hargittai, I. (Ed): *Symmetry: Unifying Human Understanding*. Pergamon Press, New York (1986)
9. Pontius, J. Richelle, J., and Wodak, S. J.: Deviations from standard atomic volumes as a quality measure for protein crystal structures, J. Mol. Biol. **264** (1996) 121-136.
10. Walter, M., Fournier, A., and Reimers, M.: Clonal mosaic model for the synthesis of mammalian coat pattern *Proc. Graphics Interface*, `http://www.graphicsinterface.org/proceedings/1998/118/`.
11. Meinhardt, H.: *The alogorithmic beauty of Sea Shells*. Springer, New York (1995).
12. Bray, N. H., Anderson, J. B., Devine, J. D., and Kwasnik, J. M.: Topological Properties of Random Crack Networks. Mathematical Geology. **8** (1976) 617–626.
13. Adamatzky, A. and De Lacy Costello, B. P. J.: Collision-free path planning in the Belousov-Zhabotinsky medium assisted by a cellular automaton. Naturwissenschaften. **89** (2002) 474–478.
14. Earnshaw, R. A. (Ed): *Theoretical Foundations of Computer Graphics and CAD*. NATO ASI series, series F: Computer and Systems Sciences. **40** Springer -Verlag, Berlin (1998).

15. Deussen, O., Hiller, S. van Overveld, C., and Strothotte, T.: Floating Points: A Method for Computing Stipple Drawings. Computer Graphics Forum. **19** (2000) 41–50.
16. Graham, R. and Yao, F.: A whirlwind Tour of Computational Geometry. American Mathematical Monthly. **97** (1990) 687–701.
17. Preparata, F. P. and Shamos, M. I.: *Computational Geometry*. Springer Verlag, Berlin (1985).
18. Adamatzky, A.: Reaction–diffusion algorithm for constructing discrete generalized Voronoi diagram. Neural Netw. World. **6** (1994) 635–643.
19. Adamatzky, A.: Voronoi–like partition of lattice in cellular automata. Mathl. Comput. Modelling. **23** (1996) 51–66.
20. Oya, T., Asai, T., Fukui, T., and Amemiya, Y.: Reaction-diffusion systems consisting of single-electron circuits. Int. J.Unconventional Computing. **1** (2005) 177–194.
21. Oya, T., Asai, T., and Amemiya, Y.: Single-electrron logic device with simple structure. Elec. Lett. **39** (2003) 965–967.
22. Oya, T., Asai, T., Fukui, T., and Amemiya, Y.: A majority-logic device using an irreversible single-electron box. IEEE Trans. Nanotech. **2** (2003) 15–22.
23. Oya, T., Asai, T., Fukui, T., and Amemiya, Y.: A majority-logic nanodevice using a balanced pair of single-electron boxes. J. Nanosci. and Nanotech. **2** (2002) 333–342.