A neuromorphic LSI performing noise-shaping pulse-density modulation with ultralow-power subthreshold neuron circuits

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An inhibitory network model that performs noise-shaping pulse-density modulation [1] was implemented on a subthreshold analog LSI, aiming at the development of ultralow-power AD converters. Through circuit simulations, we evaluate the effects of the noise shaping produced by the network on the LSI.

The network consists of N integrate-and-fire neurons (IFNs) with all-to-all inhibitory connections [1]. A common analog input is given to all the IFNs, while 1-bit digital output is given by the sum of firing events of the IFNs. Static and dynamic noises are introduced into the analog input and the reset potential of IFNs after each firing, respectively. Since the wiring complexity of the network; i.e., $O(N^2)$ in [1], can be reduced to $O(N)$ by introducing a global inhibitor [2], we designed a network circuit as shown in Fig. 1. The static and dynamic noises are given to the circuit as device mismatches of current sources (I_i) and external random (Poisson) spikes, respectively. Figure 2 shows an example of the circuit simulations (N = 3, I_i = [1:1.2] nA, amplitudes of the Poisson spikes: 1 nA, the width: 10 μs, the mean and variation: 5000). When IFNs were uncoupled (K = 0), inter-spike intervals (ISIs) of the output spike trains looked almost random, while they were almost uniform when the IFNs were coupled with K = 3. Figure 3 shows a histogram of ISIs for K = 0 and 3. As expected in [1], the coupled network produced a Gaussian-like distribution of ISIs, while the uncoupled one had a broad distribution. Figure 4 shows the power spectrum of the coupled and uncoupled network with sinusoidal inputs ($I_i = I_0 + A \sin(2\pi f t)$, I_0 = 1 nA, A = 50 pA, f = 100 Hz). A measured SNR of the uncoupled network was 10.2 dB, while that of the coupled one was 18.1 dB, which indicated that the network reduced the noises significantly, although noise-sensitive (but low-power) subthreshold CMOS devices were used in the circuit.

References

[1] Mar DJ, Chow CC, Gerstner W, Adams RW, and Collins JJ, *Neurobiology*, vol. 96, pp. 10450-10455, 1999.
[2] Asai T, Kanazawa Y, Amemiya Y, *IEEE Trans. Neural Networks*, vol. 14, no. 5, pp. 1308-1312, 2003.

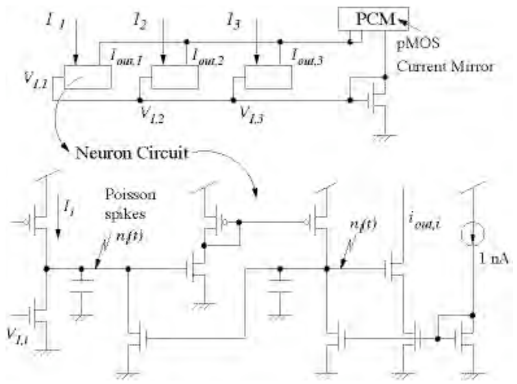

Fig. 1. Circuit structure of neuron and network.

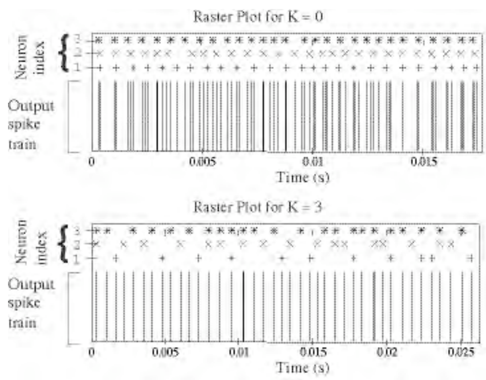

Fig. 2. Output spikes of the network circuit.

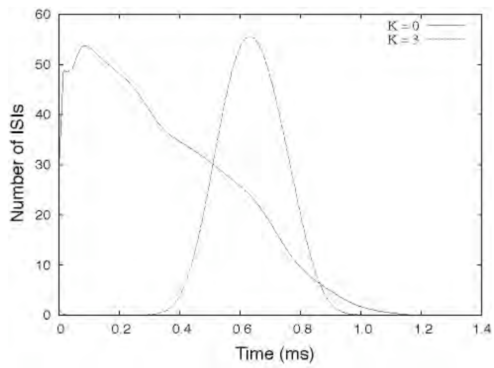

Fig. 3. Histogram of inter-spike-intervals in Fig. 2.

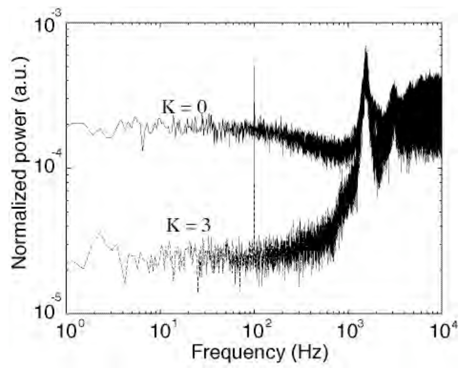

Fig. 4. Power spectrum of output spikes.