Fault-Tolerant Architectures for Nanoelectronic Circuits employing Simple Feed-Forward Neural Networks without Learning

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Abstract. A reliable circuit-design methodology [6] based on simple feed-forward neural networks (without learning) and utilizing averging and thresholding mechanisms, is used to investigate the robustness of nano-electronic circuits. The methodology, proposed earlier by some authors of this paper, provides a viable way of improving the reliability of nanoelectronic systems built with unreliable devices. In this work, single-electron Boolean circuits connected to a single-electron averaging-and-thresholding circuit demonstrated that the probability of proper functioning, hence reliability increased with the redudancy factor.

Key words: Feed-forward neural networks; Single-electron; Fault-tolerant; Averging-and-thresholding circuit; Neuro-morphic

1 Introduction

As physical features of electronic devices approach the deep sub-micron (nano) scales, nano-electronic properties become more and more pronounced [8]. A long term research into how to sufficiently use such deep sub-micron device structures, and how to utilize their quantum electronic properties in post-silicon electronics is without doubt picking pace. A number of device fabrication technologies for nano-electronic devices, in particular, single-electron [3] and nano-wire devices have been proposed and demonstrated [10]. Single-electron devices inherently operate with extreme low power dissipation, and provide a high integration density per unit area. Thus, they are viewed as potential building blocks for low-power computational applications in future LSIs. However, one of the major problems facing nano-devices in the late- and post-silicon era is that they are potentially *unreliable*. Their low reliability originates from two factors: i) inevitable high mismatches in fabricated device features amongst individual devices (this translates

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to variation in device characteristics), and ii) sensitivity to internal and external interferences (for example, thermal noises and electromagnetic radiations).

Biological systems can provide a possible solution to creating robust circuits with failure prone nano-electronic devices. For instance, neurons are highly sensitive to internal and external interference, and have a huge discrepancy in structural characteristics. Some of them are permanently faulty, and have large jitters in signal transfer. Nevertheless, they effectively carry out information processing; from sensing to signal transmission in biological systems. This is believed to be as a result of the high redudancy in their network structures. Therefore, in creating electronic systems with nano-electronic devices, learning from neuronal-systems would be significantly important. Such sytems created with hints from biological systems are referred to as *neuromorphic* systems [1]-[2].

In this paper we demonstrate that a simple feed-forward averaging-and-thresholding technique [6] can be utilized to improve robustness of single (few)-electron circuits, in the presence of mismatches in device parameters. This method can also be used to overcome soft errors and transient faults in electronic systems.

2 Methodology and Circuit Configuration

The proposed system for improving reliability with averaging-thresholding gates (see [6] for details on the methodology), consists of simple feed-forward network shown in Fig. 1.

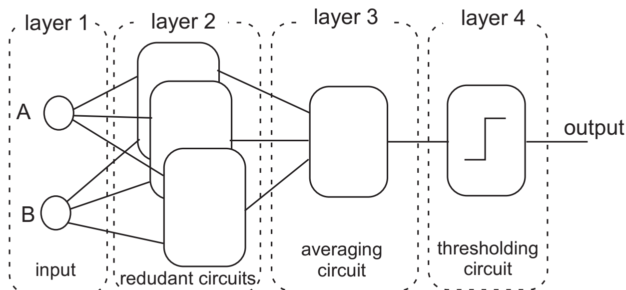

Fig. 1. Proposed simple feed-foward system consisting of redudant circuits, averaging and thresholding circuits.

The model consists of 4 layers: the input layer can accomodate digital or analog values. The second layer consists of redudant blocks performing logic computation, while the averaging layer receives inputs from the preceding logic blocks in layer 2. The averaging layer aggregates the 2nd layer's output and feeds it to the adaptabe thresholding circuit. The thresholding circuit receives

the aggregated output to produce a logic "1" output if the summed input exceeds the threshold voltage, or produces logic "0" if the sum is less than the threshold. For investigation purposes, we considered single-electron neurons [3]-[5] as logic blocks.

2.1 Neuron Circuit with Single-electron Inverter

The basic element of our single-electron neurons is a single-electron box [3]. Fig. 2(a) shows the construction consisting of a tunneling junction C_j and a biasing capacitor C. The single electron box operates by controlling the transport of individual electrons between the ground and the node through the Coulomb blockade effect [3]. When the bias voltage V_d is increased above threshold voltage V_th ($\equiv e/2(C + C_\mathrm{j})$), Coulomb blockade is broken and an electron tunnels from the ground to the node across the tunneling junction. This leads to a drop in the node voltage (see drop A $\rightarrow$ B in Fig. 2(b)). Increasing the bias voltage further increases the node voltage again to repeat the same cycles. A single-electron inverter (Fig. 3) consists of two single-electron transistors (SET 1 and SET 2), forming a *quasi*-CMOS inverter.

The inverter operates by breaking Coulomb blockade in one transistor while retaining the other within the Coulomb blockade region. This is achieved by switching input voltage V_in between logic "0" and "1". If the input voltage is at logic "0", Coulomb blockade in SET 1 is broken, and an electron tunnels from node i through SET 1 to voltage source V_dd. This leaves a hole in node i, consequently leading to a logic "1" at the output. On the other hand, if a voltage corresponding to logic "1" is fed to the input terminal, Coulomb blockade in SET 2 is broken, and an electron tunnels from the ground to node i. This introduces an excess electron in the node, leading to a logic "0" output.

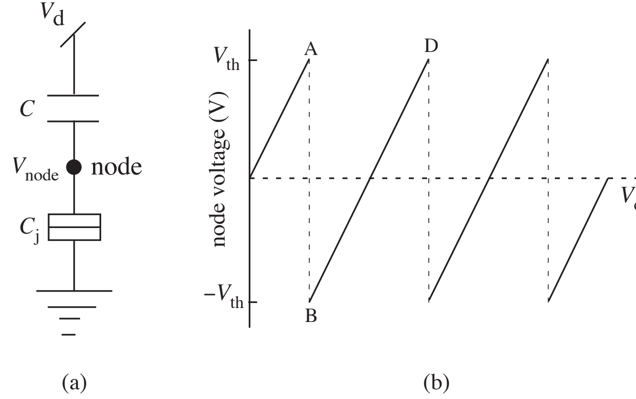

Fig. 2. Single-electron box: (a) configuration (b) charging (B $\rightarrow$ D) and discharging (A $\rightarrow$ B) waveforms for node voltage V_node.

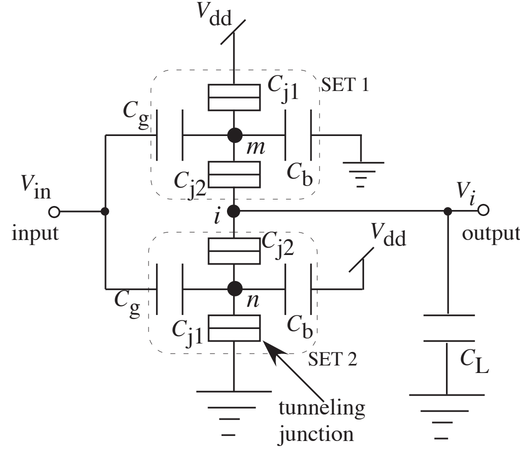

Fig. 3. Configuration of a unit inverter circuit.

2.2 Thresholding Circuit

The proposed threshold circuit (based on single-electron logic circuits [7]) consists of a tunneling junction C_j, a thresholding bias voltage V_bias, a thresholding capacitor C_b, and capacitor C_o, as shown in Fig. 4. The thresholding circuit receives inputs $(V_1, \ldots, V_n)$ from the preceeding single-electron neurons weighted through the respective capacitor C_i^w. The threshold voltage for the junction is given as $V_\text{th} = e/2(C_\text{j} + C_\text{t})$, where e is the charge of an electron, and C_t is the equivalent capacitance viewed from the tunnel junction. If the summed input voltage at node k exceeds the threshold voltage, an electron tunnels from node "o" to "k" across C_j, leading to a logic "1" output value. Otherwise the node voltage remains at logic "0". The bias voltage V_bias could be used to tune the threshold voltage across the junction.

3 Simulations Results

To confirm whether the degree of reliability improves against device failures, we investigated the performance of single-electron neural circuits connected to the thresholding circuit. The errors in individual neurons was simulated by varying the device parameters of each element of the inverter circuits (C_g, C_b, C_j1, and C_j2) in the second layer, with respect to their optimal values. The simulations were partly carried out with Monte-Carlo based SIMON simulation tool [9].

Fig. 5 shows the transient operation of a single-electron inverter with ideal parameters: $C_\text{j1} = 1$ aF, $C_\text{j2} = 2$ aF,$C_\text{g} = 8$ aF, $C_\text{b} = 7$ aF and $C_\text{L} = 24$ aF. When the input voltage exceeds (or decreases below) the threshold value, the output

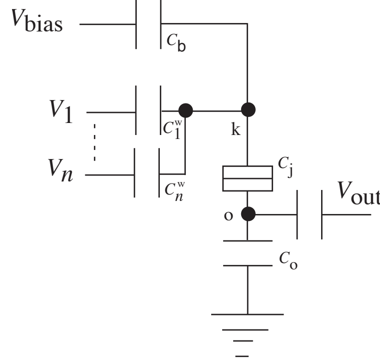

Fig. 4. Configuration of the threshold circuit based on single-electron logic circuits.

terminal produces logic "0" (corresponding to 0 V) or logic "1" corresponding to 6.5 mV.

To emulate device fabrication variations, all the device parameters were calculated in each consecutive simulation iteration, according to a Gaussian distribution with a mean value μ and standard deviation σ. The mean value for each constitutive element in the inverter circuit was defined as the ideal capacitance value, and a common standard deviation for each iteration was used to calculate all the new parameters. The thresholding circuit was assumed to be an ideal circuit. The thresholding circuit parameters were set as follows. $C_i^{\mathrm{w}\prime}$s were set to 0.5 aF, C_b to 13.7 aF, C_{j} to 1 aF, and C_{o} to 8.1 aF. Note that the thresholding circuit could be fabricated with larger device features, hence the variation in its parameters would be less critical than that of the redudant circuits. We investigated the probability of correct performance with respect to the variation of the (inverter) neuron parameters.

Fig. 6 shows the entire circuit configuration consisting of redudant circuit blocks connected to the thresholding circuit through capacitors. The input layer accepts input voltage of 6.5 mV as a logic "1" and 0 V as logic "0".

The simulation results are shown in Fig. 7. The horizontal axis shows the variance of each capacitor value with respect to the ideal value, while the vertical axis shows the probability of correct operation. The correct operation is defined as the output obtained with ideal parameters for each of the redudant circuit. As the redudancy factor R increases, the probability of correct operation, hence robustness increases.

4 Summary

We investigated the application of a simple feed-forward averaging and thresholding methodology in improving the performance of error-prone single-electron

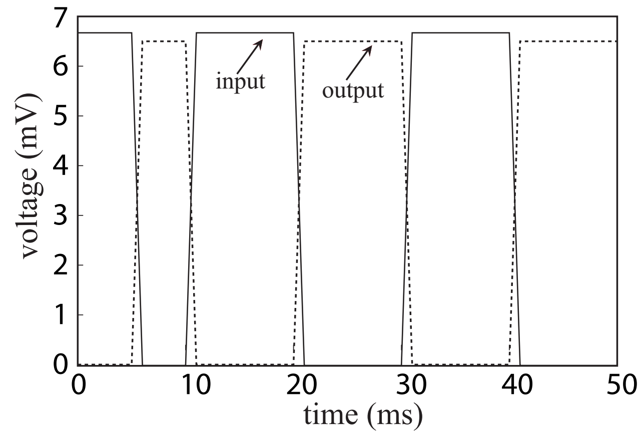

Fig. 5. Transient operation of the inverter circuit with ideal parameters. Capacitances of tunneling junctions C_{j1}, C_{j2}, gate capacitors C_g and C_b were set to 1 aF, 2 aF, 8 aF and 7 aF, respectively. Load capacitor C_{L} and bias voltage V_{dd} were set to 24 aF, and 6.5 mV, respectively. The simulation temperature (T) was 1 K.

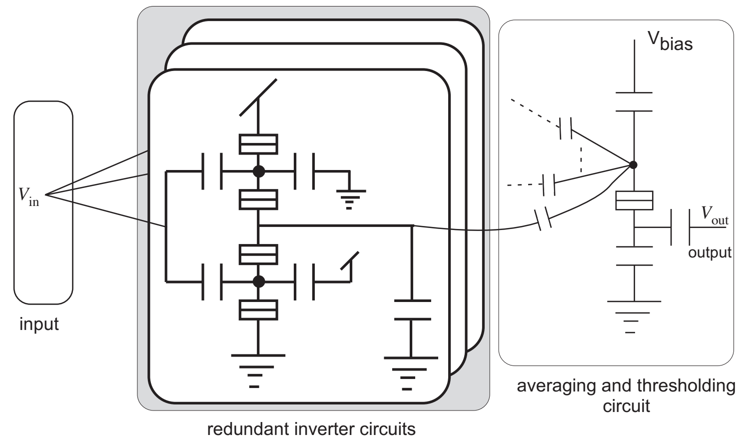

Fig. 6. Entire circuit construction consisting of redudant inverter circuits, averaging and thresholding circuits.

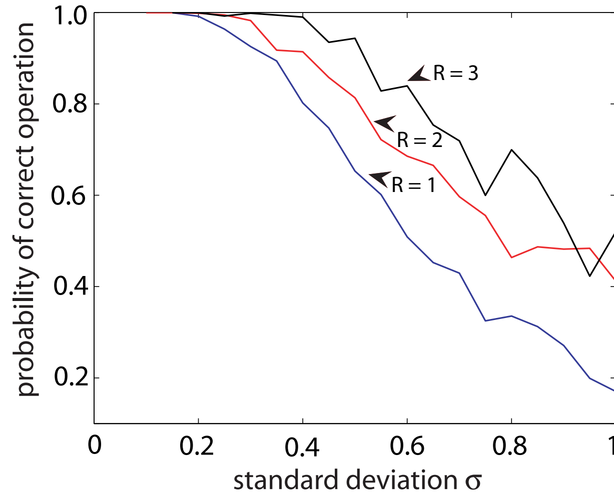

Fig. 7. Simulation results. Horizontal axis represents the standard deviation of circuit capacitances, vertical axis represents the probability of correct operation. R is the redudancy factor.

devices. We examined a significant improvement in reliability performance with increasing level of redudancy. For instance, to guarantee correct operation with a probability of above 80%, a single neuronal (inverter) circuit would allow a parameter range of $C_{\text{ideal}}(1 \pm 0.4)$, as compared to $C_{\text{ideal}}(1 \pm 0.7)$ for a network with a redudancy factor of 3, where C_{ideal} refers to the ideal capacitance value for each element in the inverter circuit.

References

1. Mead, C., (1989). *Analog VLSI and neural systems.* New York: Addison Wesley.
2. Douglas R., Mahowald M. , and Mead C. (1995). Neuromorphic Analogue VLSI. *Annual Review of Neuroscience*, 18, 255–281.
3. H. Grabert and M.H. Devoret, *Single Charge Tunneling—Coulomb Blockade Phenomena in Nanostructures.* New York: Plenum, 1992.
4. M. Akazawa, K. Kanaami, T. Yamada, and Y. Amemiya, "Multi-valued inverter using a single-electron tunneling circuit," *IEICE Trans. Electron*, E82-C, 1607, 1999.
5. J.R. Tucker, "Complementary digital logic based on the "Coulomb blockade"," *J. of Appl. Phys.*, 72, 4399, 1992.
6. A. Schmid, and Y. Leblebici, "Robust circuit and system design methodologies for nanometer-scale devices and single-electron transistors," *IEEE Trans. on VLSI systems*, 12, 1156, 2004.
7. C. Lageweg, S. Cotofana, and S. Vassiliadis, "Single electron encoded latches and flip-flops," *IEEE Transactions on Nanotechnology*, 3, 237, 2004.
8. H. Hamed, "Single electron devices: challenge for nanofabrication," *J. of vac. Sci & Tech.*, 15, 2101,1997.

9. C. Wasshuber, H. Kosina, and S. Selberherr, "SIMON-A simulator for single-electron tunnel devices and circuits ," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, 16, 937, 1997.
10. K. Kumakura, J. Motohisa, and T. Fukui, "Formation and characterization of coupled quantum dots (CQDs) by selective area metalorganic vapor phase epitaxy," *J. Crystal Growth*, vol. 170, no. 1, pp. 700-704, 1997.