An Analog-Digital Hybrid CMOS Circuit for Two-Dimensional Motion Detection with Correlation Neural Networks

Tetsuya Asai, Masato Koutani, Yoshihito Amemiya

Department of Electrical Engineering, Hokkaido University,
Kita 13, Nishi 8, Kita-ku, Sapporo, 060-8628, Japan.
E-mail: asai@sapiens-ei.eng.hokudai.ac.jp

Abstract

In this paper, we propose an analog-digital hybrid CMOS circuit producing two-dimensional optical flows, aiming at the development of high-speed and compact motion-sensing systems. The proposed circuit can compute the optical flow in real time by parallel operations of a number of local motion processors on the basis of the mechanisms of biological motion detectors. The circuit consists of asynchronous current-mode digital subcircuits for edge detection and analog subcircuits for local motion detection. The results of SPICE simulation confirmed that the circuits can compute two-dimensional local velocities with extracting edges of incident images. This shows that a high-speed motion-sensing chip can be developed with standard VLSI technology.

1 Introduction

Motion detection is the most important and fundamental visual modality in both biological and artificial vision systems. For instance, in flying insects, wide-field and direction selective neurons are major components of the optmotor pathway for flight stabilization [1], [2], [3]. From an engineering point of view, the motion detection is particularly attractive since the real-time computation of motion will greatly benefit various image applications such as the visual tracking, the depth recognition, and the formation of direction selective maps[4], [5]. However, the real-time motion detection is quite difficult for conventional digital computers because the motion computation requires massive amount of computational power.

Recently, analog motion-detection chips have been proposed and fabricated aiming at the development of the real-time motion detection systems [6], [7], [8], [9], [10], [11]. These chips can be classified into two kinds depending on their computational methods of motion: i) performing quadratic regularization and solving associated Eular-Lagrange equations by analog circuits [6], [7], [8], and ii) imitating the operation of biological motion detectors by analog circuits [9], [10], [11]. The former requires precise device matching (high uniformity in the characteristics of devices used in the computing circuits), and this prevents the development of practical motion-detection systems. In contrast, the latter approach is very attractive and promising for practical systems because the motion computation in this approach is based on collective operations of a large number of neurons and, therefore, can be performed without requiring precise device matching of neuron circuits. The fabricated chips demonstrated that the local motion detectors can compute the optical flows over a wide range of the local velocity. Although those chip have demonstrated the great superiority in calculation speed to the digital computers, the influences of the extensive device mismatches still prevents the development of practical motion-detection systems. To develop practical LSI systems based on the latter approach, several analog circuits should be replaced with asynchronous digital circuits with compact interfaces between the analog and digital circuits.

In this paper, on the bases of the latter approach, we propose a novel analog circuit for motion detection with asynchronous current-mode digital circuits (a current-mode hybrid CMOS circuit) aiming at the development of practical motion-detection systems. The current-mode digital circuit quantizes luminance values of input images and detects binary edges of the quantized image. Noises in the input image are eliminated by this quantization. The asynchronous and subthreshold current-mode operations of the proposed digital circuits make the total power dissipation quite low. The analog circuit computes local motion of the binary edged images produced by the digital circuit. In the analog circuit, a delayed signal, which is necessary to implement the biological motion detectors, is electrically produced without implementing large capacitances. The unit circuit outputs voltage pulses which represent local velocities.

This paper is organized as follows. In section II, we propose a practical motion detection system which is suitable for the hybrid CMOS circuits. Then in section III, we propose asynchronous current-mode CMOS circuits for image quantization and edge detection, and compact analog CMOS circuits for local motion detection. Section IV shows the behavior of the proposed circuits by a simulation program with integrated circuit emphasis (SPICE). Section V is devoted to summary.

2 Motion Detection Systems based on Correlation Neural Networks

In this section, we propose a practical motion-detection system consisting of a binary edge-detection system (BEDS) and correlation neural networks (CNN). In this system, the BEDS accepts an input image to extract edges of the image and then the CNN processes the edged signals to detect the motion in the image.

The BEDS consists of i) an image smoother, ii) a quantizer, and iii) exclusive OR (XOR) operators. Figure 1 shows the one-dimensional operation of the BEDS. First, the image smoother eliminates noises in the input image[Fig. 1(a)]. Then, the quantizer transforms the pixel values of the smoothed image into binary data by comparing the pixel values with specified threshold value [Fig. 1(b)]. Finally, the XOR operator extracts the edges of the quantized image by an exclusive-OR operation between the binary values of adjacent two pixels [Fig. 1(c)].

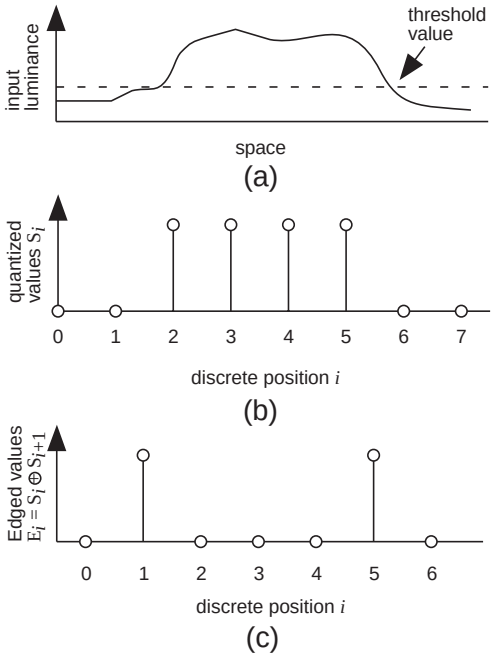

Fig. 1 One-dimensional operations of BEDs

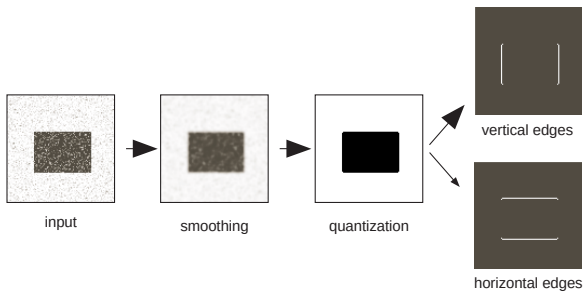

Fig. 2 Two-dimensional operations of BEDs

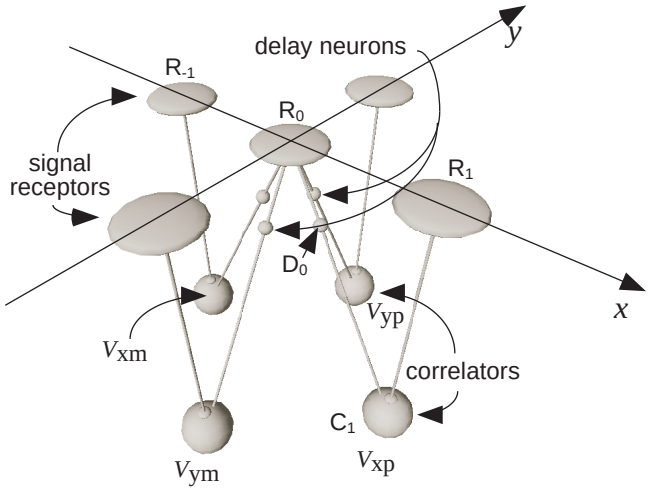

Fig. 3 An unit network of the two-dimensional CNN

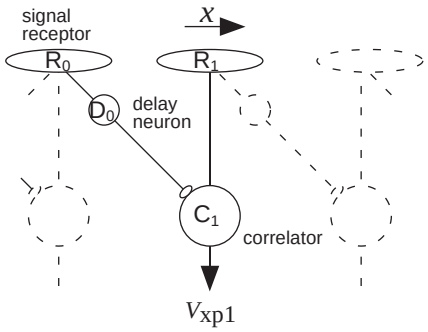

Fig. 4 One-dimensional CNN

Figure 2 shows the two-dimensional operation of the BEDS. First, an input image is smoothed and quantized. Then, two edged images are produced: i) vertical edges produced by the XOR operations between horizontal pixels, and ii) horizontal edges produced by the XOR operations between vertical pixels. The horizontal and vertical edged images are separately given to the following two-dimensional CNNs.

Figure 3 shows an unit network of the two-dimensional CNN (a pixel element together with adjacent four pixel elements). The unit CNN consists of i) five signal receptors that receive the pixel value of the horizontal and vertical edged images from the BEDS, ii) four delay neurons, and iii) four correlators that correlate the outputs of the signal receptors and the delay neurons. Velocity signals in the unit CNN are represented by four outputs ($V_{\rm xm}$, $V_{\rm xp}$, $V_{\rm ym}$, and $V_{\rm yp}$) of the four correlators. When an edged image moves along with the x-axis, either $V_{\rm xm}$ or $V_{\rm xp}$ becomes nonzero value depending on the sign of velocity (direction) of the moving edge, while $V_{\rm ym}$ or $V_{\rm yp}$ becomes nonzero value when the edged image moves along with the y-axis.

One-dimensional CNN (cross-sectional view along with the x-axis in Fig. 3) is shown in Fig. 4. The edges moving past the signal receptors generates sequential responses on the correlators because the receptors view adjacent points in space and project to the correlator. At correlator $\rm C_1$, the output signal $V_{\rm xp1}$ is the correlation

value given by the product of the signal from R_0 delayed through delay neuron D_0 and undelayed signals from R_1. The output depends on the velocity of the edge moving past from R_0 to R_1, and in consequence, the local velocity signal can be obtained by this CNN structure. When the edge moves in the opposite direction (R_1 to R_0), the delay mechanism decreases the correlation between the delayed and undelayed signals and, in consequence, decreases the output of the correlator. Therefore, the one-dimensional CNN has direction selectivity to the moving edges.

It should be noticed that the correlator also produces an output when both R_0 and R_1 are simultaneously activated. This means that the network regrettably responds to a stational inputs given to two or more pixels. Therefore, edge detection transforming an input image into a one-pixel-line image is necessary in advance of the CNN processing.

3 Hybrid CMOS Circuits for Motion Detection

To present practical form of our idea, we designed hybrid CMOS LSIs that implement the proposed motion-detection system. Figure 5 shows the floorplan of the LSI. The LSI consists of two-dimensional array of unit processors (pixel circuits operating in parallel). Each pixel circuit accepts incident images and calculates local motion according to the proposed motion-detection scheme. When a pixel circuit (i, j) is selected by signals (x-select and y-select) produced by vertical and horizontal scan registors, the circuit outputs four voltage signals; $VX_{\rm out}$(rightward), $VX_{\rm out}$(leftward), $VY_{\rm out}$(downward), and $VY_{\rm out}$(upward) representing rightward, leftward, downward, and upward motions of pixels at the position (i, j) in the incident image.

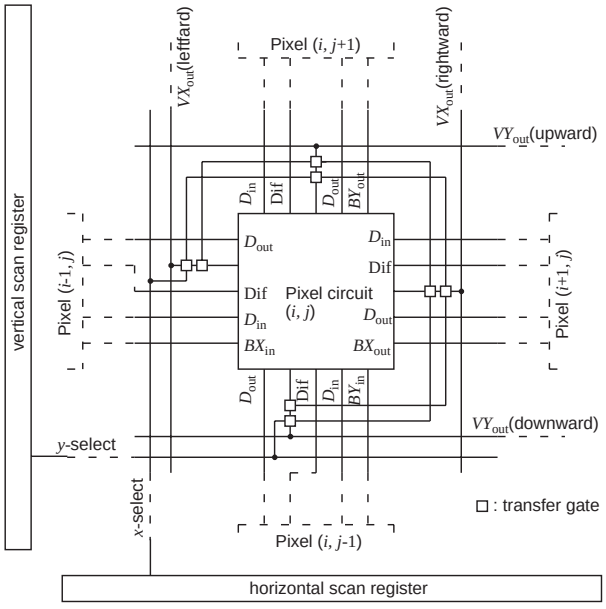

Fig.5 Chip overview

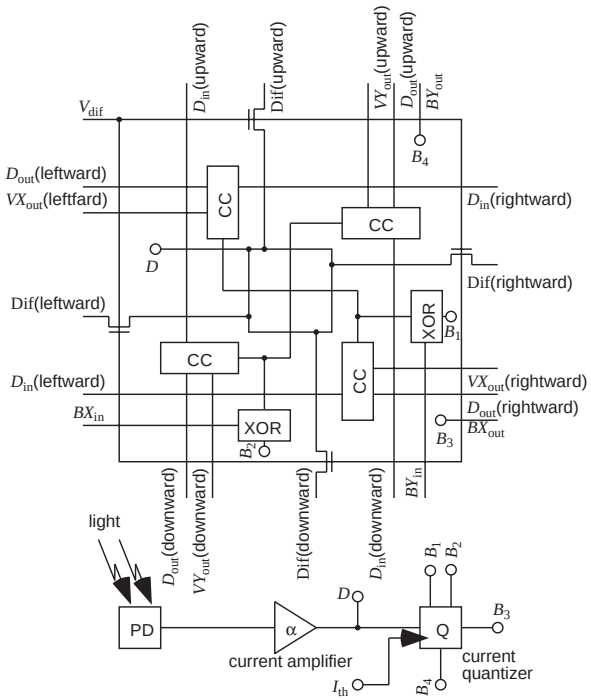

Fig.6 Construction of the pixel circuit

Figure 6 shows the construction of the pixel circuit. The circuit consists of a photodiode (PD), a current amplifier (α), a current quantizer (Q), two current-mode exclusive OR circuits (XOR), four nMOS transistors, and four correlation circuits (CC). The circuit has 16 local ports for the data inputs/outputs. The four ports labeled Dif (leftward, rightward, upward, and downward) are used for the image smoothing. The four ports denoted by $BX_{\rm in}$, $BX_{\rm out}$, $BY_{\rm in}$, and $BY_{\rm out}$, are for the edge detection. The eight ports labeled $D_{\rm out}$ (leftward, rightward, upward, and downward) and $D_{\rm in}$ (leftward, rightward, upward, and downward) are for the motion detection. In the pixel circuit, the photodiode accepts an incident image and generates the corresponding photocurrent. The photocurrent is amplified with gain α by the current amplifier. The amplified current is given to the current quantizer and the four nMOS transistors through port D. The spatial image smoothing is performed by the nMOS transistors connected with port D (the smoothing constant is determined by gate voltage $V_{\rm dif}$, which is common to all the nMOS transistors). The smoothed current is given to the current quantizer. The quantizer has four current output ports (B_1, B_2, B_3, and B_4), and all four output currents are equal. If the smoothed current is larger than a given threshold current ($I_{\rm th}$), the output current is produced, and if the smoothed current is smaller than the threshold

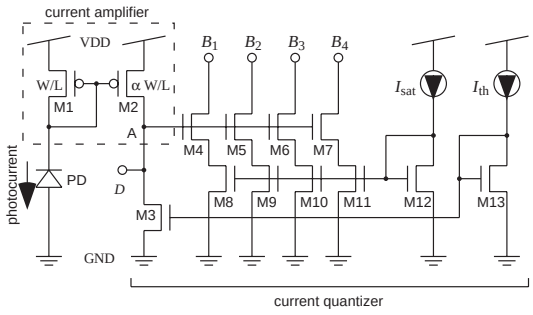

Fig.7 Current quantizer and amplifier

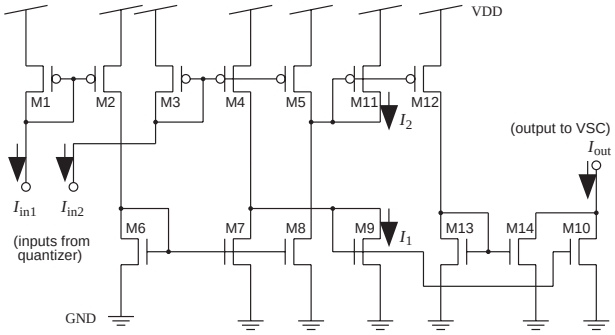

Fig.8 Current-mode XOR circuit

current, then the output current is zero. The output B_1 and B_2 of the quantizer are connected with two XOR circuits. The XOR circuits also receives local inputs $BX_{\rm in}$ and $BY_{\rm in}$ from the neighboring two pixel circuits. The XOR circuit receiving the $BX_{\rm in}$ (or $BY_{\rm in}$) and B_2 (or B_1) produces an exclusive-OR output that represents a vertical (or horizontal) edge. The output of XOR circuits (horizontal and vertical edges) are given to the four CCs. Each CC produces delayed signals $D_{\rm out}$ (leftward, rightward, upward, and downward) and send the signals to neighboring four pixel circuits and, at the same time, receives delayed signals $D_{\rm in}$ (leftward, rightward, upward, and downward) from the four neighbors. The CC receiving the neighboring $D_{\rm in}$ (leftward, rightward, upward, and downward) shows direction selectivity to the rightward, leftward, downward, and upward motion, respectively, as explained below.

The construction of the current amplifier and quantizer is shown in Fig. 7. The photocurrent is amplified by a current mirror (M1 and M2) with mirror rate α. The voltage on node A is nearly equal to 0 V (or VDD) if the photocurrent is smaller (or larger) than threshold $I_{\rm th}$. The voltage is then amplified by transistors M4 through M7. The output currents on port B_1, B_2, B_3, and B_4 are equal to each other and limited to $I_{\rm sat}$ by transistors M8 through M12. Thus, the circuit outputs zero currents (or $I_{\rm sat}$) if the input photocurrent is smaller (or larger) than $I_{\rm th}$.

For the XOR operation, the authors developed a current-mode digital logic circuit shown in Fig. 8. The circuit receives binary input currents $I_{\rm in1}$ and $I_{\rm in2}$ from the current quantizer (each current is 0 or $I_{\rm sat}$) . If $I_{\rm in1} = I_{\rm in2} = 0$, an output current of the circuit ($I_{\rm out}$) is 0 because no input currents are given to current mirrors in the circuit. If $I_{\rm in1} = 0$ and $I_{\rm in2} = I_{\rm sat}$, the current $I_{\rm in2}$ is copied into M4. The current of M4 is then copied into M9 ($I_1 = I_{\rm in2}$) and M10, so the output current ($I_{\rm out}$) is equal to $I_{\rm in2}$ ($= I_{\rm sat}$). If $I_{\rm in1} = I_{\rm sat}$ and $I_{\rm in2} = 0$, the current $I_{\rm in1}$ is copied into M11 ($I_2 = I_{\rm in1} = I_{\rm sat}$) through M2, M6, and M8. The current of M11 is copied into M14 through M12 and M13, so the output $I_{\rm out}$ is equal to $I_{\rm in1}$ ($= I_{\rm sat}$). If $I_{\rm in1} = I_{\rm in2} = I_{\rm sat}$, the output current ($I_{\rm out}$) is 0 because the current of M4 is equal to the current of M7 (therefore $I_1 = 0$) and the current of M5 is equal to the current of M8 (therefore $I_2 = 0$). In consequence, the circuit produces an exclusive OR output from binary input currents $I_{\rm in1}$ and $I_{\rm in2}$ (each is 0 or $I_{\rm sat}$).

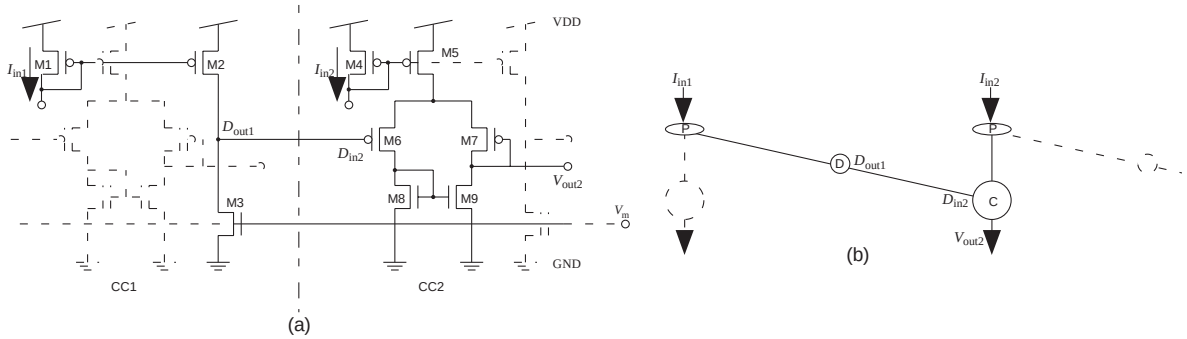

Fig.9 The correlation circuit (a) and corresponding one-dimentional unit network (b)

The correlation circuit CC corresponding to the one-dimensional CNN is shown in Fig. 9. The unit circuit, which is represented by solid lines in Fig. 9(a), consists of an unity gain amplifier (M5 through M9) and a pMOS common-source amplifier (M2 and M3). The unity gain amplifier and the pMOS common-source amplifier act as the correlator and the delay neuron, respectively, in the CNN [Fig. 9(b)]. When an input current $I_{\rm in1}$ larger than the current of M3, is applied to M1, a voltage output appears on node $D_{\rm out1}$ with a time delay caused by the Miller effect in the amplifier. The delay time can be externally controlled by adjusting common gate-voltage $V_{\rm m}$ for M3. A long (or short) delay is obtained for small (or large) values of $V_{\rm m}$. The source current of differential pair M6 and

M7 is determined by input current $I_{\rm in2}$ through current mirror M4 and M5. When the input current ($I_{\rm in2}$) is applied, the output voltage of the unity gain amplifier ($V_{\rm out2}$) is equal to the input voltage ($D_{\rm in2}$). When the input current approaches to 0, the value of $V_{\rm out2}$ also approaches to 0 V. Therefore the output voltage represents product-like value of those two inputs and, in consequence, the unity gain amplifier computes correlation-like value between the values of $I_{\rm in2}$ and $D_{\rm in2}$.

4 Simulation Results

In this section, we show SPICE simulation results for the proposed hybrid circuits. In the following simulations, we used a typical parameter set for all transistors, assuming a 1.2-μm CMOS process.

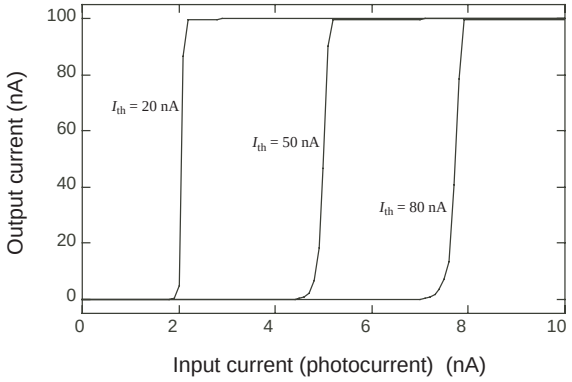

Fig.10 Static responses of the quantizer

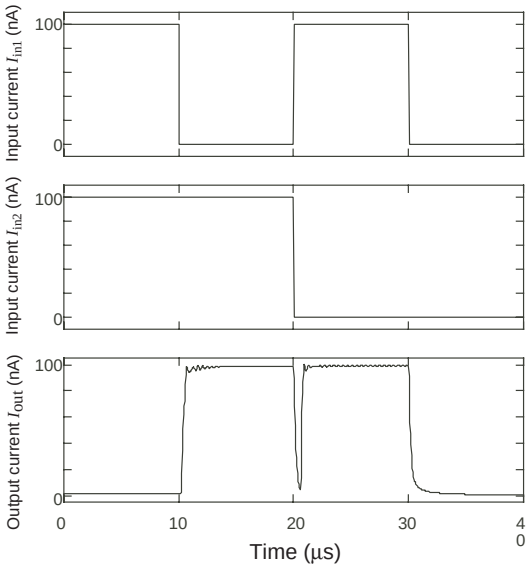

Fig.11 Transient responses of the XOR circuit

Figure 10 shows static responses of the current quantizer given in Fig. 7. The plotted output current is for output port B_1 in Fig. 7 (the outputs of B_2, B_3, and B_4 are equal in value to output B_1). In simulation, we assumed as: the supply voltage (VDD) is 3 V, the gain of current amplifier (α) is 10, the saturation current ($I_{\rm sat}$) is 100 nA, and the threshold current ($I_{\rm th}$) is 20 nA, 50 nA, and 80 nA. It was confirmed that the circuit successfully produced a quantized output in response to the input current (photocurrent).

The operation of the XOR circuit was also simulated and the result is shown in Fig. 11. Plotted are the waveforms of two input currents $I_{\rm in1}$ and $I_{\rm in2}$ and the corresponding output current. The output current was 0 when $I_{\rm in1} = I_{\rm in2}$ and 1 when $I_{\rm in1} \neq I_{\rm in2}$, so the expected XOR operation was obtained. A slight delay of a few microseconds was observed in the response, but this is not a problem in circuit operation.

Using two CCs connected to each other as shown in Fig. 9(a), we investigated transient responses of the CC network. The result is shown in Fig. 12 (the supply voltage and $V_{\rm m}$ were set at 3 V and 0.5 V, respectively). First, the input spot was applied to the CC1 [denoted by input current $I_{\rm in1}$ in Fig. 12(a)], and the corresponding delayed voltage ($D_{\rm out1}$) was produced [Fig. 12(b)]. Then the input spot was applied to CC2 (denoted by $I_{\rm in2}$ in the figure). From the delayed voltage $D_{\rm out1}$ and the applied input $I_{\rm in2}$, the CC2 calculated the correlation voltage $V_{\rm out2}$, which was approximately proportional to $I_{\rm in2} \times D_{\rm out1}$ as shown in the figure. When the spot moves at a constant velocity, a local velocity is represented by an inverse of the width of the input pulses. Therefore, the local velocity can be approximately obtained as an inverse value of the temporal integration of the correlation voltage.

We designed a prototype LSI, assuming a 1.2-μm double-poly double metal CMOS process. Figure 13 shows a layout pattern of the pixel circuits. Single pixel circuit occupied an area of only 220 μm $\times$ 290 μm including the area of the photodiode (40 μm $\times$ 40 μm). The resultant fill factor was approximately 3%.

5 Summary

Analog CMOS circuits for motion detection with asynchronous current-mode digital circuits was proposed for the development of practical motion-detection systems. The proposed circuits possesses the following merits: i) noises in input images can be eliminated by a current-mode digital quantizer, ii) in the analog correlation circuits,

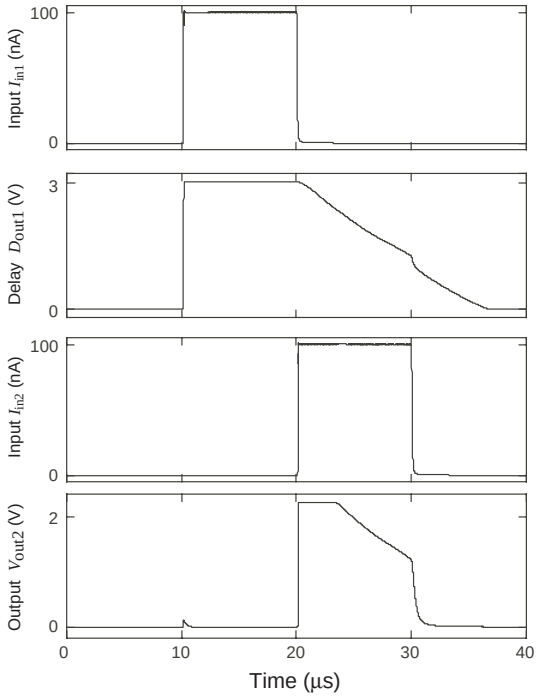

Fig.12 Transient responses of the CC network

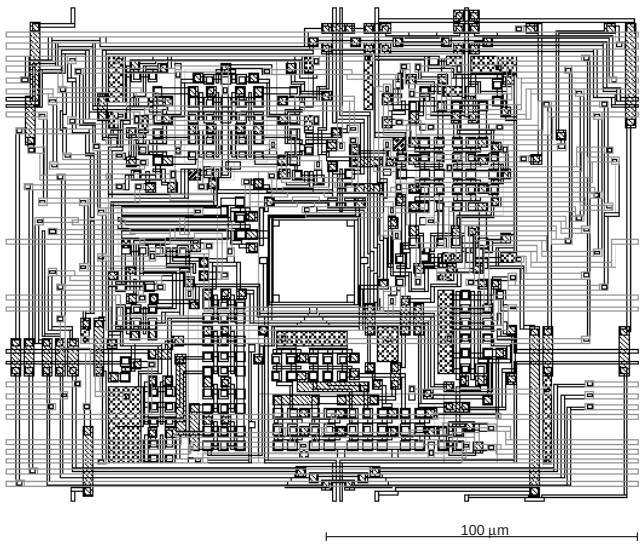

Fig.13 Layout pattern of the unit pixel circuit

a delayed signal, which is necessary to implement the biological motion detectors, is electrically produced without using large capacitances, iii) the asynchronous and subthreshold current-mode operations of the proposed digital and analog circuits make the total power dissipation very low, iv) local velocity signals are represented by voltage pulses, which makes subsequent analog-to-digital conversion very easy. The results of simulation indicated that the proposed circuits can compute two-dimensional local velocities with extracting edges of input images. By using the proposed circuits, we will be able to construct a high-speed motion-sensing chip with standard VLSI technology.

Acknowledgments

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