Frequency- and Temporal-Domain Neural Competition in Analog Integrate-and-Fire Neurochips

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Abstract - In this report, we present an inhibitory neural network implemented on analog CMOS chips, whose neurons compete with each other in the frequency and time domains. The circuit for each neuron was designed to produce sequences in time of identically shaped pulses, called *spikes*. The results of experiments and simulations revealed that the network more efficiently achieved the selective activation and inactivation of the neural circuits on the basis of spike timing than on the basis of firing rates. The results indicate that neural processing based on the spike timing of neural circuits provides a possible way to overcome the low-tolerance problems of analog devices in noisy environments.

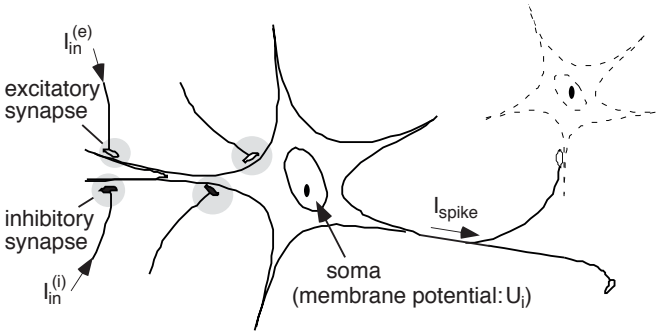

Fig. 1. Schematic image of the neuron model.

I. Introduction

Silicon circuits that mimic the nervous systems of insects and other animals represent the future of neurocomputing [1]. They incorporate various neural functions by replicating the microstructures of a nervous system (neural network) on a silicon chip. Analog VLSI is a key to the implementation of large-scale neural networks. However, traditional models of neurons and neural networks are not suitable for analog VLSI implementation due to the need for computational accuracy; i.e., analog devices have poor properties in terms of the matching and temperature dependence of device characteristics, and they have a low degree of tolerance to noisy environments. Therefore it is essential to improve precision and reproducibility at the device level by introducing redundancy at the hardware neural-network level.

Although the precision, reliability, and noise properties available in single neurons fall short of those in even the most rudimentary analog VLSIs, the nervous system exhibits marvelously accurate behavior. Recent physiological and theoretical studies support the possibility that accurate spike timing has a role in cortical processing [2]; e.g., constant stimuli lead to imprecise spike trains, whereas stimuli that include fluctuations produce spike trains with timing reproduced to within 1 millisecond [3]. The results indicate that a low level of intrinsic noise in spike generation allows cortical neurons to accurately transform a synaptic input into a sequence of spikes.

Fukai showed that a network of inhibitory integrate-and-fire neurons (IFNs) achieves a robust and efficient neural competition on the basis of a novel timing mechanism of neural activity [4]. We found that a network with such a timing mechanism provides an appropriate basis for the development of analog VLSI circuits that overcome the problems of analog devices, namely the lack of precision and reproducibility. In this report, we present a novel analog IFN circuit that can be implemented easily on analog VLSIs. We show, by both experiments and computer simulations, that a network of IFN circuits very efficiently achieves a robust form of neural competition that is based on spike timing rather than firing rates.

II. The IFN and Network Circuit

Figure 1 is a schematic image of a neuron model. The neuron accepts input currents, $I_{\rm in}^{(e)}$ and $I_{\rm in}^{(i)}$, through the excitatory and inhibitory synapses, respectively. When the input currents are integrated, the membrane potential U_i is produced at the soma. An excitatory input increases the membrane potential, whereas an inhibitory input decreases the potential. When the potential exceeds a threshold value, the neuron produces a current pulse $I_{\rm spike}$ and the membrane potential is reset to its resting value. This model is called the integrate-and-fire neuron (IFN) [5].

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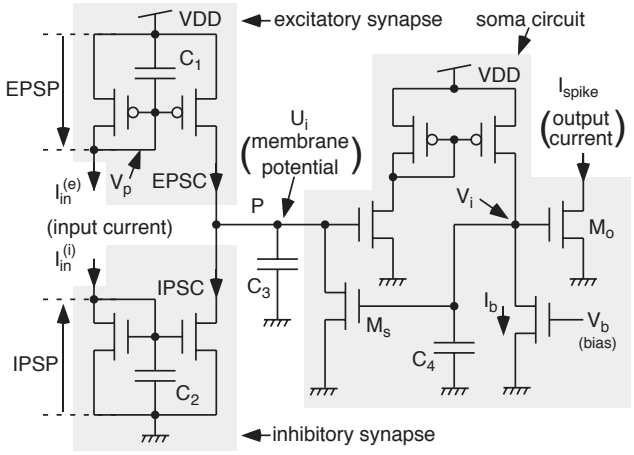

Fig. 2. The IFN circuit.

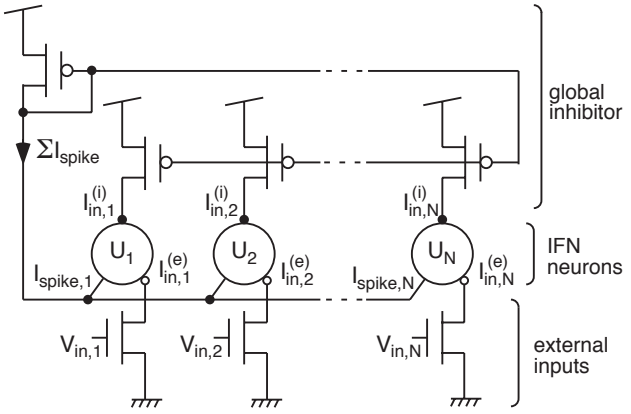

Fig. 3. Inhibitory neural circuits using IFNs.

Figure 2 shows an IFN circuit constructed of analog CMOS circuits. The circuit implements the excitatory and inhibitory synapses of the neuron model as well as the soma. The excitatory input current $I_{\rm in}^{(e)}$ produces the excitatory postsynaptic potential (EPSP) in the excitatory synapse circuit. The membrane potential U_i is thus increased by the excitatory postsynaptic current (EPSC) that is produced by the EPSP. Similarly, the inhibitory input $I_{\rm in}^{(i)}$ decreases the membrane potential through the inhibitory postsynaptic current (IPSC) that is produced by the inhibitory postsynaptic potential (IPSP). An increase in the membrane potential induces an increase in potential V_i. Thus, when the membrane potential exceeds a certain threshold voltage, input node P of the membrane is suddenly shunted by transistor M_s. The shunted current increases exponentially with the membrane potential. This sudden increase in the current represents the spike generation. The output current $I_{\rm spike}$ is

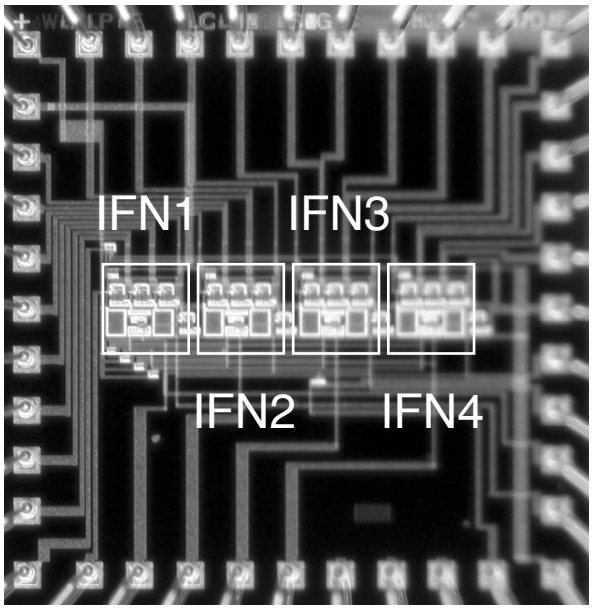

Fig. 4. Micrograph of the fabricated IFN chip.

obtained by transistor M_o.

The input current $I_{\rm in}$ and bias current I_b for the circuit determine the magnitude of the spike and the duration of the refractory period. If both the input current and the bias current are less than 100 nA, the MOS transistors of the IFN circuit operate in their subthreshold region [6], where the IFN circuit consumes very little power (on the order of 1 nW or less) but where the MOS transistors are very sensitive to external noise. We are interested in whether or not the IFN network is able to overcome this noise sensitivity.

We constructed an inhibitory neural network in which the IFN circuits are coupled to each other through all-to-all inhibitory connections of equal strength. This coupling reduces the complexity of the connection of N neurons to $O(N)$. Figure 3 shows the reduced network consisting of N IFN circuits and a global inhibitor constructed of $(N+1)$ pMOS transistors. Each IFN circuit accepts an intrinsic external input $V_{\rm in}$. The nMOS transistors connected to the IFN circuits produce an excitatory input current $I_{\rm in}^{(e)}$. The global inhibitor receives the sum of the IFN outputs ($\sum_i^N I_{{\rm spike},i}$). This total current is copied in each IFN circuit to produce the inhibitory input current $I_{\rm in}^{(i)}$.

III. Results

We fabricated a prototype IFN chip using a 1.5 μm CMOS process (MOSIS, vendor: AMI). Figure 4 is a photograph of the chip, which contains four IFN circuits

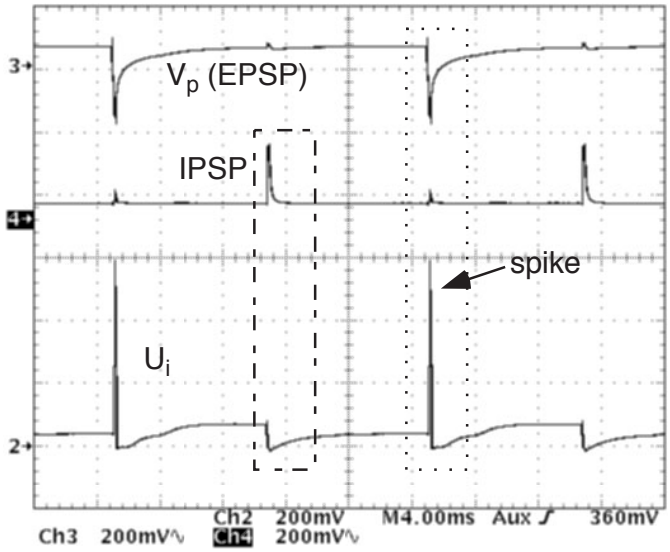

Fig. 5. Experimental results for the IFN circuit

and one global inhibitor circuit. The capacitors C_1, C_2, C_3, and C_4 were designed with a large capacitance due to the limit on the time resolution of our measurement systems. The capacitors took up a total area of 120 μm $\times$ 200 μm.

Figure 5 shows experimental results for the fabricated IFN circuit. The supply voltage was set at 5 V, and the bias current I_b was set at 100 nA. In the experiment, periodic current pulses were applied to the excitatory and inhibitory synapse circuits. When an input pulse was applied to the inhibitory synapse circuit, the membrane potential U_i was decreased by the increase in the IPSP (see box outlined by dashes in Fig. 5). Similarly, the membrane potential was increased by the input pulse applied to the excitatory synapse circuit. When the IPSP fell below a certain threshold voltage, a spike was generated (box outlined by dots in Fig. 5) because of the reduction of the shunting inhibition by the IPSC. The spike current I_{spike} ($\approx$100 nA) was five orders of magnitude larger than the resting current ($\approx$1 pA), and these two are thus very easily distinguished from each other.

Figure 6 shows experimental results for a four-neuron network. In these experiments, external input values were encoded as either firing rate or spike timing. Encoding of the external input as a firing rate means that the strength of the external input is equivalent to the frequency of the train of identically shaped voltage pulses V_{in}. Encoding of the external input as spike-timing code means that the strength is equivalent to the timing of spike generation relative to the timing of its external periodic input.

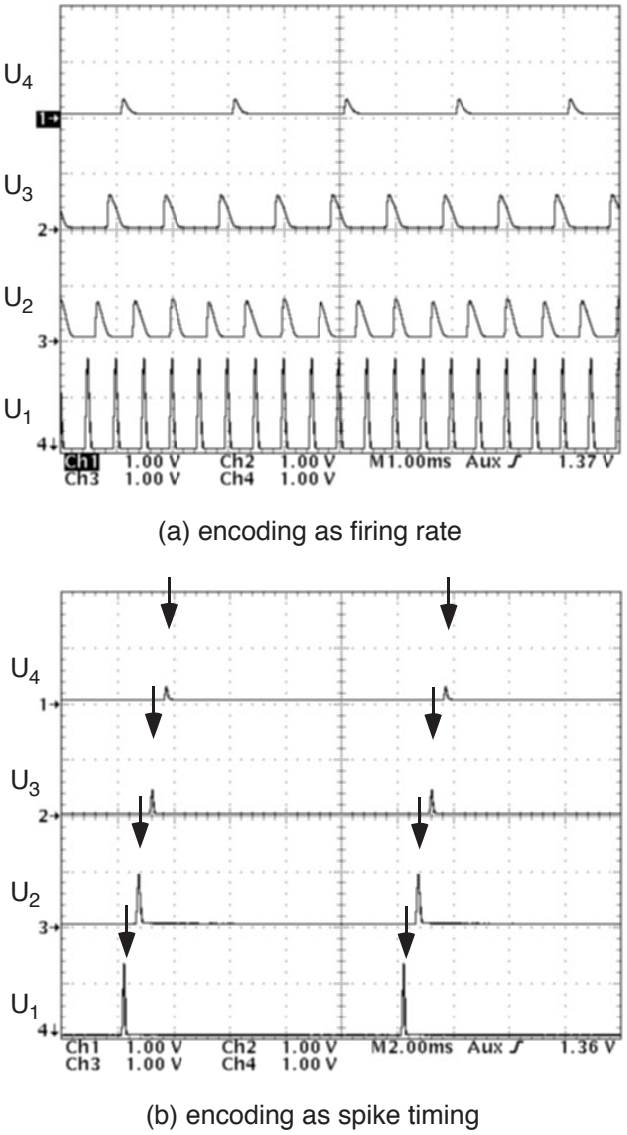

Fig. 6. Experimental results for the four-IFN network.

The results for a firing rate encoded input are shown in Fig. 6(a). The amplitudes of the input current pulses $|I_{\text{in}}^{(e)}|$ were fixed at 100 nA. The frequencies of four periodic pulses $I_{\text{in},1}^{(e)}$; $I_{\text{in},2}^{(e)}$; $I_{\text{in},3}^{(e)}$; and $I_{\text{in},4}^{(e)}$ were set at 200 kHz, 150 kHz, 100 kHz, and 50 kHz, respectively. Because an IFN circuit inhibits each other through the global inhibitor, an IFN receiving high-frequency input remained active, while those receiving low-frequency inputs became inactive.

When inputs encoded as spike timings were applied to the same network, the network exhibited a qualitatively quite different behavior, as shown in Fig. 6(b). Here, the external input values are transformed into the initial

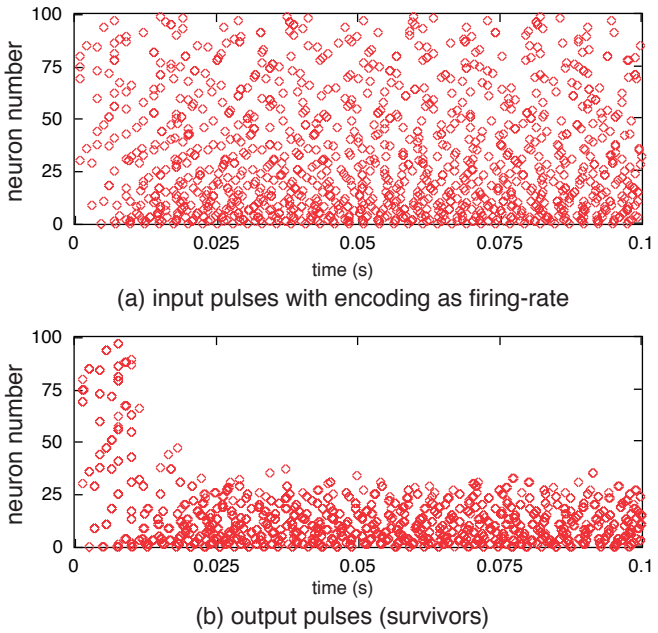

Fig. 7. Results of simulation of a 100-IFN network (firing-rate encoding).

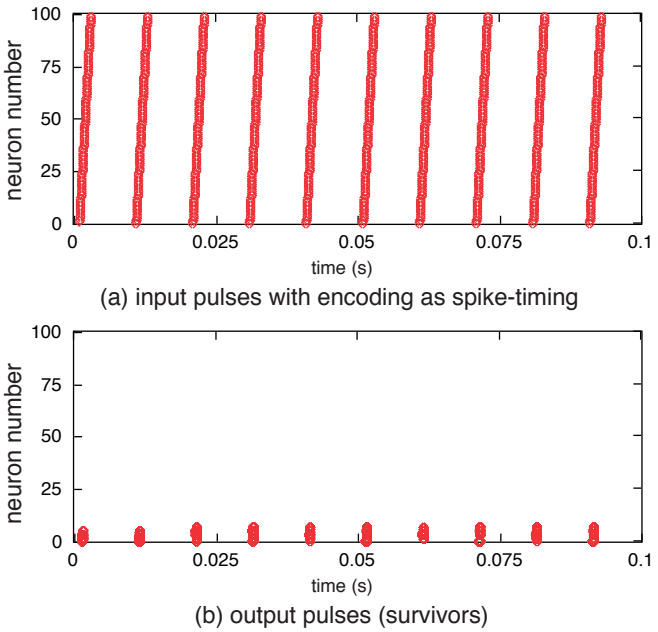

Fig. 8. Results of simulation of a 100-IFN network (spike-timing encoding).

delay times of the periodic input pulses. In Fig. 6(b), the arrows show the timing at which each IFN received the input pulse. From this, it can be seen that competition occurred in terms of the times at which the input pulse reached the individual IFNs. This phenomena ("first come, first served" or "early arrival matters") simply comes from the refractory period of the IFN circuits and lateral inhibition.

The next area of interest was the behavior of a large-scale IFN network in terms of improving its noise tolerance. It is rather difficult to construct a large-scale network of our prototype chips, because each chip includes only four IFN circuits. Therefore, we conducted SPICE simulations of a large-scale network, using device parameters obtained from the chip we fabricated.

Figure 7 shows typical results obtained from the simulation of a 100-IFN network with firing-rate encoding. In the figure, the IFNs are represented by neuron numbers, labeled from 0 to 99. Each neuron receives input pulses with an amplitude of 10 nA at a timing represented by one of the circles in Fig. 7(a). The bias current I_b was set at 1 nA, while capacitors C_1, C_2, C_3, and C_4 were set at 1 pF, 10 pF, 10 pF, and 1 pF, respectively. Each circle in Fig. 7(b) represents the timing at which the i-th IFN circuit generated a spiking output I_{spike} of amplitude greater than 4.5 nA. As expected, those IFNs receiving high-frequency inputs remained active, while those receiving low-frequency inputs became inactive.

The reaction of the same network to spike timing was also simulated. Figure 8(a) shows the inputs with encoding as the spike timing. Those IFNs labeled by small numbers receive early input pulses, while those IFNs labeled with large numbers receive later input pulses. In this experiment, the first seven IFN circuits exhibited steady periodic responses, as can be seen in Fig. 8(b).

Figure 9 shows the results of a simulation in which the same network as was used to produce Fig. 8 was exposed to a noisy periodic input. The amplitude of the noise was set at 2 nA, and its frequency was set at one-half to one-sixth of the periodic input. Six of the seven survivors shown in Fig. 8 ceased to exhibit steady periodic responses, while some of the losers in the process of competition fired occasionally. Only the first survivor showed a steady periodic response to the input. When the amplitude of the noise was set at 1 nA, the seven neurons that had survived in Fig. 8 exhibited steady periodic responses, whereas none of the losers fired. Although the amplitude of the noise is close to the order of the amplitude of the periodic input, the noise did not affect the activity of survivors that were distant from the border of losers. That is, an IFN receiving an input pulse earlier in each oscillatory cycle had a higher probability of firing than one receiving a pulse later in each oscillatory cycle. This implies that noise does *not* affect the essential features of the timing mechanism.

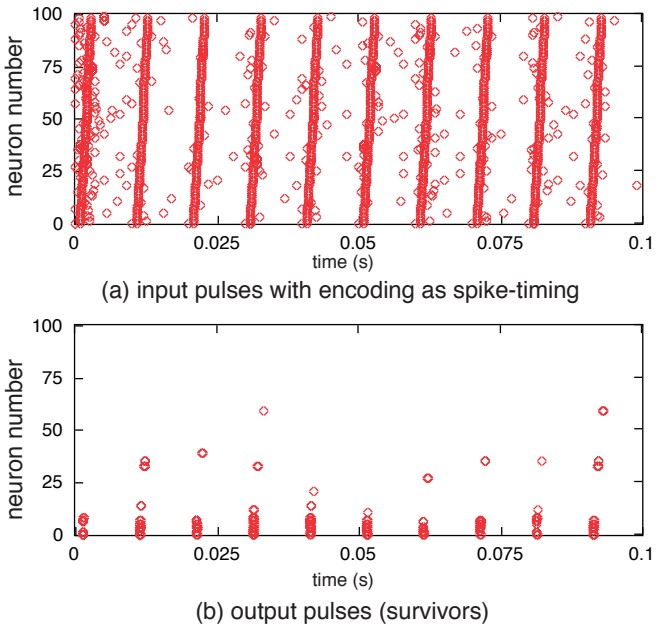

Fig. 9. Results of simulation of a 100-IFN network with noise (spike-timing encoding).

IV. Summary

We have proposed and fabricated a simple integrate-and-fire neuron (IFN) circuit and an inhibitory neural network consisting of a small number of IFN circuits. The IFN circuit is designed to produce sequences of spikes in time according to the strengths of the signals on its inhibitory and excitatory inputs. Results of experiments and simulations revealed that the IFN circuits of the network exhibited competitive behavior in the frequency and time domains. The frequency-domain competition was achieved by introducing analog inputs that carried encoding in the form of the frequency of the firing rate, while competition in the time domain was achieved by having inputs that carried encoding in the form of the timing of spikes.

In the case of spike-timing encoding, an IFN circuit becomes a loser if it remains inactive or ceases to fire within several oscillatory cycles of the onset of the train of input pulses. Survivors exhibit steady periodic responses, while losers exhibit no activity. The distinction between survivors and losers is thus obvious from the spiking activity in the time of the IFNs.

In the case of firing-rate encoding, however, the distinction is not very obvious from the activity in time. To determine the precise result of selection for activity or inactivity, mean firing rates of activities must be recovered for a sufficiently long time. If a short time interval is used for averaging, the obtained firing rates do not reflect the relative intensity of the stimuli. Thus the responses of survivors do not, in general, represent the precise order of the stimuli. These observations lead us to conclude that the interpretation of the results is immediate and clear for spike-timing encoding, but is time-consuming and ambiguous in the case of firing-rate encoding.

Acknowledgement

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