Neuromorphic CMOS Circuits implementing a Novel Neural Segmentation Model based on Symmetric STDP Learning

Gessyca Maria Tovar, Eric Shun Fukuda, Tetsuya Asai, Tetsuya Hirose and Yoshihito Amemiya

***Abstract*— We designed a simple neural segmentation model that is suitable for analog circuit implementation. The model consists of excitable neural oscillators and adaptive synapses, where the learning is governed by a symmetric spike-timing dependent plasticity (STDP). We numerically demonstrate basic operations of the proposed model as well as fundamental circuit operations using a simulation program with integrated circuit emphasis (SPICE).**

I. Introduction

Humans can distinguish multiple sensory sources that coincide. Recent discoveries of synchronous oscillations in the visual and auditory cortex have triggered much interest in exploring oscillatory correlation to solve the problems of neural segmentation. Many neural models that perform segmentation have been proposed, e.g., [1], [2], [3], but they are often difficult to implement on practical integrated circuits. Recently, a neural segmentation model called LEGION (Locally Excitatory Globally Inhibitory Oscillator Networks) [4] has been attracting attention because it is easy to implement on circuits. However, not including learning of neurons, under certain conditions the LEGION model does not work. In this paper, we present a simple neural segmentation model that is suitable for analog complementary metal-oxide-semiconductor (CMOS) circuits and that includes learning.

The segmentation model is suitable for applications such as figure-ground segmentation and the cocktail-party effect, among others. The model consists of mutually coupled neural oscillators exhibiting synchronous (or asynchronous) oscillations. All the neurons are coupled with each other through positive or negative synaptic connections. Each neuron accepts external inputs, e.g., sound inputs in the frequency domain, and oscillates (or does not oscillate) when the input amplitude is higher (or lower) than a given threshold value. Our basic idea is to strengthen (or weaken) the synaptic weights between synchronous (or asynchronous) neurons, which may result in phase-domain segmentation. The synaptic weights are updated based on symmetric spike-timing dependent plasticity (STDP) using Reichardt's correlation neural network [5] which is suitable for analog CMOS implementation.

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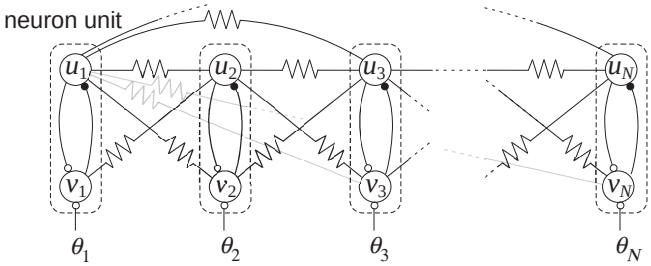

Fig. 1. Network construction of segmentation model.

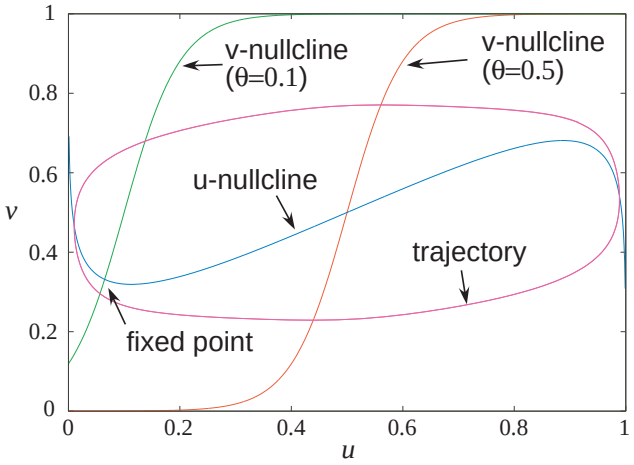

Fig. 2. Nullclines and trajectories of single neural oscillator.

In the following sections, we introduce our segmentation model and demonstrate the operations through numerical simulations. Then we present unit CMOS circuits for our model and demonstrate the operations using a simulation program with integrated circuit emphasis (SPICE).

II. The Model and Basic Operations

Our segmentation model is illustrated in Fig. 1. The network has N neural oscillators consisting of the Wilson-Cowan type activator and inhibitor pairs (u_i and v_i) [6]. All the oscillators are coupled with each other through resistive synaptic connections, as illustrated in the figure. The dynamics are defined by

$$\tau \frac{du_i}{dt} = -u_i + f_{\beta_1}(u_i - v_i) + \sum_{j \neq i}^{N} W_{ij}^{\mathrm{uu}} u_j, \qquad (1)$$

$$\frac{dv_i}{dt} = -v_i + f_{\beta_2}(u_i - \theta_i) + \sum_{j \neq i}^{N} W_{ij}^{\mathrm{uv}} u_j, \qquad (2)$$

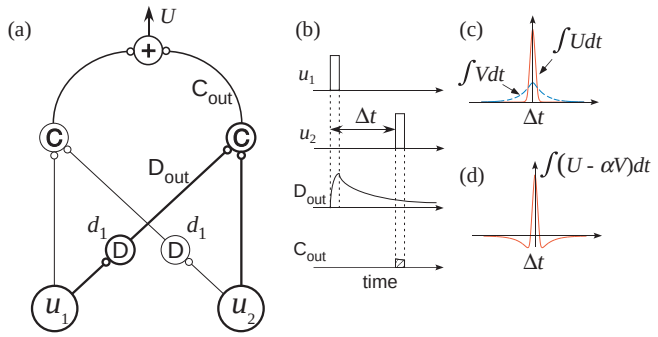

Fig. 3. Reichardt's correlation neural network.

where τ represents the time constant, N the number of oscillators, θ_i the external input to the i-th oscillator. $f_{\beta_i}(x)$ represents the sigmoid function defined by $f_{\beta_i}(x) = [1 + \tanh(\beta_i x)]/2$, $W_{ij}^{\rm uu}$ the connection strength between the i-th and j-th activators and $W_{ij}^{\rm uv}$ the strength between the i-th activator, and the j-th inhibitor. The nullclines of a single oscillator ($W_{ij}^{\rm uu} = W_{ij}^{\rm uv} = 0$) for different θs (0.1 and 0.5) and trajectories for $\theta = 0.5$ are shown in Fig. 2. The rest of the parameters were set at $\tau = 0.1$, $\beta_1 = 5$ and $\beta_2 = 10$. Models whose dynamics are described by Eqs. (1) and (2), are suitable for implementation in analog VLSIs becuase the sigmoid function can be implemented in VLSIs by using differential-pair circuits.

According to the stability analysis in [6], the i-th oscillator exhibits excitable behaviors when $\theta_i < \Theta$ where $\tau \ll 1$ and $\beta_1 = \beta_2$ ($\equiv \beta$), where Θ is given by

$$\begin{aligned} \Theta &= u_0 - \frac{2}{\beta}\tanh^{-1}(2v_0 - 1), \qquad (3)\\ u_0 &\equiv \frac{1-\sqrt{1-4/\beta}}{2},\\ v_0 &\equiv u_0 - \frac{2}{\beta}\tanh^{-1}(2u_0 - 1), \end{aligned}$$

and exhibits oscillatory behaviors when $\theta_i \geq \Theta$, if $W_{ij}^{\rm uu}$ and $W_{ij}^{\rm uv}$ for all i and j are zero.

Suppose that neurons are oscillating ($\theta_i \geq \Theta$ for all i) with different initial phases. The easiest way to segment these neurons is to connect the activators belonging to the same (or different) group with positive (or negative) synaptic weights. In practical hardware, however, the corresponding neuron devices have to be connected by special devices having both positive and negative resistive properties, which prevents us from designing practical analog circuits. Therefore, we simply use positive synaptic weights between activators and inhibitors, and do not use negative weights. When the weight between the i-th and j-th activators ($W_{ij}^{\rm uu}$) is positive and $W_{ij}^{\rm uv}$ is zero, the i-th and j-th activators will be synchronized. Contrarily, when the weight between the i-th activator and the j-th inhibitor ($W_{ij}^{\rm uv}$) is positive and $W_{ij}^{\rm uu}$ is zero, the i-th and j-th activators will exhibit asynchronous oscillation because the j-th inhibitor (synchronous to the i-th activator) inhibits the j-th activator.

The synaptic weights ($W_{ij}^{\rm uu}$ and $W_{ij}^{\rm uv}$) are updated based on our assumption; one neural segment is represented by synchronous neurons, and is asynchronous with respect to neurons in the other segment. In other words, neurons should be correlated (or anti-correlated) if they received synchronous (or asynchronous) inputs. These correlation values can easily be calculated by using Reichardt's correlation neural network [5] which is suitable for analog circuit implementation [7]. The basic unit is illustrated by thick lines and circles in Fig. 3(a). It consists of a delay neuron (D) and a correlator (C). A delay neuron produces blurred (delayed) output $D_{\rm out}$ from spikes produced by activator u_1. The dynamics are given by

$$d_1 \frac{dD_{\rm out}}{dt} = -D_{\rm out} + u_1, \qquad (4)$$

where d_1 represents the time constant. The correlator accepts $D_{\rm out}$ and spikes produced by activator u_2 and outputs $C_{\rm out} = D_{\rm out} \times u_2$. The conceptual operation is illustrated in Fig. 3(b). Note that $C_{\rm out}$ qualitatively represents correlation values between activators u_1 and u_2 because $C_{\rm out}$ is decreased (or increased) when Δt, inter-spike intervals of the activators, is increased (or decreased). Since this basic unit can calculate correlation values only for positive Δt, we use two basic units, which we call a unit pair, as shown in Fig. 3(a). The output (U) is thus obtained for both positive and negative Δt by summing the two $C_{\rm out}$s. Through temporal integration of U, we obtain impulse responses of this unit pair. The sharpness is increases as $d_1 \to 0$. Two impulse responses for small and large d_1 (red and blue curves) are plotted in Fig. 3(c). Introducing two unit pairs with different time constants, i.e., d_1 and d_2 ($\gg d_1$), one can obtain those two impulse responses (U and V) simultaneously. The weighted subtraction ($U - \alpha V$) produces well-known Mexican hat characteristics, as shown in Fig. 3(d). We use this symmetric characteristic for the weight updating as a spike-timing dependent plasticity (STDP) in the oscillator network.

A schematic of our learning circuitry is shown in Fig. 4. The two unit pairs are located between two activators u_1 and u_2. The weighted subtraction ($U - \alpha V$) is performed by interneuron W. According to our above assumptions for neural segmentation, when $U - \alpha V$ is positive, the weight between activators u_1 and u_2 (illustrated by a horizontal resistor symbol in Fig. 4) is increased because the activators should be correlated. On the other hand, when $U - \alpha V$ is negative, the weight between activator u_1 and inhibitor v_2 (illustrated by a slant resistor symbol in Fig. 4) is increased because activators u_1 and u_2 should be anti-correlated. To this end, the output of interneuron W is given to two additional interneurons ($f_{\rm uu}$ and $f_{\rm uv}$). The input-output characteristics of these interneurons are shown in Figs. 4(a) and (b). Namely, $f_{\rm uu}$ (or $f_{\rm uv}$) increases linearly when positive (or negative) $U - \alpha V$ increases, but is zero when $U - \alpha V$ is negative (or positive). Those positive outputs ($f_{\rm uu}$ and $f_{\rm uv}$) are given to the weight circuit to modify the positive resistances. The dynamics of the "positive" weight between activators u_i and

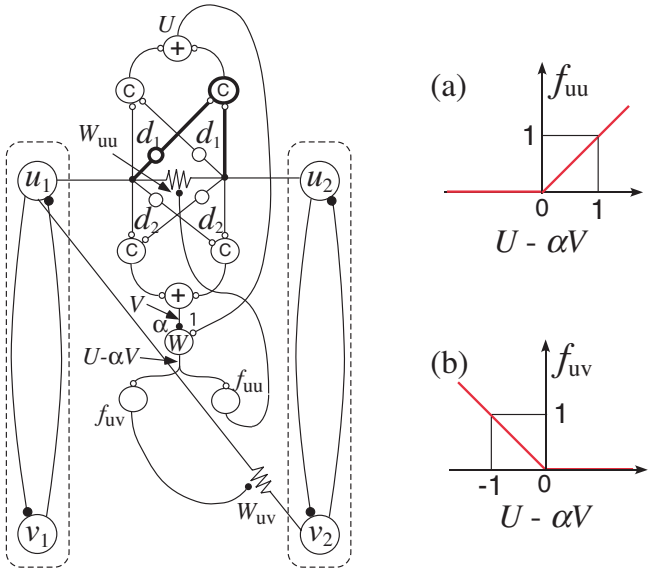

Fig. 4. STDP learning circuitry.

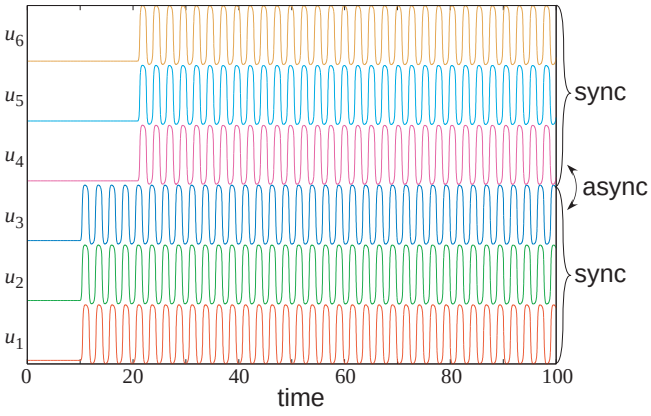

Fig. 5. Numerical simulation results.

u_j is given by

$$\frac{dW_{ij}^{\mathrm{uu}}}{dt} = -W_{ij}^{\mathrm{uu}} + f_{\mathrm{uu}}, \tag{5}$$

and the "positive" weight between activator u_i and inhibitor v_j is

$$\frac{dW_{ij}^{\mathrm{uv}}}{dt} = -W_{ij}^{\mathrm{uv}} + f_{\mathrm{uv}}. \tag{6}$$

We carried out numerical simulations with $N = 6$, $\tau = 0.1$, $\beta_1 = 5$, $\beta_2 = 10$, $d_1 = 2$, $d_2 = 0.1$ and $\alpha = 1.2$. Time courses of activators u_i $(i = 1 \sim 6)$ are shown in Fig. 5. Initially, the external inputs θ_i $(i = 1 \sim 6)$ were zero $(< \Theta)$, but θ_i for $i = 1 \sim 3$ and $i = 4 \sim 6$ were increased to 0.5 $(> \Theta)$ at $t = 10$ s and 20.9 s, respectively. We observed that $u_{1\sim3}$ and $u_{4\sim6}$ were gradually desynchronized without breaking synchronization amongst neurons in the same group, which indicated that segmentation of neurons based on the input timing was successfully achieved.

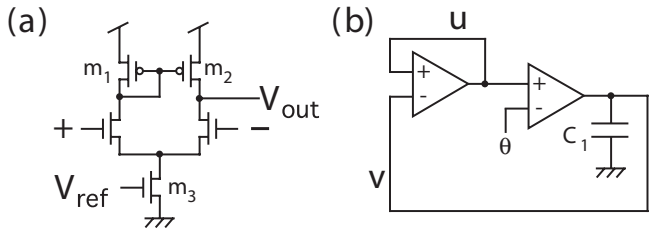

Fig. 6. Unit circuits for neural segmentation; (a) differential amplifiers and (b) neural oscillator

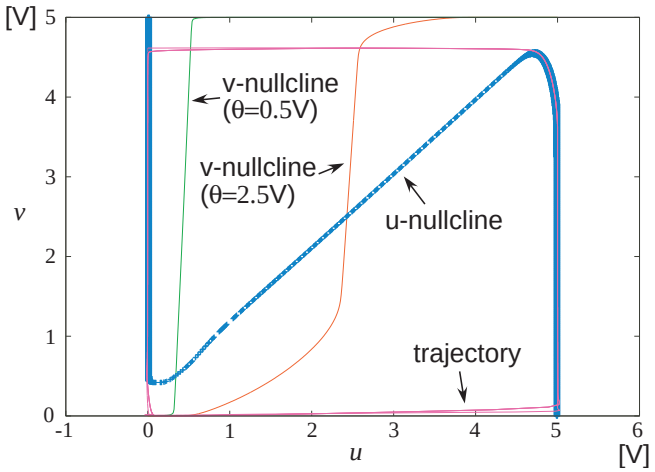

Fig. 7. Nullclines and trajectory for $\theta = 2.5$ V obtained from circuit simulations.

III. CMOS UNIT CIRCUITS AND OPERATIONS

Our Wilson-Cowan based neural oscillators have been implemented in [6]. The oscillator uses standard differential amplifiers shown in Fig. 6(a) which consists of a differential pair (+ and -), a current mirror (m_1 and m_2) and a bias transistor (m_3). The construction of an entire neural oscillator including additional capacitor C_1 is illustrated in Fig. 6(b). The simulated nullclines of a single neuron circuit for different θs (0.5 V and 2.5 V) and trajectories for $\theta = 2.5$ V with $C_1 = 10$ pF and $V_{\mathrm{ref}} = 2$ V are shown in Fig. 7. Transient simulation results of the neuron circuit are shown in Fig. 8. Time courses of the activator unit (u) are shown. Initially, θ was set at 0.5 V (in relaxing state), and u did not oscillate. Then θ was increased to 2.5 V at t = 0.1 ms, and u exhibited stiff oscillations. Again, θ was set at 0.5 V at t = 0.3 ms. Since u had been excited before this time, the neuron emitted one spike and then relaxed, as expected.

A circuit implementing Reichardt's basic unit shown in Fig. 3(a) is shown in Fig. 9. For practical purposes, we added two limiters that convert voltage pulses of u_1 and u_2, which vary from 0 to V_{dd}, into subthreshold current pulses. Bias current I_1 drives m_4 and m_5. Transistor m_6 is thus biased to generate I_1 because m_4 and m_6 share the gates. When m_7 is turned on (or off) by applying V_{dd} (or 0) to u_1, I_1 is (or is not) copied to m_8. Transistors m_8 and m_9 form a current mirror, whereas m_9 and m_{10} form

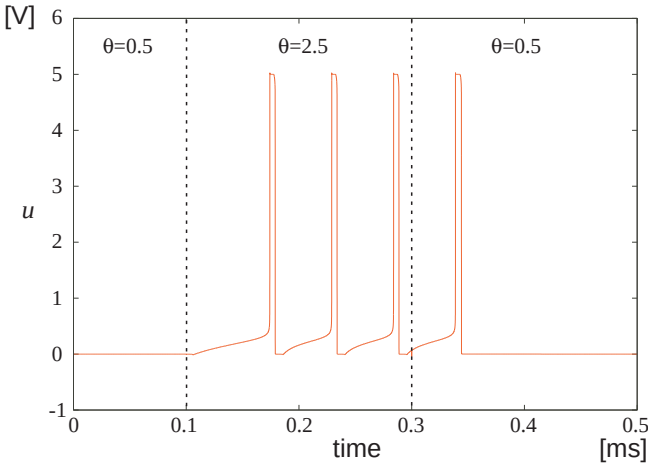

Fig. 8. Simulation results of neural oscillator.

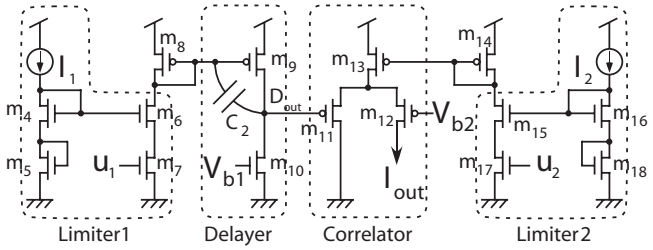

Fig. 9. STDP circuit.

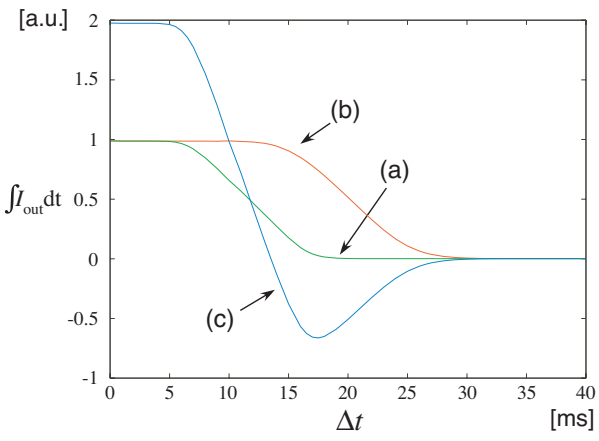

Fig. 10. Ideal STDP characteristics without limiters.

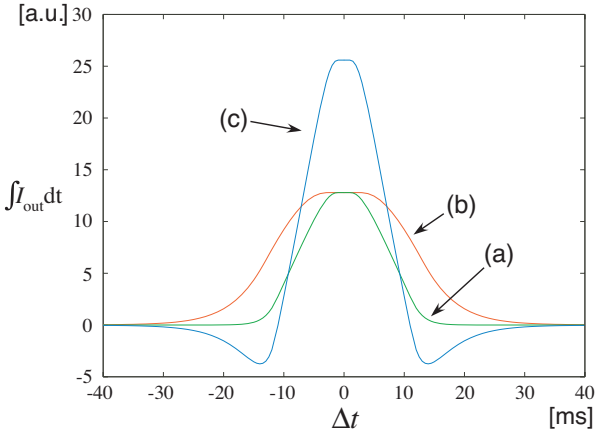

Fig. 11. Symmetric STDP characteristics with limiters.

a pMOS source-common (inverting) amplifier whose gain is increased as $V_{\rm b1} \rightarrow 0$. Since parasitic capacitance C_2 is significantly amplified by this amplifier, temporal changes of u_1 are blurred on the amplifier's output ($D_{\rm out}$). Therefore this "delayer" acts as a delay neuron in Fig. 3(a). A correlator circuit consists of a pMOS differential pair ($\rm m_{11}$ and $\rm m_{12}$) and a bias transistor ($\rm m_{13}$). When $u_2 = V_{\rm dd}$ (or zero), I_2 is (or is not) copied to $\rm m_{13}$ through $\rm m_{15}$ to $\rm m_{18}$, as explained above. Therefore, output current $I_{\rm out}$ is obtained only when $u_2 = V_{\rm dd}$. Under this condition, $I_{\rm out}$ is proportional to $D_{\rm out} - V_{\rm b2}$ for small $|D_{\rm out} - V_{\rm b2}|$. This operation corresponds to that of a correlator in Fig. 3(a).

We carried out circuit simulations of the above circuits. The parameter sets we used for the transistors were obtained from MOSIS AMIS 1.5-μm CMOS process. Transistor sizes of $\rm m_1$, $\rm m_2$, $\rm m_3$, $\rm m_{13}$ and $\rm m_{14}$ were fixed at $L = 16$ μm and $W = 4$ μm to construct accurate current mirrors. Sizes of the resting transistors were set at $L = 1.6$ μm and $W = 4$ μm. The supply voltage was set at 5 V.

Simulation results of our STDP circuits are shown in Figs. 10 and 11. In Fig. 10, ideal current pulses (amplitude: 100 nA, pulse width: 10 ms) were used instead of limiters as shown in Fig. 9. Parameters C_2, V_{b1} and V_{b2} were set at 100 fF, -0.2 V and 3.7 V, respectively. The value of V_{b2} was set at the intermediate value between m_{11}'s maximum and minimum gate voltage, and this makes the differential pair's output vary the most. The value of V_{b1} was chosen so that the delayer makes a reasonable delay. Horizontal axes (Δt) in Figs. 10 and 11 represent time intervals of input current pulses (spikes). We integrated $I_{\rm out}$ during the simulation and plotted normalized values [(a) in Fig. 10]. Then we changed the value of V_{b_1} to -2 V. The lowered V_{b1} reduced the drain current of $\rm m_{10}$ and made the delay larger. Again, $I_{\rm out}$ was integrated and normalized. The result is plotted [(b) in Fig. 10]. Larger delay made the integrated $I_{\rm out}$ converge to zero at a larger Δt. By subtracting (b) from tripled (a), we obtained half characteristics of STDP learning (c) in Fig. 10. In Fig. 11, voltage pulses (amplitude: 5 V, pulse width: 10 ms) were applied to u_1 and u_2 in Fig. 9. Parameters C_2 and V_{b2} were set at 5 pF and 3.7 V, respectively. The integrated $I_{\rm out}$s were plotted in Fig. 11(a) for $V_{b1} = 0$ and Fig. 11(b) for $V_{b1} = -0.04$ V. The result was qualitatively equivalent to the STDP characteristics shown in Fig. 3(d).

IV. Conclusion

In this paper, we proposed a simple neural segmentation model that is suitable for analog CMOS implementation. First, instead of employing negative weights required for anti-correlated oscillation among different segments, we in-

troduced positive connections between activators and inhibitors among different neuron units. Second, we proposed a novel segmentation method based on a symmetric spike-timing dependent plasticity (STDP). The STDP characteristics were produced by combining Reichard's correlation neural networks that are suitable for analog CMOS implementation. The proposed segmentation network was demonstrated through numerical simulations. Basic circuits for constructing segmentation hardware were proposed and evaluated. We showed that our circuit could produce symmetric STDP characteristics. Our next target is to setup the entire segmentation network with the proposed circuits.

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