Analog CMOS Implementation of a Bursting Oscillator with Depressing Synapse

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Abstract

The present paper proposes an analog CMOS circuit that implements a bursting oscillator with a depressing synapse. Bursting oscillation arises the result of interaction between a fast excitatory subsystem and a slow subsystem. We employ an analog circuit, called the hardware Oregonator, for emulating the Belousov-Zhabotinsky reaction as a fast subsystem and an additional circuit as a slow subsystem. We constructed a bursting oscillator circuit from two bursting cell circuit based on the hardware Oregonator with a depressing synaptic circuit. Using the simulation on program with integrated circuit emphasis (SPICE), we demonstrate that the circuit shows bursting oscillations and the bursting frequency can be regulated by tuning the depressing synapse circuit.

1. INTRODUCTION

Bursting activities are often observed in neural systems at both the single cell level and the network level. In central pattern generators (CPGs) that are neural networks responsible for generating rhythmic behaviors, bursting oscillations arise from the interactions of bursting neurons [1]. Recently, it is suggested that short-term synaptic plasticity plays critical roles in such bursting oscillations in CPGs [3]-[5]. Nadim and his colleagues proposed computational models of CPGs with depressing syapse, which is a form of short-term synaptic plasticity, inspired by experimental results of the pyloric CPG of the lobster [3]-[5]. In their models, depressing synapses mediate bistability [3] and promote phase invariance [4], and regulate the frequency of bursting oscillations in CPGs [5].

In neuromorphic engineering, the output pathways of neural systems, such as CPG, have attracted much attention as well as sensory perception, recognition, and learning. Many neuromorphic engineers designed and fabricated analog CPG chips [7]-[9]. Most of these chips are difficult to regulate the operation speed because it is determined by circuit parameters physically. Focusing on the roles of the short-term synaptic plasticity in CPGs, we propose analog CMOS circuit that implements a bursting oscillator with depressing synapse. The proposed circuit is constructed form two oscillatory circuits, called the hardware Oregonator [10], and a depressing synapse circuit [11]. Using the simulation on program with integrated circuit emphasis (SPICE), we demonstrate that the circuit shows bursting oscillations and the bursting frequency can be regulated by tuning circuit parameters in the depressing synapse circuit.

2. BURSTING OSCILLATOR MODEL

We here propose a bursting oscillator model with depressing synapse for analog CMOS circuit implementation.

A. Bursting Cell Model based on the Hardware Oregonator

Bursting oscillation arises as a result of the interaction between a fast excitatory subsystem and a slow subsystem [2]. The fast excitatory subsystem has two different time-scales, i.e., it itself is a slow-fast system. As a slow-fast system, we considered the following system [2]:

$$\frac{du}{dt} = \frac{1}{\tau}\left(-u + f(u - v, \beta_u)\right) \quad (1)$$

$$\frac{du}{dt} = -v + f(u - \theta, \beta_v) \quad (2)$$

where u and v represent state variables, τ a time constant, and θ a threshold. The nonlinear function $f(x, \beta)$ is given by a sigmoid function defined by:

$$f(x, \beta) = \frac{1 + \tanh(\beta x)}{2} \quad (3)$$

where $\tanh(\beta x)$ is the hypobolic tangent function, and β is a gain parameter. This system has originally been proposed for implementing the Oregonator model for the Belousov-Zhabotinsky (BZ) reaction system, a reaction-diffusion (RD) system, on silicon chips. Thus, the system is called the hardware Oregonator model [10].

The hardware Oregonator model has qualitatively similar dynamics to models of excitable cells, such as the Fitzhugh-Nagumo model and the Morris-Lecar model [6]. Figure 1 shows the nullclines and trajectories of both the hardware Oregonator model and the Fitzhugh-Nagumo model. These models have in common three circulative states; inactive (A), active (B $\rightarrow$ C), and refractory periods (D $\rightarrow$ A), as labeled in Fig. 1. Depending on the stability of the system, the hardware Oregonator shows two distinct behaviors. When the system is inactive and a fixed point of the system is unstable, it easily becomes active (A $\rightarrow$ B) by external stimuli. Then, it turns in refractory state (C $\rightarrow$ D). During the refractory state, the system can not be activated even if the external stimuli was

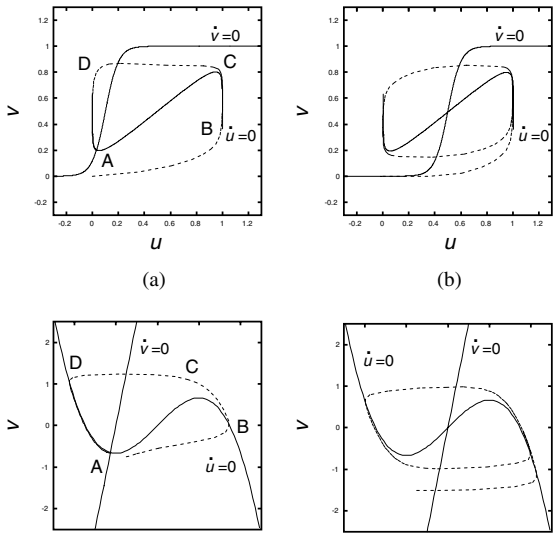


Fig. 1: Nullclines and Trajectories of hardware Oregonator model [(a) and (b)] and FitzHugh-Nagumo model [(c) and (d)].

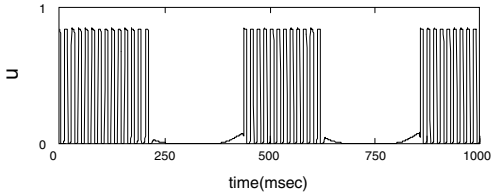


Fig. 2: Waveform of bursting cell model with periodic input.

given (excitatory mode). When a fixed point of the system is stable, the system oscillates (A → B → C → D → A) without external inputs (oscillatory mode).

For constructing a bursting cell model, we consider the hardware Oregonator model as a fast subsystem and introduce a slow subsystem represented as:

$$\epsilon \frac{dw}{dt} = -I_{leak} + I_{syn},\ \theta = \begin{cases} \theta_{osc} & \text{if } w \geq w_{th} \\ \theta_{exc} & \text{otherwise} \end{cases} \quad (4)$$

where w is a slow variable, ϵ a time constant, I_{leak} a leak current, I_{syn} a synaptic current, and θ_{osc} and θ_{exc} thresholds corresponding to the excitatory and oscillatory mode. We defined a burst cell model by Eqs. (1)-(4). The model shows bursting oscillations if w are varied periodically by current injection as shown in Fig. 2.

B. Bursting Osicllator with Depressing Synapse

We constructed a bursting oscillator model from two bursting cell models with excitatory and inhibitory synapses as shown in Fig. 3. We defined thresholds by:

$$\theta_1 = \begin{cases} \theta_{osc} & \text{if } w \leq w_{th} \\ \theta_{exc} & \text{otherwise} \end{cases},\ \theta_2 = \begin{cases} \theta_{osc} & \text{if } w \geq w_{th} \\ \theta_{exc} & \text{otherwise} \end{cases}. \quad (5)$$

where θ_1 and θ_2 represent the threshold of the first and second cell, respectively. Initially, the first cell operates in the

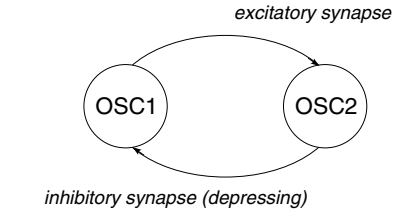


Fig. 3: Configuration of bursting oscillator model.

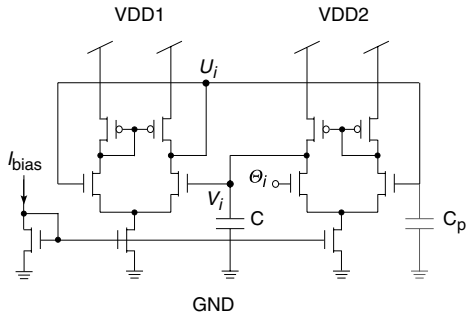
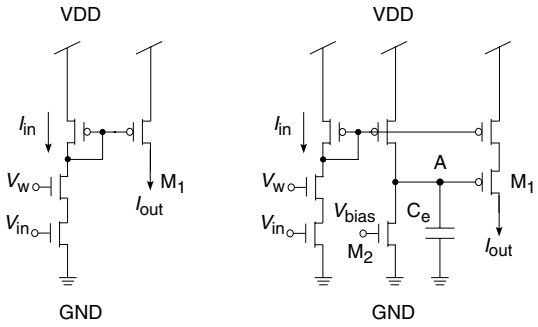


Fig. 4: Schematic of hardware Oregonator.



(a) conventional synapse circuit. (b) depressing synapse circuit.

Fig. 5: Schematics of synapse circuits. (a) conventional synapse circuit. (b) depressing synapse circuit.

oscillatory mode and the second cell operates in the excitatory mode. The second cell becomes the oscillatory mode through synaptic excitation with a short delay. Then, the first cell becomes the excitatory mode through synaptic inhibition, and the second cell becomes the excitatory mode in time. Thus, the bursting oscillator model shows bursting oscillation. For regulating the bursting frequency, we employ a depressing synapse as an inhibitory synapse.

3. CIRCUIT IMPLEMENTATION

We here propose analog CMOS circuit implementation of a bursting oscillator with depressing synapse.

A. Hardware Oregonator

First, let us describe an oscillatory circuit based on the hardware Oregonator model [10]. The oscillatory circuit, called the hardware Oregonator, consists of two operational-transconductance amplifiers (OTAs) and two capacitances as shown in Fig 4. The circuit dynamics are approximately

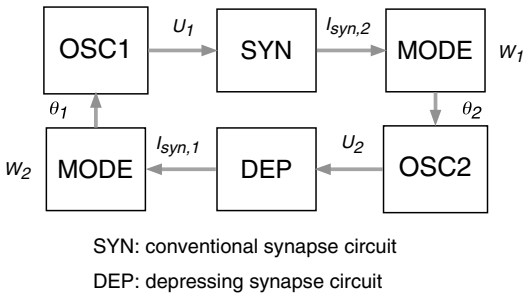


Fig. 6: Block diagram of bursting oscillator circuit.

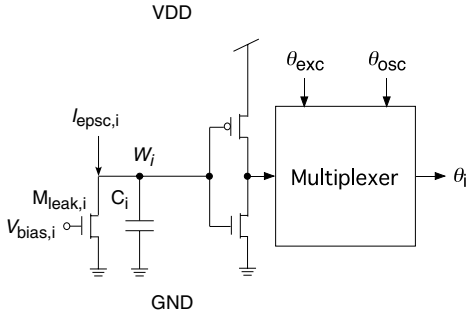


Fig. 7: Schematic of mode selector.

represented as follows:

$$U = F(U - V) \tag{6}$$

$$C\frac{dV}{dt} = \begin{cases} I_{bias} & \text{if } V \geq \theta \\ -I_{bias} & \text{otherwise} \end{cases} \tag{7}$$

where U and V represent voltages, θ a threshold voltage, C a capacitance, $F(\cdot)$ an output voltage of an OTA, and I_{bias} a bias current. The circuit dynamics can be obtained by qualitative approximation of Eqs. (1) and (2). We assume that the variables u and v of Eqs. (1) and (2) are restricted within [0:1]. When the rate of constant of Eq. (1) is much larger than that of Eq. (2), the differential term of Eq. (1) can be neglected. Furthermore, Eq. 7 with $\beta_v \to \infty$ forces the values of variable v to be zero when $u \leq \theta$, while $v \to 1$ when $u > \theta$. Thus, the temporal difference in Eq. (2) can approximately be represented binary values. Consequently, we obtain the circuit dynamics represented by Eqs. (5) and (6) [10].

B. Depressing Synapse Circuit

We employ a depressing synapse circuit that consists of a current mirror and a common-source amplifier as shown in Fig. 5(b) [11]. When the input voltage V_{in} is zero, the input current I_{in} and the voltage $V_{\rm A}$ at node A are zero. Therefore, the transistor $\rm M_1$ is in an on state. When $V_{in} > 0$, I_{in} increases $V_{\rm A}$ and decreases the conductance of M1. If one pulse input is given, the circuit outputs a pulse current I_{out} and I_{in} charges $V_{\rm A}$, and then the transistor $\rm M_2$ discharge C_e and V_A returns to zero. If pulse inputs are given at a short interval, subsequent inputs enter before $V_{\rm A}$ returns to zero, decreasing the conductance of $\rm M_1$ and the amplitude of I_{out}. Thus, this circuit acts as a depressing synapse circuit [11].

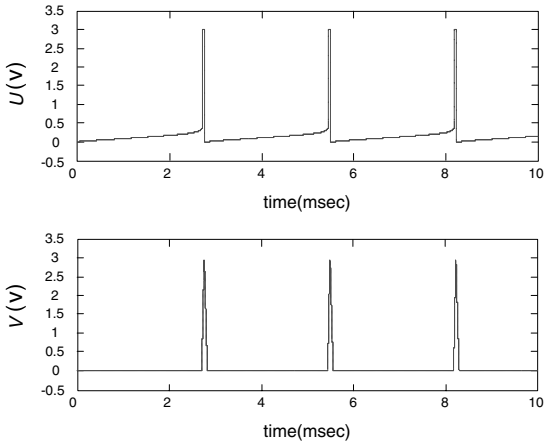


Fig. 8: Waveforms of hardware Oregonator in oscillatory mode.

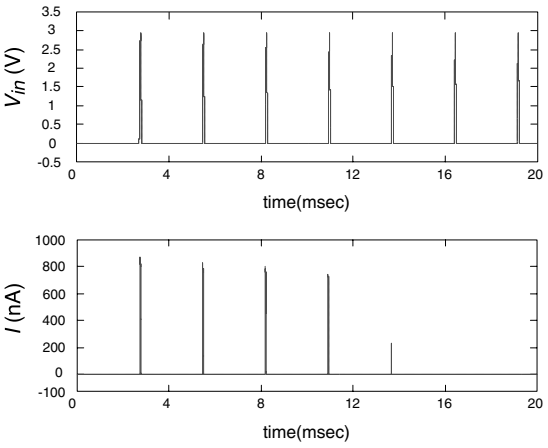


Fig. 9: Output currents of depressing synapse circuit.

C. Bursting Oscillator Circuit

We constructed a bursting oscillator circuit from two bursting cell circuit based on the hardware Oregonator, a depressing synapse circuit, and a conventional synapse circuit. Figure 6 shows the block diagram of the bursting oscillator circuit. We added a mode selector (Fig. 7) to the hardware Oregonator for constructing a bursting cell circuit.

4. Simulation Results

We demonstrate the operation of the bursting oscillator circuit through circuit simulations. Throughout simulations, we used a circuit simulator HSPICE and the model parameters for the 1.5-μm CMOS process.

First, we show the operation of the hardware Oregonator as shown in Fig. 3. We set the capacitances at $C = 10$ pF and $C_p = 0.1$ pF, the bias current at $I_{bias} = 500$ nA, the supply voltages at VDD1=VDD2 = 3 V, and the threshold voltage at $\theta = 0.8$ V so that the circuit operates in the oscillatory mode. Figure 8 shows the waveforms of voltages U and V in the oregonator circuit.

We show the operation of the depressing synapse circuit as shown in Fig. 4. We set the capacitance at $C_e = 50$ pF, the supply voltages at VDD $= 3.0$ V, and the bias voltages at

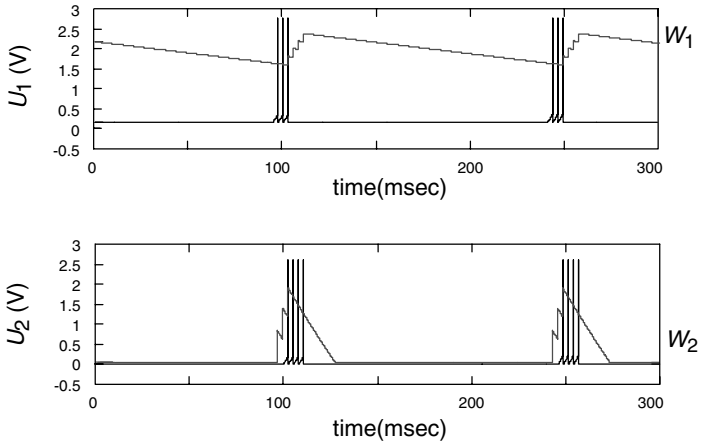


Fig. 10: Waveforms of voltages in bursting oscillator circuit (nondepressing).

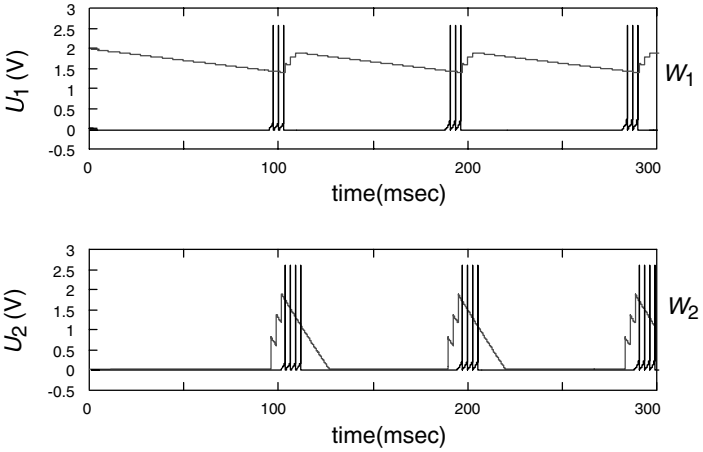


Fig. 11: Waveforms of voltages in bursting oscillator circuit (depressing).

$V_{bias} = 0.38$ V and $V_W = 1.0$ V. When a pulse train was given, the amplitude of the output current depressed (Fig. 9).

We show the operation of the bursting oscillator circuit. In the mode selectors, we set the capacitances at $C_1 = 200$ pF and $C_2 = 50$ pF, the bias voltages at $V_{bias,1} = V_{bias,2} = 0.5$ V, and the threshold voltages at $\theta_{osc} = 0.8$ V and $\theta_{exc} = 0$ V. When we set the voltages at $W_1 = 2.0$ V and $W_2 = 0$ V as an initial condition, then the circuit shows bursting oscillation as shown in Fig. 10.

By tuning the bias voltages of the depressing synapse circuit, we can change the bursting frequency of the bursting oscillatory circuit. We set the bias voltage at $V_{bias} = 0.35$ V. As a result of the depression of the synaptic current from the second cell to the first cell, the frequency of the slow variable W_1 becomes high, and then the bursting frequency also becomes high (Fig. 11).

Figure 12 shows the relationship between the bias voltage of the depressing synapse circuit and the bursting frequency of the bursting oscillator circuit. This result shows that if the bias voltage becomes large, the bursting frequency monotonically decreases.

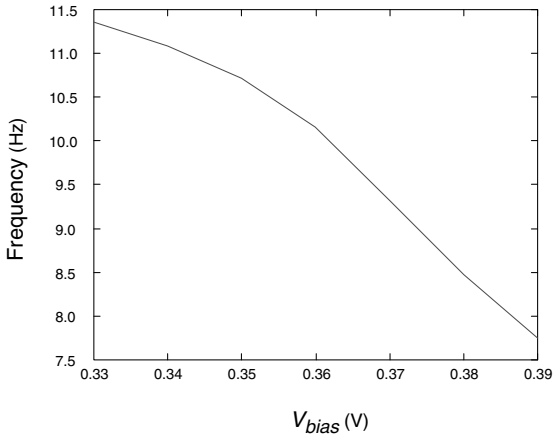


Fig. 12: Relationships between the frequency of the bursting oscillation and the bias voltages of the depressing synapse circuit.

5. SUMMARY

We designed an analog CMOS circuit implementing a bursting oscillator with a depressing synapse. Bursting oscillation arises the result of interaction between a fast excitatory subsystem and a slow subsystem [2]. We employ an analog oscillatory circuit, called the hardware Oregonator, for emulating the Belousov-Zhabotinsky reaction as a fast subsystem and an additional circuit as a slow subsystem. We constructed a bursting oscillator circuit from two bursting cell circuits with a depressing synaptic circuit. Through SPICE simulations, we demonstrated that the proposed circuit shows bursting oscillations and the bursting frequency can be regulated by tuning the depressing synapse circuit. Such characteristics are suitable as a component of an analog CPG chip.

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