Level-shift Circuit using Subthreshold-operated CMOS Operational Amplifiers

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Abstract

A CMOS level shifter that operates as a dc-cut capacitor is proposed. This circuit consists of a differential pair and a unity-gain buffer connected to one input of the differential pair. The unity-gain buffer consists of a subthreshold-operated operational amplifier and operates very slowly. The circuit operates as a high-pass filter and transmits ac signals but cuts off a dc voltage level. Therefore it can be used to connect two analog circuits having different dc levels. The results for the simulation and fabrication of this level shifter circuit are described.

Keywords: level shift, CMOS, circuit, subthreshold, operational amplifier, dc cut

1. Introduction

Subthreshold circuits are CMOS circuits in which MOSFETs are operated in the subthreshold region, i.e., the region where the gate-source voltage is set smaller than the threshold voltage of MOSFETs [1,2]. Subthreshold circuits operate very slowly because their circuit currents are quite small, on the order of 0.01 - 10 nA. This low-speed property can develop new circuit architectures for analog LSIs. This paper shows one example, a level shifter that uses a subthreshold-operated operational amplifier (subth-OP amp).

This level shifter operates as a high-pass filter or dc-cut capacitor and can be used to connect two analog circuits that have different dc levels. A coupling capacitor for low frequencies, e.g., for audio-band applications, has a large capacitance and cannot be fabricated monolithically on an integrated circuit. Our level shifter, however, consists of a concise CMOS circuit and can be integrated with other CMOS circuits on a chip. The following provides the details on this level shifter.

2. Operational amplifier operating in the subthreshold region

We first illustrate the schematic of a subth-OP amp we used. Figure 1 shows the circuit. The circuit topology is the same as that of ordinary two-stage amplifiers [3], but we drove the input stage (M1-M4) with a very small tail current I_0 (< 1 nA). Therefore, MOSFETs in the input stage operated in the subthereshold region. The common-source gain stage (M5) was driven with ordinary current levels (I_1 = 10-100 μA). Figure 2 depicts the frequency characteristics, simulated using a set of 0.35-μm CMOS device parameters and a phase compensation capacitance C of 10 pF. The driving currents were set to I_0 = 0.1 nA for the input stage and I_1 = 10 μA for the gain stage. The OP amp operated with a -3 dB cutoff frequency of 160 μHz, a unity-gain frequency of 24 Hz, and a slew rate of 9.8 μV/μs.

3. Level-shift circuit using subth-OP amp

Figure 3 shows the level shifter we propose. This circuit consists of a differential pair (M1, M2) with diode-connected MOSFET loads (M3, M4) and a subth-OP amp used as a unity-gain buffer. The input V_{in} for the level shifter is applied directly to one input of the differential pair and also applied to the other input V_{in2} through the subth-OP amp.

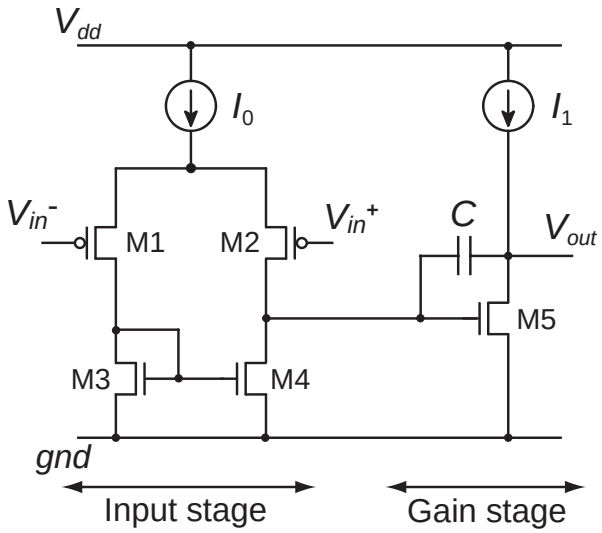


Figure 1. Operational amplifier, with input stage operated in the subthreshold region.

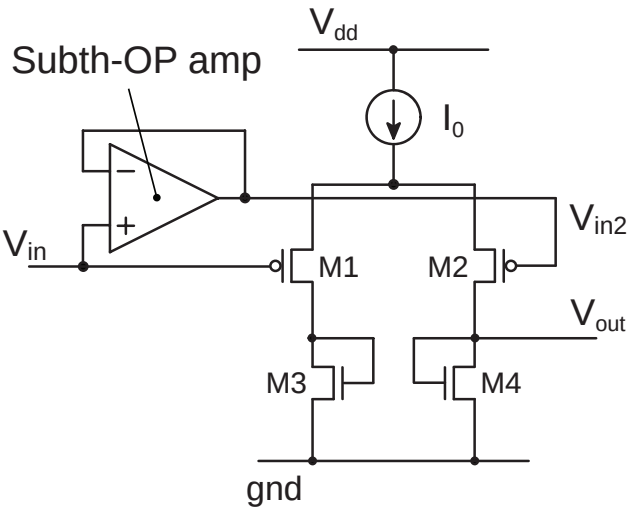


Figure 3. Level shifter consisting of differential pair and subth-OP amp.

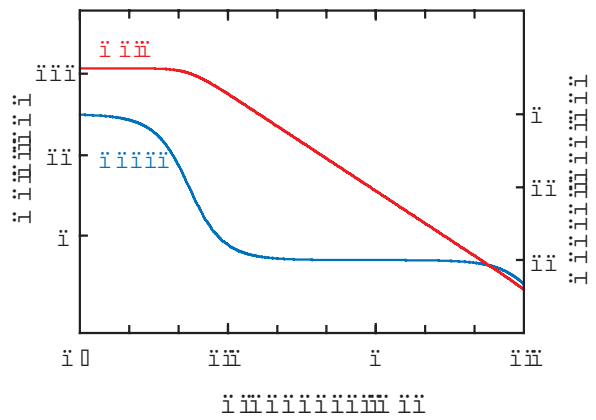


Figure 2. Bode plots for subth-OP amp, simulated using parameters given in the text.

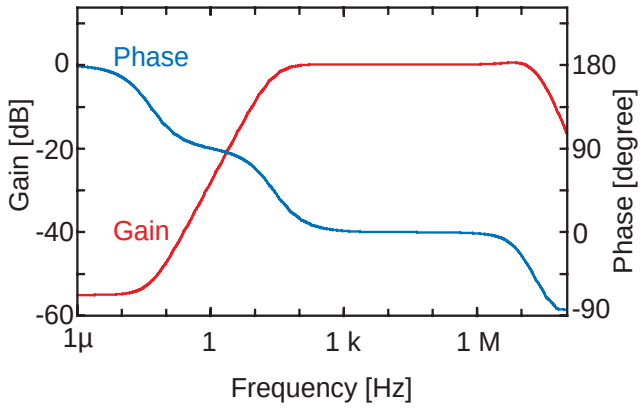


Figure 4. Bode plots for level shifter.

The circuit operates as a high-pass filter and cuts off the dc level of the input signal V_{in} as follows. For dc- and low-frequency input signals, output V_{in2} of the subth-OP amp can follow input signal V_{in}, and therefore, V_{in2} is set equal to V_{in}. Consequently, the differential pair produces no output signal, and V_{out} is fixed to a bias voltage determined by driving current I_0. In contrast, for high frequencies, the subth-OP amp cannot follow the input signal V_{in}, and therefore, V_{in2} is fixed to the dc level of the input signal. The differential pair receives ac input V_{in}-V_{in2} and therefore produces the corresponding ac output. In this way, the level shifter fixes the dc level of the output to a bias voltage regardless of the input dc level. Therefore the dc component of the input signal is not transmitted to the output.

4. Simulation results

We confirmed the effect of our level shifter shown in Fig. 3. We first simulated the operation, using a set

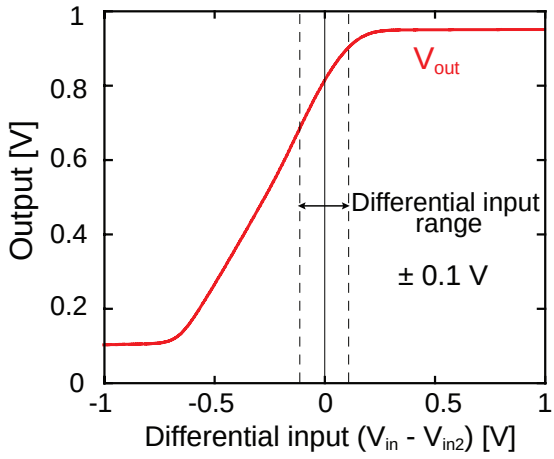
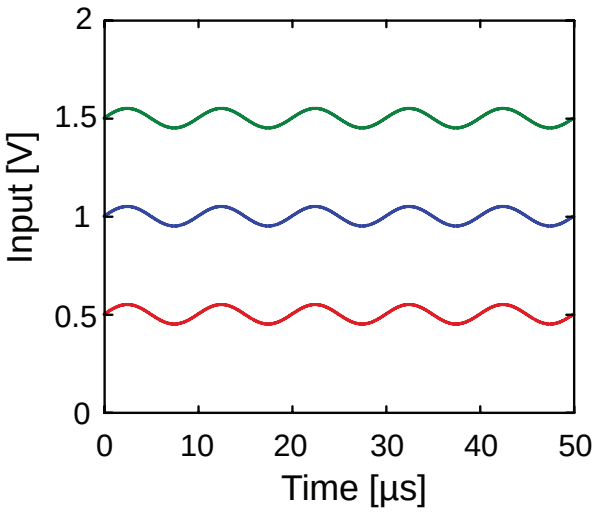


Figure 5. Voltage-transfer curve for differential pair of level shifter.

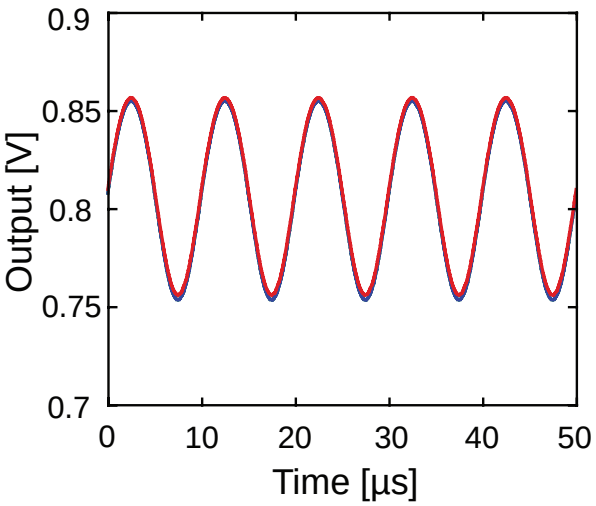
of 0.35-µm CMOS device parameters. Parameters used for the subth-OP amp were the same as given in the previous section. The driving current was set to I_0 = 10 µA for the differential pair.

Figure 4 shows the frequency characteristics of the level shifter. In this example, the gain was 0 dB at frequencies from 25 Hz to 10 MHz. For frequencies lower than 25 Hz, the gain decreased as frequency decreased and reached 0 at zero frequency. Owing to this zero dc gain, dc components of input signals are suppressed and does not appear in the output. The circuit operates as a high-pass filter and cuts off the dc level of input signals.

Figure 5 shows the voltage-transfer curve for the input stage (M1-M4) of the level shifter. The common-mode voltage of the input was set to 1 V. Transfer curve is almost linear for an input range of ±0.1 V. Figure 6 shows the ac response of the level shifter. Figure 6(a) shows input signals with different common-mode voltage levels (0.5 V, 1 V, and 1.5 V). Figure 6(b) shows the output for these inputs. The level shifter cut the dc voltage level of the inputs and produced a signal with a fixed dc level (0.8 V in this example) that is independent of input dc levels.



(a)



(b)

Figure 6. Ac response of level shifter.
(a) Input signals with different common-mode voltage levels (0.5 V, 1 V, and 1.5 V).
(b) Output signals with a fixed dc level independent of input dc levels.

5. Device fabrication

We fabricated our level shifter on a chip, using a 0.35-µm 2poly-4metal standard CMOS process. Figure 7 shows the micrograph of the circuit. The chip area was 140 µm × 220 µm (0.03 mm^2). Figure 8 depicts the measured gain of the circuit as a function of frequency. The operating condition was as follows:

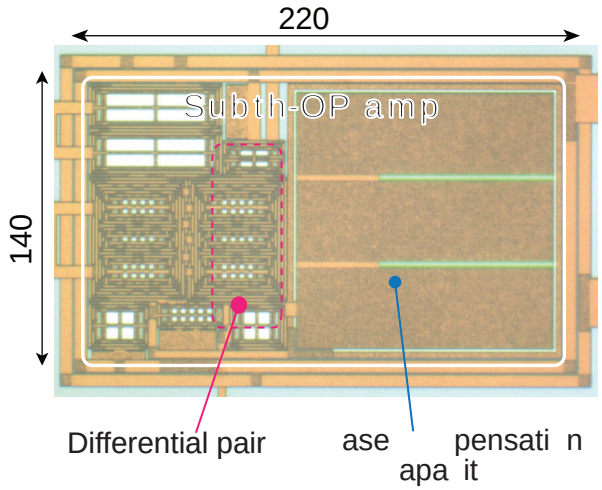


Figure 7. Chip micrograph of level shifter (area = 140 µm × 220 µm, 0.03 mm^2), fabricated using 0.35-µm, 2poly-4metal CMOS process.

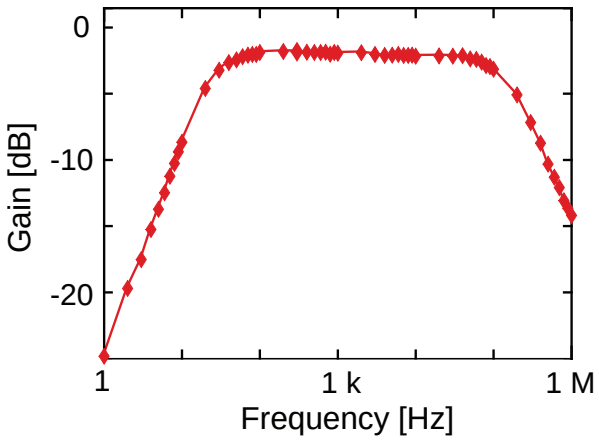


Figure 8. Gain of level shifter as a function of frequency (measured results).

power supply voltage V_{dd} = 3 V, input common-mode voltage = 1 V, and driving current I_0 = 10 µA. The gain decreased at low frequencies, and therefore, the dc component of the input was removed.

6. Summary

We proposed a level shifter consisting of a differential pair combined with a subth-OP amp. Our circuit operates as a dc-cut capacitor and can cut off the dc level of input signals. We fabricated this level shifter on a chip and confirmed its dc-cut operation.

Acknowledgement

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