A PTAT Voltage Source consisting of Subthreshold MOSFETs for Temperature Sensor LSIs

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Abstract— **An ultra-low power temperature sensor circuit based on a subthreshold MOSFET was proposed. The sensor consists of a modified β-multiplier self biasing circuit that uses a switched capacitor resistor instead of ordinary resistors. The circuit is operated in the subthreshold region, and it generates a proportional to absolute temperature (PTAT) voltage. Simulation with SPICE demonstrated that the circuit can be used as a smart temperature sensor with ultra-low power consumption of 3.5 μW or less. The accuracy of the sensor output was within $\pm$1.5℃.**
Keywords: CMOS, Temperature sensor, PTAT, Subthreshold, Ultra-low power

I. INTRODUCTION

An ultra-low power LSIs have been required for low-cost and low-power LSI applications such as implantable medical devices, sensor networks, and portable mobile devices. In this paper, we propose one such sensor IC, a temperature sensor that can operate with a low power of microwatts or less. Many temperature sensors consisting of CMOS circuits have been reported [1],[2] but are unsuitable for use in ultra-low power systems because of their large power consumption of several hundred microwatts. To achieve ultralow-power operation, we propose a temperature sensor IC that uses MOSFET circuits operated in the subthreshold region. Our sensor produces an output voltage that is proportional to absolute temperature (PTAT).

II. CIRCUIT CONFIGURATION

Figure 1 shows our PTAT voltage source. The circuit consists of a β-multiplier self biasing circuit, switched-capacitor resistors, a digital divider based on digital counters, and non-overlapping circuits. Transistors M_1 and M_2 are operated in the subthreshold region. Capacitors C_{B1} and C_{B2} remove high-frequency noise caused by switching operation. The following describe the operation of the generator in detail.

The subthreshold MOS current I_D can be expressed as

$$I_D = K I_0 \exp\left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right), \qquad (1)$$

where K is the aspect ratio (=W/L) of transistors, $I_0 (= \beta(\eta - 1)V_T^2)$ is the process-dependent parameter, $V_T (=k_B T/q)$ is the thermal voltage, V_{TH} is the threshold voltage of a MOSFET, and η is the subthreshold slope factor [3]. In the circuit in Fig.1, the current flowing in the circuit I_{OUT} is determined by the ratio of M_1 and M_2 and the resistance of switched-capacitor resistor $(f_{REF} \cdot C_1)^{-1}$, and is given by

$$I_{OUT} = f_{REF} \cdot C_1 \cdot \frac{\eta k_B T}{q} \ln(K_2/K_1). \qquad (2)$$

The voltage generator accepts the current I_{OUT} and the reference clock $(1/4 \cdot f_{REF})$ with the digital divider, and is given by

$$V_{OUT} = 4 \cdot \frac{C_1}{C_2} \cdot \frac{\eta k_B T}{q} \ln(K_2/K_1). \qquad (3)$$

Therefore, adjusting the capacitor ratio (C_1/C_2) and the number of digital counter, we can obtain the PTAT voltage with large temperature coefficient. The output voltage is insensitive to the process variations of capacitors because the output voltage depends on the capacitor ratio.

III. RESULTS

We confirmed the operation of our circuit with the aid of SPICE simulation. We used the SPECTRE level 53 model with a parameter set for the 0.35-μm 2P4M standard CMOS process. The supply voltage was set to 3 V, and the reference clock was set to 1 MHz.

To verify the stability of the circuit operation in device variation, we performed a corner analysis, using parameters provided by the manufacturer. The worst corners of nMOS and pMOS transistors, and capacitors (S: slow, T: typical, and F: fast) were taken into consideration.

Figure 2 shows the output voltage V_{OUT} for for three different process corner conditions as a function of temperature in a range from 0℃ to 80℃. As expected from Eq. (3), the value of V_{OUT} increased linearly with temperature. The average temperature coefficient of the three different corners was 5.5 mV/℃. The voltage error of difference between the simulation results and the theoretical results is shown in Fig. 3. The error shows a small value within $\pm$ 1.5℃ in a temperature range of 0℃ to 80℃. Figure 4 shows a layout pattern of the sensor circuit. The area was 0.07 mm^2.

Table I summarizes the performance of our circuit. The power consumption was about 10 μW at a 3-V supply voltage. Our circuit would be useful for smart temperature-sensor LSIs that are required to operate with ultra-low-power consumption.

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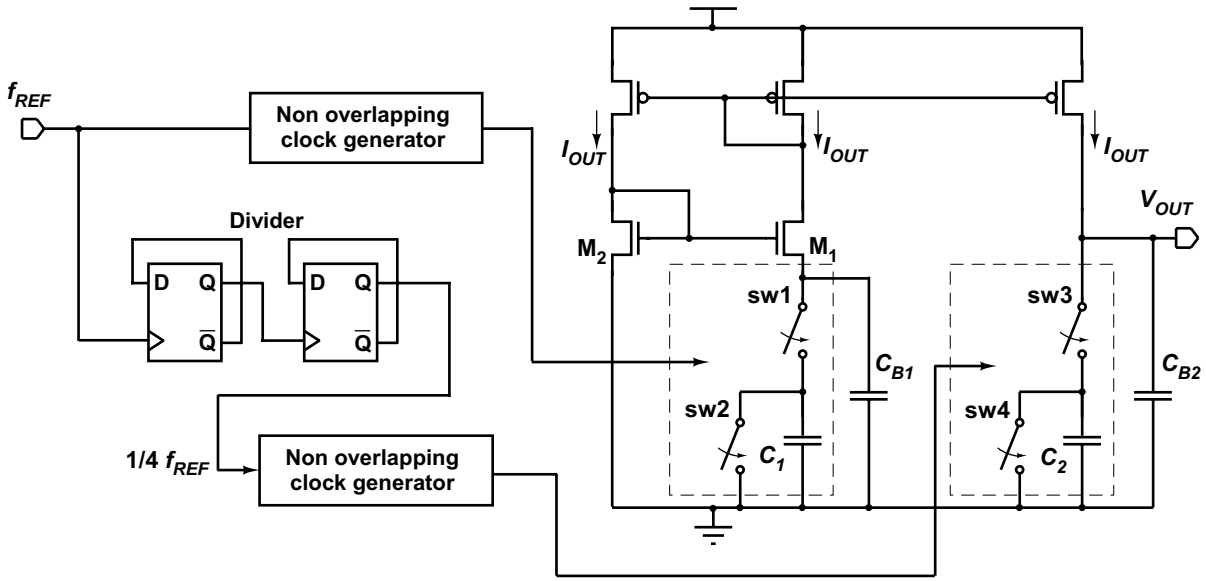
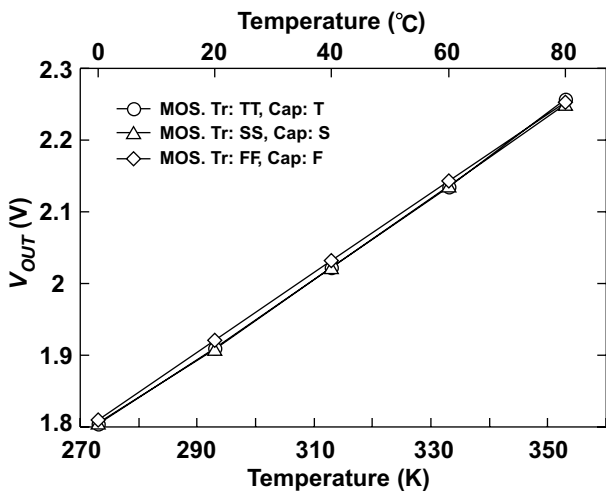Fig. 1: Circuit configuration of our PTAT voltage source.

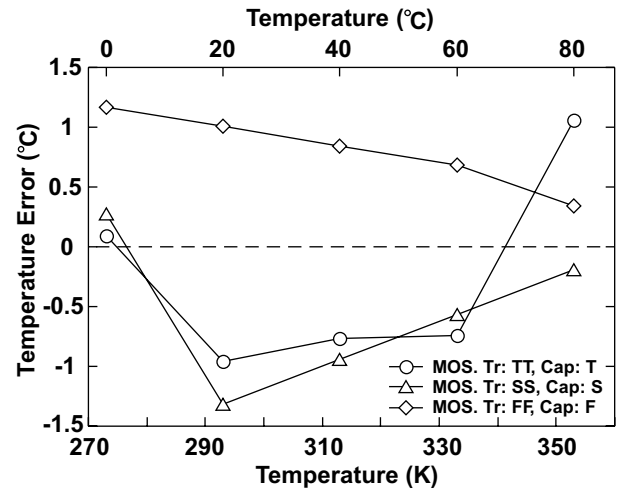Fig. 2: Simulated output voltage as a function of temperature.

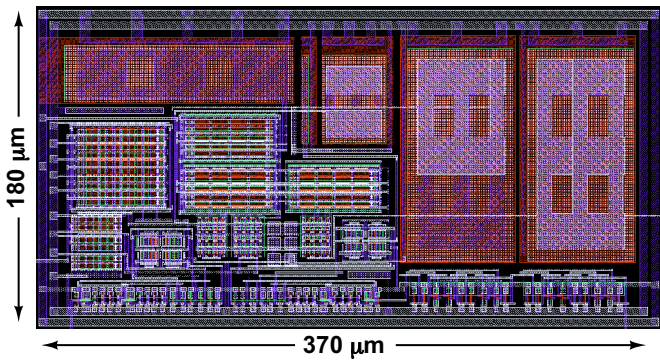Fig. 3: Calculated temperature error of output voltage without calibration and trimming techniques.

Fig. 4: Layout pattern of our circuit. Area is 0.07mm^2.

Process	0.35-μm CMOS
Temp. range	0 - 80 $^{\circ}$C
V_{DD}	3 V
Supply current	3.5 μA
T.C.	5.5 mV/$^{\circ}$C
Temp. error	$\pm$ 1.5 $^{\circ}$C
Area	0.07 mm^2

Table I: Performance Summary