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L E T T E R S

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Special issue devoted to the International Conference on Nano energies: theory and applications. *Perugia, July 10-13 2013.*	*What is Temperature?* *Peter Hänggi, Augsburg university* **July 11, 2013**	*FET Programs in Horizon2020* *Ales Fiala, Head of FET Unit* **July 11, 2013**	*Short papers from the Conference proceedings*

NANOENERGY LETTERS number 6 is a special issue devoted to the presentation of short papers from NANO*ENERGY*2013, the first international conference devoted to nanoenergies (Perugia, Italy, July 10-13 2013).

The aim of this conference is to bring together researchers, engineers, academicians as well as industrial professionals from all over the world and from different disciplines interested in the subject of micro and nanoscale energies. Energy at small scales is a cross-disciplinary field that covers both theoretical and experimental aspects of fundamental and applied sciences ranging from nanotechnology to statistical physics, from computer science to biomedicine.

This conference, supported by the E.C. FET program through the "Toward zero power" initiative, provides opportunities to exchange new ideas and application experiences face to face, to establish business or research relations and to find global partners for future collaboration. Topics of the conference include (but are not limited to): Energy transformation processes and dissipation at micro and nanoscale, Non equilibrium thermodynamics of small systems, Magnetic and Nanomechanical Logic principles and devices, Bioenergetics and bio-inspired low energy computation, Energy harvesting for powering micro and nano devices, ICT-Energy: switch architectures and zero power computing, Energy aware algorithms and software strategies for low power computing, Low power distributed sensor networks, Landauer limit: theory and experiments, Stochastic Resonance, Noise and fluctuations phenomena in small systems. I hope you enjoy the contributions that we present in this issue.

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NANOENERGY LETTERS

Towards Asynchronous Digital Circuit Design based on Stochastic Resonance

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***Abstract*—A CMOS configuration of the basic digital logic gates using the concept of stochastic resonance (SR) is presented. In this framework, the SR effect applied to nonlinear electrical systems that exhibit hysteresis is proposed, in order to build logical gates (SR gates). The hysteresis property is crucial, because it ensures the stability of all logic states. Moreover, this configuration also allows the selection of the logic operations, by applying an external bias. SPICE simulations are run using a 0.18-µm CMOS technology. The simulations results have proven the effective performance of the SR gates for an optimal amount of noise, despite the introduction of an intentional mismatch between the threshold voltages of the transistors.**

I. INTRODUCTION

THE use of an optimal amount of noise has proved to be an effective method to improve specific tasks. This effect is well-known as stochastic resonance (SR) [1]. One of the main applications of the SR effect is the improvement of the response of nonlinear systems to weak input stimuli [2]. An application of noise in nonlinear systems was proposed by Murali *et al.*, where the basic logic operations can be implemented by electrically modeling a double-well potential function with an additive Gaussian noise [3]; further, the precise values for the bias are necessary to set the logical operation, However, the implementation of this system is quite complex because it requires the use of several operational amplifiers and additional bias circuits, which is expensive in terms of VLSI. This paper proposes a novel configuration, by cooperative use of noise in nonlinear systems. The concept involves the electrical systems where the hysteresis phenomenon occurs. In this case, the presence of two thresholds prevents the activation of the output in the presence of large noise fluctuations.

II. CIRCUIT DESIGN AND SIMULATION OF THE SR GATES

The idea of this paper is based on the utilization of noise to build logic gates. The main design is based on electrical systems with hysteresis, which posses a double threshold. Traditionally, noise assistance has been used to improve weak signals detection in systems with one threshold. However, one evident problem is that a high-amplitude peak of the noise signal can trigger an unnecessary response (Fig. 1a). Generally this response has fluctuations and hazards; in our case, the double-threshold system avoids hazards as long as the noise amplitude remains lower than the difference between the two thresholds, therefore the logic state remain stable (Fig. 1b). Figure 2 shows the proposed electrical

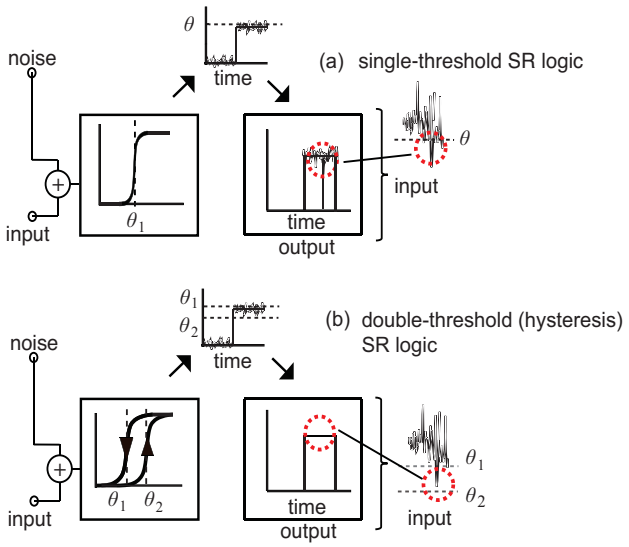

Fig. 1 (a) Noise assistance in nonlinear systems with one threshold; (b) noise assistance in nonlinear systems exhibiting hysteresis.

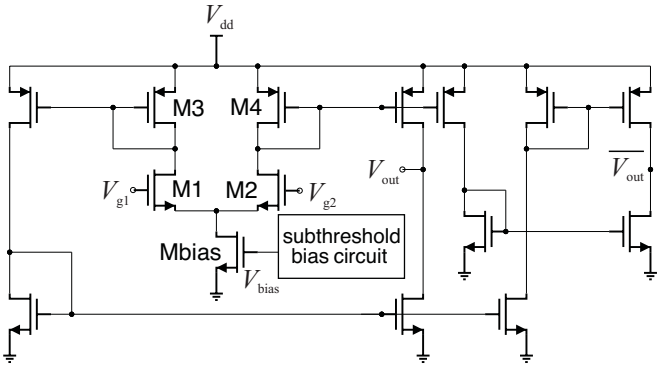

Fig. 2 (a) Noise assistance in nonlinear systems with one threshold; (b) noise assistance in nonlinear systems exhibiting hysteresis.

diagram of the implementation of the SR gates. This configuration is a differential pair configuration where V_{g1} and V_{g2} denote the floating gates, and V_{out} and $\overline{V_{out}}$ are the outputs. V_{bias1} and V_{bias2} serve as selectors for the logic operations. The generic symbol of a four-terminals SR gate is shown in Fig. 3.
Table 1 lists the combinations of V_{bias1} and V_{bias2} to set either the NOR or the NAND operation with V_{out} as the output. By selecting $\overline{V_{out}}$ as the output, both the OR and the AND operations can be performed (Fig. 4a). The introduction of noise (V_{noise}) aids in the detection of the weak input signals as well as to overcome the problem associated with the mismatch between

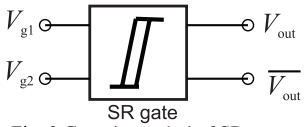

Fig. 3 Generic symbol of SR gate.

Table 1: Selection of the logic operations according

V_{bias1}	V_{bias2}	$\overline{V_{out}}$	V_{out}
V_{dd}	0	OR	NOR
V_{dd}	V_{dd}	AND	NAND

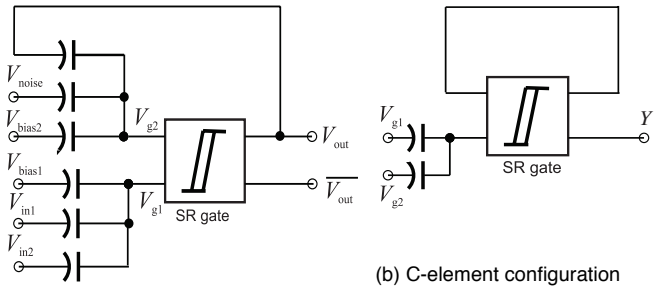

Fig. 4 (a) Configuration for the basic logic operations depends on the values of V_{bias1} and V_{bias2}; (b) configuration of the C-element.

the threshold voltages. However, a main limitation is the timing of the SR gates. The delay time of the SR gate response is limited by the stochastic process; therefore, synchronization would be a problem for the effective performance of high-complexity circuit configurations. A suitable alternative is the implementation of asynchronous circuits with the current SR gates. Therefore, in addition of the basic logic gates, there are some necessary configurations required to implement asynchronous logic. Such is the case of the C-element. This is a two-input configuration, where the output storages the previous state as long as both the inputs are different. This configuration can be implemented as shown in Fig. 4b. Table 2 represents the state table of the C-element. In this case, the feedback allows the storage of the previous state, until both the inputs attain the same value. The circuit simulations are performed through a SPICE program using a 0.18μm CMOS technology. The power supply is set to 0.35V and all the transistors are working in the subthreshold region. Additive Gaussian noise is introduced in V_{noise} (μ = 0 and σ =18mV) and an offset voltage of V_{dd}. One well-known advantage of the subthreshold regimen is the reduction of the power consumption; however one implication, is the increase of the sensitivity of the threshold-voltage variations; particularly in the differential pair configuration, where a precise matching is required between the transistors.

Table 2: C-element state table

V_{in1}	V_{in2}	Y	Y_{next}
0	0	X	0
0	1	0	0
1	0	0	0
1	1	1	1
0	1	1	1
1	0	1	1
0	0	0	0

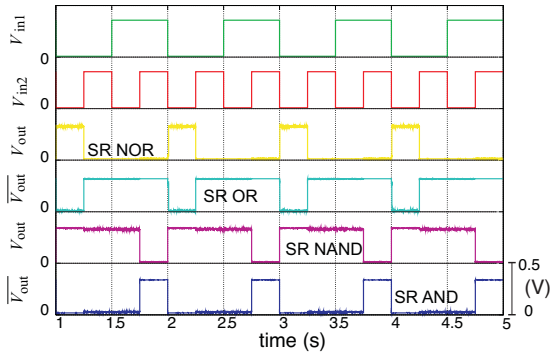

Figure 5: Simulation results of SR gate for NOR, OR, NAND and AND operations.

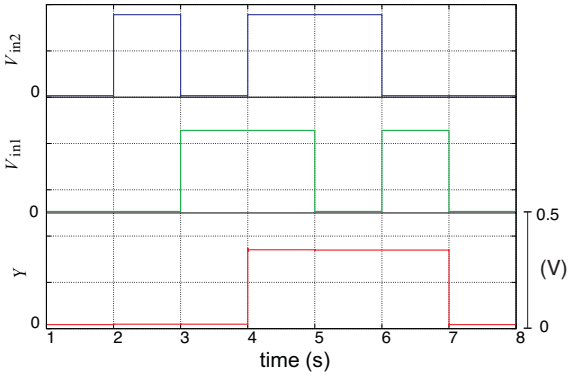

Figure 6: Simulation results for the C-element.

In this case, the introduction of noise actually helps to overcome this problem. During the simulations, the threshold voltage is intentionally varied. Figure 5 shows the simulation results of the SR gates of the four basic logic gates. The simulation results for the C-element are shown in Fig. 6 for a power supply of 0.35 V.

III. CONCLUSIONS

The concept of stochastic resonance effect served as the basis to build a digital logic with noise assistance in bistable systems. The main contribution of this study is the use the hysteresis characteristic of the differential pair configuration to avoid spontaneous hazards and high amplitude oscillations. Moreover, the proposed circuit can be used to implement the four basic logic gates, by simply varying the two external bias values, either to 0 or to V_{dd}. Owing to the fact that all the transistors are working in the subthreshold regime, the circuit achieves a low power consumption. Noise also reduces the mismatch effect of the differential pair. The circuit simulations have demonstrated the effectiveness of using noise in the proposed configuration to build logical circuits.

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