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Precisely-timed synchronization among spiking neural circuits on analog VLSIs

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Abstract.
A neural network exhibiting precisely–timed synchronization under a noisy environment with depressing synapses is proposed [1]. We explain how the neural network was constructed by using silicon neural circuits [2] and depressing synapse circuits [3], which we have already developed, and evaluate the precision of timing among silicon neurons. Moreover, a simple analog spike timing dependent plasticity STDP circuit was designed for constructing a neural network that exhibited robust synchronization under a noisy environment. We confirmed that it operated as required.

1. Introduction

Although some cells have been found to have firing variations when the spike rows of neuronal cells in the cerebral cortex have been analyzed, they often synchronize very precisely [4- 6]. The discovery of this synchronous activation phenomenon was almost concurrent with the time gap (clock skew) problem in digital large-scale integrated circuits, which is due to wiring capacitance and the difference in the clock propagation delay time. Problems with unevenness between single devices have recently become even more remarkable with continuing miniaturization in the semiconductor process. Guaranteeing an appropriate timing margin is presently difficult and major semiconductor manufacturers are using hereditary algorithms in post-manufacturing processes to achieve the required margin.

Against such a background, reports on a group of nerve cell whose variations are markedly larger than those in a semiconductor device, demonstrating exceptionally accurate synchronization, have been extremely inspiring. A novel solution to the clock skew problem in LSIs could be found by imitating that system. A neural network model using depressing synapses was recently proposed [1]. It was reported to have precisely-timed synchronization even under a noisy environment. We constructed this network, and numerically confirmed neuron circuits were synchronized by making use of silicon neuron and depressing synapses developed by Asai et. al. [2] and Kanazawa et. al. [3]. Fukai and Kanemura [1] found a higher noise tolerance could be achieved by combining STDP learning circuit. We developed a basic analog circuit for the STDP learning circuit.

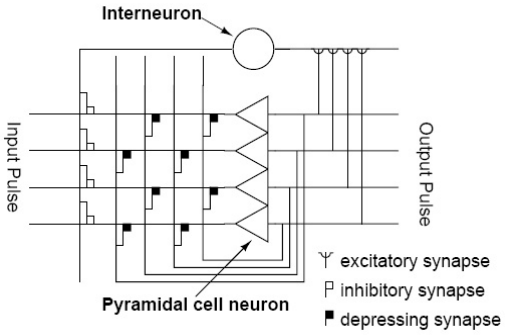

Fig. 1: Inhibitory neural network with depressing synapses

2. Precisely–timed pulse synchronization network

Figure 1 shows the network model consisting of four pyramidal neurons with their outputs connected to an inter-neuron through excitatory synapses. The inter-neuron is also connected to the inputs of all the pyramidal neurons through inhibitory synapses. There are positive feed-back connections through randomly-connected depressing synapses from the output of a pyramidal neuron to the input of other pyramidal neurons. Therefore, the activation of a pyramidal neuron further activates pyramidal neurons connected to it, resulting in their synchronization.

2.1 CMOS circuit implementation

Asai et. al [2] and Kanazawa et. al. [3] proposed a large-scale integration circuit of spiking neurons and a circuit for dynamic synapses by using CMOS analog technology.

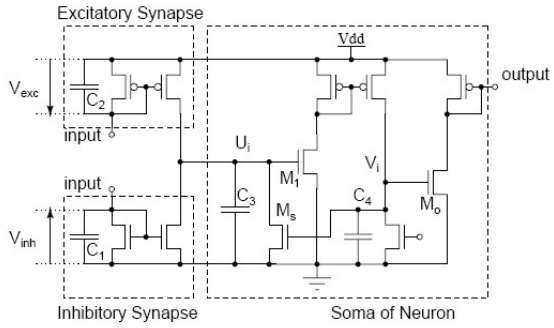

Fig. 2: CMOS neuron circuit.

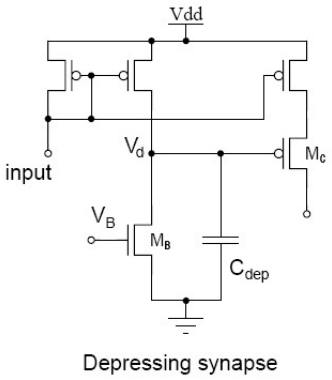

Fig. 3: Depressing synapse circuit.

We implemented the network model explained above by using CMOS neuron circuits with depressing synapse circuits, and describe its operating principles here.

Figure 2 shows a CMOS neuron circuit, an excitatory synapse circuit, and an inhibitory synapse circuit. Input pulses for excitatory synapse circuits are sent through a ***p*** type current mirror circuit, whose output is connected to membrane capacitor $\mathbf{C_3}$. Because of this, the membrane potential rises. The input pulses for inhibitory synapse circuits are sent through an ***n*** type current mirror circuit that reduces the charge on $\mathbf{C_3}$, and the membrane potential decreases. The neuron circuit that receives the output current of the excitatory and inhibitory synapses does not fire when membrane potential $\mathbf{U_i}$ is below the threshold voltage of the ***n*** type MOSFET $\mathbf{M_1}$, but when it rises above this threshold, $\mathbf{M_1}$ begins to turn ON, and potential $\mathbf{V_i}$ rises. As a result, $\mathbf{M_o}$ turns ON. At the same time, $\mathbf{M_s}$ discharges the membrane, which results in the membrane potential being reset.

Figure 3 shows a depression synapse circuit. V_d is generated in the circuit voltage by the source-common amplifier, which acts as load to the current source by load capacitance $\mathbf{C_{dep}}$. The input pulse is amplified and increases V_d. This voltage is gradually decreased by nMOS current source M_B to the ground level. If input is a high-frequency pulse, load capacitance $\mathbf{C_{dep}}$ is not fully discharged. The synapse circuit cannot copy the input current to the output node at this time because M_c is turned off. Therefore, the circuit operates as a depressing synapse when it receives high-frequency pulses at input.

A pulse synchronization circuit was constructed by using the neuron circuits in Figs. 2 and 3. Figure 4 shows the implementation of the network. We constructed a small-scale network that consisted of two pyramidal neurons and an inter-neuron to study the network's operation. Two kinds of feed-back synaptic junctions were studied, i.e., (I) excitatory synapses (NDSs) and (II) depressing synapses (DSs).

3. **Simulation Results**

We used HSPICE to study the operation of the pulse-synchronization network circuit. We used a MOSIS, and the AMIS 1.5-μm CMOS process with a channel length of 1.5 μm and a channel width of 2.3 μm in the simulation. Two kinds of feedback synaptic junctions were studied for comparison excitatory synapses (NDSs) and depressing synapses (DSs).

We designed the circuit to attain the same amount of integration current for the membrane capacitance for the neuron circuit when an input pulse of 500 μs (amplitude of 10 nA) was applied. The membrane potential for the NDSs increased when input pulse was applied, but the rate of increase was constant. However, the rate of increase of the membrane potential for DSs was higher than for NDSs. The amount of output current for a continuous pulse decreased.

Figure 5 shows the simulation results for NDSs, and Fig. 6 shows those for DSs. For both NDSs and DSs, the output pulses were synchronous. This is because all the synaptic feed-back strength is positive. The firing output of one pyramidal neuron induces firing in the other pyramidal neurons, leading to synchronization.

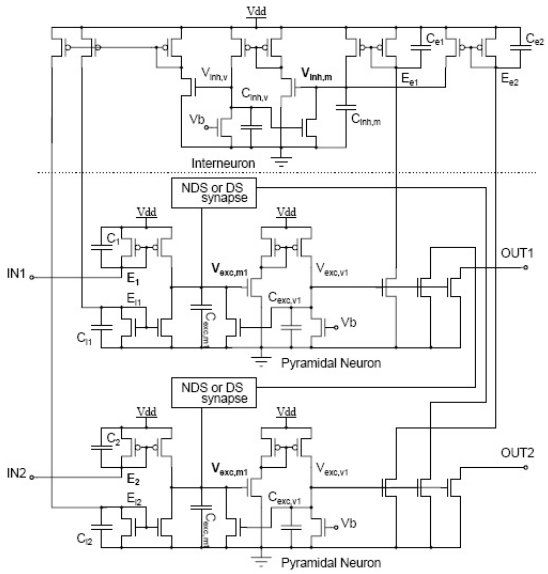

Fig. 4: CMOS neuron circuit for precisely-timed synchronization. Network is structured with two pyramidal neurons and inter-neuron. There are two kinds of feed-back synaptic junctions: excitatory synapses (NDSs) and depressing synapses (DSs).

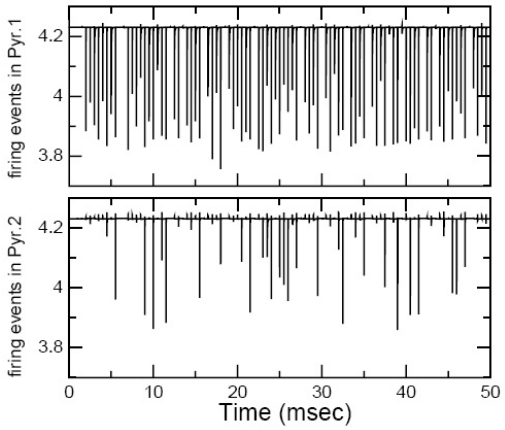

Fig. 5: Firing events of neurons when using NDSs.

Synapses	Excitatory	Depressing
Average (ns)	924	821
Standard deviation (ns)	356	207

Table 1: Results for output pulse jitter.

The firing pulse jitter of the two pyramidal neurons was also measured. Table 1 lists these. They indicate precisely-timed synchronization with average timing jitter of 924 ns for NDSs and 821 ns for DSs. The DSs' standard deviation for pulse jitter distribution decreased to 58% that for NDSs'.

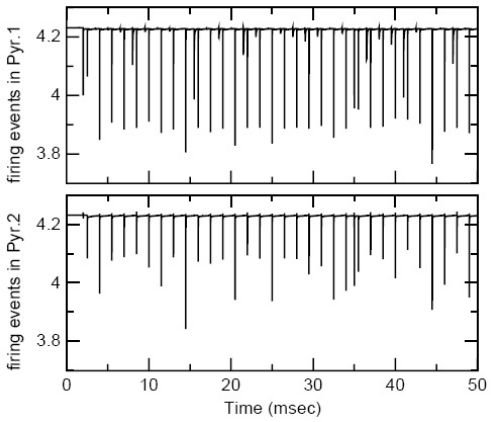

Fig. 6: Firing events of neurons when using DSs.

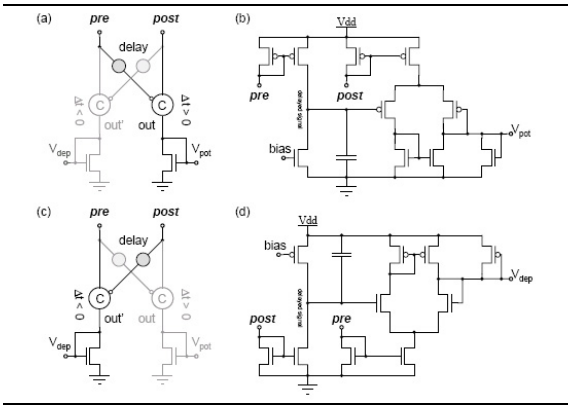

Fig. 7: Spike-timing detection circuit.

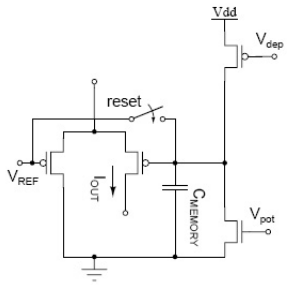

Fig. 8: Silicon synapse circuit for initializing, renewing, and storing coupling strengths in response to spike-timing.

4. **STDP circuit structure**

Fukai and Kanemura [1] showed that synchronization among pyramidal cells became robust when STDP learning was introduced to the network with DSs. Motivated by these results, we developed a new, basic, analog STDP circuit, which we propose in this section.

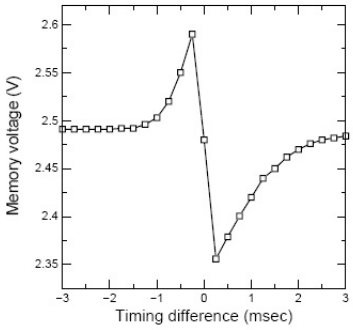

Fig. 9: Simulation results for STDP circuit.

The STDP circuit was constructed to study the timing for the output pulse. It was composed of a spike-timing detection circuit and a memory circuit. Figure 7 shows a spike-timing detection circuit, composed of a delay circuit (source common amplifier and a capacitor **C**), correlation detection circuits (unity gain differential amplifier), and current conversion circuits (diode-connected MOSFET). The circuit for positive spike timing is in Figs. 7 (a) and (b), and that for negative in Figs. 7 (c) and (d). If the interval between ***pre*** pulse and ***post*** pulse is positive ($t_{post} - t_{pre}>0$), as seen in Figs. 7 (a) and (b), when the delay circuit receives a ***pre*** pulse input, this is amplified by the source common amplifier. The amplified signal is a stationary current, and the time constant is attenuated by capacitor **C.** The ***post*** pulse is represented by the current source of the unity gain amplifier. Therefore, the ***post*** pulse operates as a switch for the unity gain amplifier. In other words, the ***pre*** pulse voltage corresponding to the ***post*** pulse delay time will be transmitted to the unity gain amplifier. The transmitted voltage is applied in the diode-connected MOSFET. Therefore, the voltage output responding to delay time is converted into the current value by the MOSFET. Therefore, current corresponding to the delay time can be obtained. A similar operation is observed when the interval between the pre pulse and the post pulse is negative and the output current corresponding to the pulse interval is generated.

Figure 8 outlines the structure of a memory circuit, composed of a current mirror circuit whose current value depends on the spike-timing, a differential pair, and capacitance. The voltage in the memory capacitance is stored and erased and the input current value of the differential pair changes by using the current value, which depends on the spike-timing. As a result, we can obtain a circuit whose pulse timing relies on the connection weights. When the spike timing is positive, $\mathbf{V_{pot}}$ is high and the voltage of C_{MEMORY} is decreased. Because the voltage of the differential pair decreases, the output (gate to source voltage of the transistor making up the differential pair) increases, thus increasing the coupling strength.

We used SPICE simulation to verify the operation of the proposed STDP circuit. Figure 9 plots the simulation results showing variations in the voltage of C_{MEMORY} according to spike-timing. The reference voltage was assumed to be 2.5 V.

5. **Summary**

A CMOS neural network circuit based on a precisely-timed pulse synchronization network model was proposed. The network was constructed using large-scale integration CMOS circuits, and their synchronization was verified. In addition, we confirmed that it could achieve a precise jitter conversion of approximately 58% by using depressing synapses instead of excitatory synapses. We also constructed a new STDP circuit and verified its operation by simulation. We intend to construct pulse synchronous network and increase the number of pyramidal neurons using this STDP circuit in the future.

References

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