

A Novel Segmentation Model for Neuromorphic CMOS Circuits

Eric Shun Fukuda[†], Tetsuya Asai, Tetsuya Hirose and Yoshihito Amemiya

Graduate School of Information Science and Technology, Hokkaido University.

Kita 14, Nishi 9, Kita-ku, Sapporo, 060-0814 Japan.

Phone:+81-11-706-7147, Fax:+81-11-706-7890

[†] email: fukuda@sapiens-ei.eng.hokudai.ac.jp

Abstract

We designed a simple neural segmentation model that is suitable for analog circuit implementation. The model consists of excitable neural oscillators and adaptive synapses where the learning is governed by a symmetric spike-timing dependent plasticity (STDP). We numerically demonstrate basic operations the proposed model, as well as fundamental circuit operations using a simulation program with integrated circuit emphasis (SPICE).

1. Introduction

Humans can distinguish multiple sensory sources that coincide. Recent discoveries of synchronous oscillations in the visual and auditory cortex have triggered much interest in exploring oscillatory correlation to solve the problems of neural segmentation. Many neural models that perform segmentation have been proposed, e.g., [1, 2, 3], but they are often difficult to be implemented on practical integrated circuits. In this paper, we propose a simple neural segmentation model that is suitable for analog complementary metal-oxide-semiconductor (CMOS) circuits.

Our segmentation model consists of mutually-coupled neural oscillators exhibiting synchronous (or asynchronous) oscillations. All the neurons are coupled with each other through positive or negative synaptic connections. Each neuron accepts external inputs, e.g., sound inputs in the frequency domain, and oscillates (or does not oscillate) when the input amplitude is higher (or lower) than a given threshold value. Our basic idea is to strengthen (or weaken) the synaptic weights between synchronous (or asynchronous) neurons, which may result in phase-domain segmentation. The synaptic weights are updated based on symmetric spike-timing dependent plasticity (STDP) using Reichardt's correlation neural network [4] that is suitable for analog CMOS implementation. In the following sections, we introduce our segmentation model, and demonstrate the operations through numerical simulations. Then we present unit CMOS circuits for our model, and demonstrate the operations using a simulation program with integrated circuit emphasis (SPICE).

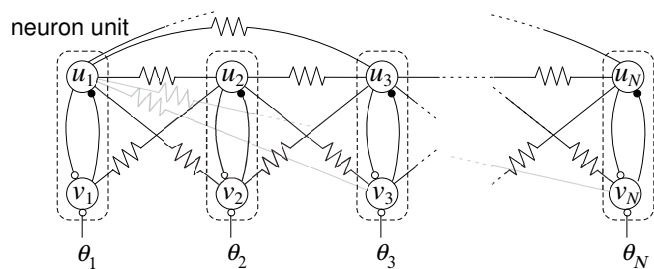


Figure 1: Network construction of segmentation model.

2. The model and basic operations

Figure 1 illustrates our segmentation model. The network has N neural oscillators consisting of the Wilson-Cowan type activator and inhibitor pairs (u_i and v_i) [5]. All the oscillators are coupled with each other through resistive synaptic connections, as illustrated in the figure. The dynamics are defined by

$$\tau \dot{u}_i = -u_i + f_{\beta_1}(u_i - v_i) + \sum_{j \neq i} W_{ij}^{uu} u_j, \quad (1)$$

$$\dot{v}_i = -v_i + f_{\beta_2}(u_i - \theta_i) + \sum_{j \neq i} W_{ij}^{uv} u_j, \quad (2)$$

where τ represents the time constant, θ_i the external input to the i -th oscillator, $f_{\beta_i}(x) = [1 + \tanh(\beta_i x)]/2$, W_{ij}^{uu} the connection strength between the i -th and j -th activators and W_{ij}^{uv} the strength between the i -th activator and the j -th inhibitor. According to the stability analysis in [5], the i -th oscillator exhibits excitable behaviors when $\theta_i < \Theta$, and exhibits oscillatory ones when $\theta_i \geq \Theta$, if W_{ij}^{uu} and W_{ij}^{uv} for all i and j were zero.

Suppose that neurons are oscillating ($\theta_i \geq \Theta$ for all i) with different initial phases. The easiest way to segment these neurons is to connect the activators belonging to the same (or different) group with positive (or negative) synaptic weights. In practical hardware, however, the corresponding neuron devices have to be connected by special devices having both positive and negative resistive properties, which prevents us

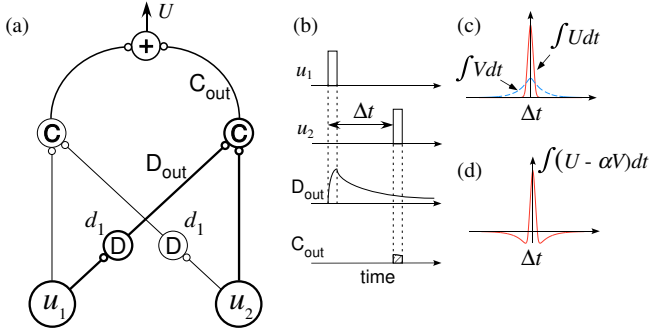


Figure 2: Reichardt's correlation neural network.

from designing practical analog circuits. Therefore, we simply employ positive synaptic weights between activators and inhibitors, and do not use negative weights. When the weight between the i -th and j -th activators (W_{ij}^{uu}) is positive and W_{ij}^{uv} is zero, the i -th and j -th activators will be synchronized. Contrarily, when the weight between the i -th activator and the j -th inhibitor (W_{ij}^{uv}) is positive and W_{ij}^{uu} is zero, the i -th and j -th activators will exhibit asynchronous oscillation because the j -th inhibitor (synchronous to the i -th activator) inhibits the j -th activator.

The synaptic weights (W_{ij}^{uu} and W_{ij}^{uv}) are updated based on our assumption; one neural segment is represented by synchronous neurons, and is asynchronous to neurons in the other segment. In other words, neurons should be correlated (or anti-correlated) if they received synchronous (or asynchronous) inputs. These correlation values can easily be calculated by using Reichardt's correlation neural network [4] that is suitable for analog circuit implementation [6]. The basic unit is illustrated by thick lines and circles in Fig. 2(a). It consists of a delay neuron (D) and a correlator (C). A delay neuron produces blurred (delayed) output D_{out} from spikes produced by activator u_1 . The dynamics is given by

$$d \cdot \dot{D}_{out} = -D_{out} + u_1, \quad (3)$$

where d represents the time constant. The correlator accepts D_{out} and spikes produced by activator u_2 , and outputs $C_{out} = D_{out} \times u_2$. The conceptual operation is illustrated in Fig. 2(b). Note that C_{out} qualitatively represents correlation values between activators u_1 and u_2 because C_{out} is decreased (or increased) when Δt , inter-spike intervals of the activators, is increased (or decreased). Since this basic unit can calculate correlation values only for positive Δt , we employ two basic units, which we call a unit pair, as shown in Fig. 2(a). The output (U) is thus obtained for both positive and negative Δt by summing the two C_{out} s. Through temporal integration of U , we obtain impulse responses of this unit pair. The sharpness is increased as $d \rightarrow 0$. Figure 2(c) plots two impulse responses for small and large d (red and

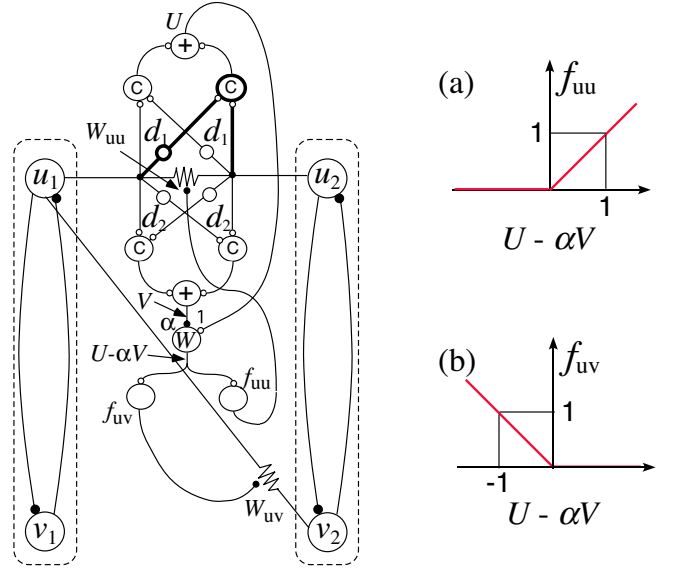


Figure 3: STDP learning circuitry.

blue curves). Introducing two unit pairs with different ds , i.e., d_1 and d_2 ($\gg d_1$), one can obtain those two impulse responses (U and V) simultaneously. The weighted subtraction ($U - \alpha V$) produces well-known Mexican hat characteristics, as shown in Fig. 2(d). We use this symmetric characteristic for the weight updating as a spike-timing dependent plasticity (STDP) in the oscillator network.

Figure 3 shows a schematic of our learning circuitry. The two unit pairs are located between two activators u_1 and u_2 . The weighted subtraction ($U - \alpha V$) is performed by interneuron W . According to our assumptions above for neural segmentation, when $U - \alpha V$ is positive, the weight between activators u_1 and u_2 (illustrated by a horizontal resistor symbol in Fig. 3) is increased because they should be correlated. On the other hand, when $U - \alpha V$ is negative, the weight between activator u_1 and inhibitor v_2 (illustrated by a slant resistor symbol in Fig. 3) is increased because activators u_1 and u_2 should be anti-correlated. To this end, the output of interneuron W is given to two additional interneurons (f_{uu} and f_{uv}). Figures 3(a) and (b) shows the input-output characteristics of these interneurons. Namely, f_{uu} (or f_{uv}) is linearly increased when positive (or negative) $U - \alpha V$ is increased, but is zero when $U - \alpha V$ is negative (or positive). Those positive outputs (f_{uu} and f_{uv}) are given to weight circuit to modify the positive resistances. The dynamics of the "positive" weight between activators u_i and u_j is given by

$$\dot{W}_{ij}^{uu} = -W_{ij}^{uu} + f_{uu}, \quad (4)$$

and the "positive" weight between activator u_i and inhibitor v_j is

$$\dot{W}_{ij}^{uv} = -W_{ij}^{uv} + f_{uv}. \quad (5)$$

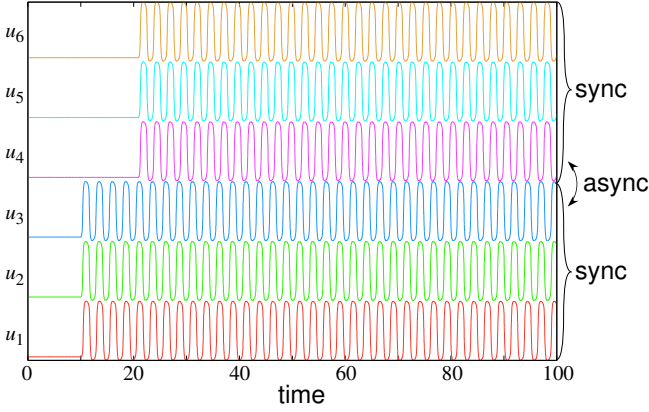


Figure 4: Numerical simulation results.

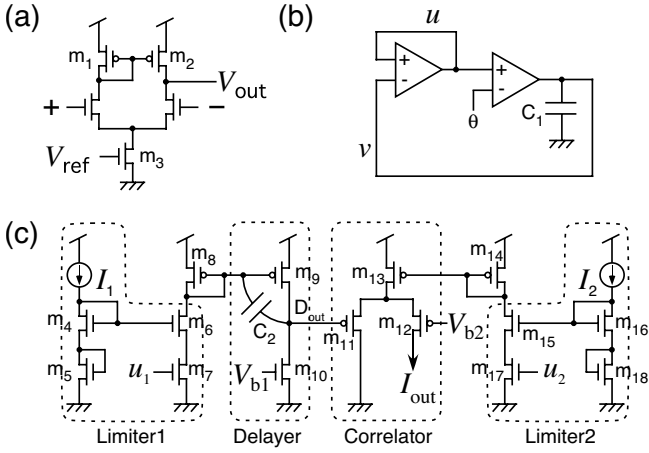


Figure 5: Unit circuits for neural segmentation; (a) differential amplifiers, (b) neural oscillator, and (c) STDP circuit.

We carried out numerical simulations with $N = 6$, $\tau = 0.1$, $\beta_1 = 5$, $\beta_2 = 10$, $d_1 = 2$, $d_2 = 0.1$ and $\alpha = 1.2$. Figure 4 shows time courses of activators u_i ($i = 1 \sim 6$). Initially, the external inputs θ_i ($i = 1 \sim 6$) were zero ($< \Theta$), but θ_i for $i = 1 \sim 3$ and $i = 4 \sim 6$ were increased to 0.5 ($> \Theta$) at $t = 10$ s and 20.9 s, respectively. We observed that $u_{1\sim 3}$ and $u_{4\sim 6}$ were gradually desynchronized without breaking synchronization amongst neurons in the same group, which showed that segmentation of neurons based on the input timing was successfully achieved.

3. CMOS unit circuits and operations

Our Wilson-Cowan based neural oscillators have been implemented in [5]. The oscillator uses standard differential amplifiers shown in Fig. 5(a) that consists of a differential pair (+ and -), a current mirror (m_1 and m_2) and a bias transis-

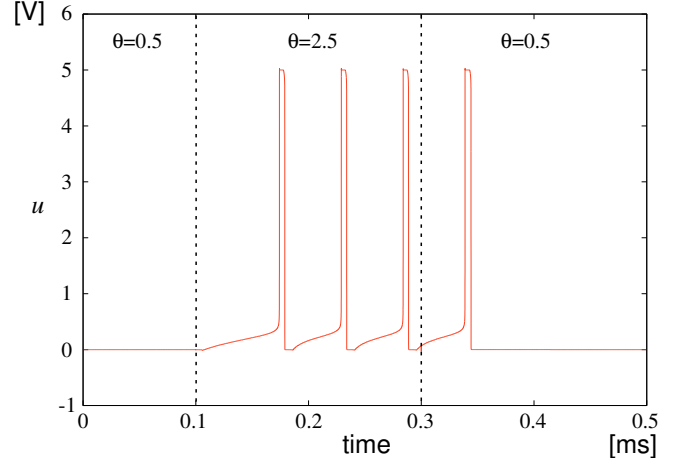


Figure 6: Simulation results of neural oscillator.

tor (m_3). Whole construction of a neural oscillator including additional capacitor C_1 is illustrated in Fig. 5(b). Figure 5(c) shows a circuit implementing the Reichardt's basic unit in Fig. 2(a). For practical purposes, we added two limiters that convert voltage pulses of u_1 and u_2 , which vary from 0 to V_{dd} , into subthreshold current pulses. Bias current I_1 drives m_4 and m_5 . Transistor m_6 is thus biased to generate I_1 because m_4 and m_6 share the gates. When m_7 is turned on (or off) by applying V_{dd} (or 0) to u_1 , I_1 is copied (or isn't copied) to m_8 . Transistors m_8 and m_9 form a current mirror, whereas m_9 and m_{10} does a pMOS source-common (inverting) amplifier whose gain is increased as $V_{b1} \rightarrow 0$. Since parasitic capacitance C_2 is significantly amplified by this amplifier, temporal changes of u_1 are blurred on the amplifier's output (D_{out}). Therefore this "delayer" acts as a delay neuron in Fig. 2(a). A correlator circuit consists of a pMOS differential pair (m_{11} and m_{12}) and a bias transistor (m_{13}). When $u_2 = V_{dd}$ (or zero), I_2 is copied (or isn't copied) to m_{13} through m_{15} to m_{18} , as explained above. Therefore, output current I_{out} is obtained only when $u_2 = V_{dd}$. Under this condition, I_{out} is proportional to $D_{out} - V_{b2}$ for small $|D_{out} - V_{b2}|$. This operation corresponds to that of a correlator in Fig. 2(a).

We carried out circuit simulations of the circuits above. The parameter sets we used for the transistors were obtained from MOSIS AMIS 1.5- μm CMOS process. Transistor sizes of m_1 , m_2 , m_3 , m_{13} and m_{14} were fixed at $L = 16 \mu\text{m}$ and $W = 4 \mu\text{m}$ to construct accurate current mirrors. Sizes of the resting transistors were set at $L = 1.6 \mu\text{m}$ and $W = 4 \mu\text{m}$. The supply voltage was set at 5 V.

Figure 6 shows simulation results of a neuron circuit with $C_1 = 10$ pF and $V_{ref} = 2$ V. Time courses of the activator unit (u) are plotted. Initially, θ was set at 0.5 V (in relaxing state), and u didn't oscillate. Then θ was increased to 2.5 V

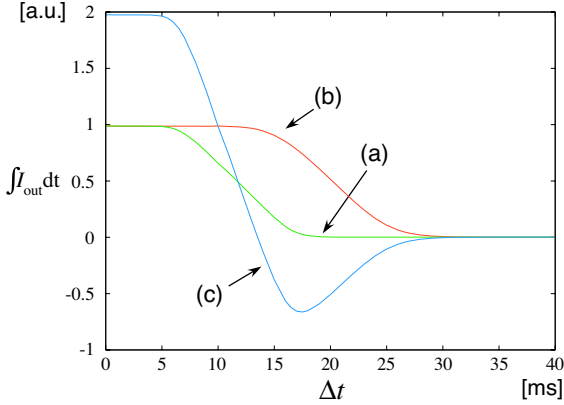


Figure 7: Ideal STDP characteristics without limiters.

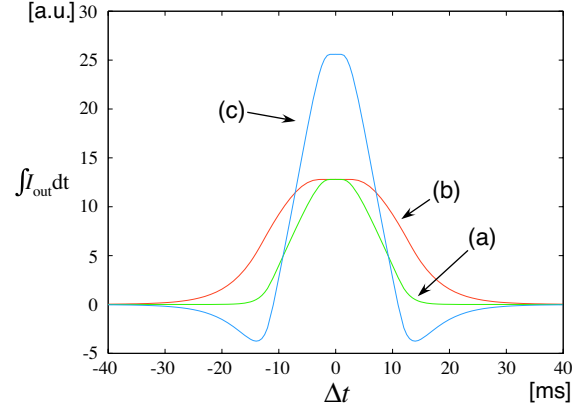


Figure 8: Symmetric STDP characteristics with limiters.

at $t = 0.1$ ms, and u exhibited stiff oscillations. Again, θ was set at 0.5 V at $t = 0.3$ ms. Since u had been excited before this time, the neuron emitted one spike and then relaxed, as expected.

Figures 7 and 8 show simulation results of our STDP circuits. In Fig. 7, ideal current pulses (amplitude: 100 nA, pulse width: 10 ms) instead of limiters were used in Fig. 5(c). Parameters C_2 , V_{b1} and V_{b2} were set at 100 fF, -0.2 V and 3.7 V. The value of V_{b2} was set at the intermediate value of m11's maximum and minimum gate voltage, and this makes the differential pair's output vary the most. The value of V_{b1} was chosen so that the delayer makes a reasonable delay. Horizontal axes (Δt) in Figs. 7 and 8 represent time intervals of input current pulses (spikes). We integrated I_{out} during the simulation and plotted normalized values [(a) in Fig. 7]. Then we changed the value of V_{b1} to -2 V. The lowered V_{b1} reduced the drain current of m10 and made the delay larger. Again, I_{out} was integrated and normalized. The result is plotted [(b) in Fig. 7]. Larger delay made the integrated I_{out} converge to zero at a larger Δt . By subtracting (b) from tripled (a), we obtained half characteristics of STDP learning (c) in Fig. 7. In Fig. 8, voltage pulses (amplitude: 5 V, pulse width: 10 ms) were applied to u_1 and u_2 in Fig. 5(c). Parameters C_2 and V_{b2} were set at 5 pF and 3.7 V. The integrated I_{out} s were plotted in Fig. 8(a) for $V_{b1} = 0$ and Fig. 8(b) for $V_{b1} = -0.04$ V. The result was qualitatively equivalent to the STDP characteristics shown in Fig. 2(d).

4. Conclusion

In this paper, we proposed a simple neural segmentation model that is suitable for analog CMOS implementation. First, instead of employing negative weights required for anti-correlated oscillation among different segments, we introduced positive connections between activators and inhibitors among different neuron units. Second, we proposed

a novel segmentation method based on a symmetric spike-timing dependent plasticity (STDP). The STDP characteristics were produced by combining Reichardt's correlation neural networks that are suitable for analog CMOS implementation. The proposed segmentation network was demonstrated through numerical simulations. Basic circuits for constructing segmentation hardware were proposed and evaluated. We showed that our circuit could produce symmetric STDP characteristics. Our next target is to setup the whole segmentation network with the proposed circuits.

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