Neuromorphic MOS Circuits Implementing a Temporal Coding Neural Model

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Abstract

A model for the storage of temporal sequences was proposed. On the basis of this model, we propose a neural model suitable for implementation on CMOS circuits that is capable of learning and recalling temporal sequences. In this paper, we numerically confirmed basic operations of the model and demonstrate fundamental circuit operations using a simulation program with integrated circuit emphasis (SPICE).

1. Introduction

Many real-world tasks demand the ability of natural, or artificial neural systems to process patterns in which the information content depends on the temporal order of the input patterns. In consequence, temporal information processing is of fundamental importance in various brain functions. The brain routinely learns and recalls information as the environment changes over time. This set of temporally ordered patterns is commonly referred to as "spatio-temporal sequence learning". The processing of such sequences is a topic arising in several fields, such as pattern recognition.

In [1] Fukai proposed a model for the storage of temporal sequences. Based on this model, we propose a neural model being suitable for implementation on CMOS circuits that is capable of learning and recalling temporal sequences. The model consists of neural oscillators connected to an output cell through synaptic connections. The basic idea is to learn input sequences, by superposition of rectangular periodic activity (oscillators) with different frequencies.

In the following sections, we explain the operation of the temporal coding model. Then we present the CMOS circuit for implementing the model. Finally we demonstrate the operation of the network using a simulation program with integrated circuit emphasis (SPICE).

2. The model

The main purpose of the model [1] is learning and memorizing the input stimuli ($I(t)$). The temporal coding model

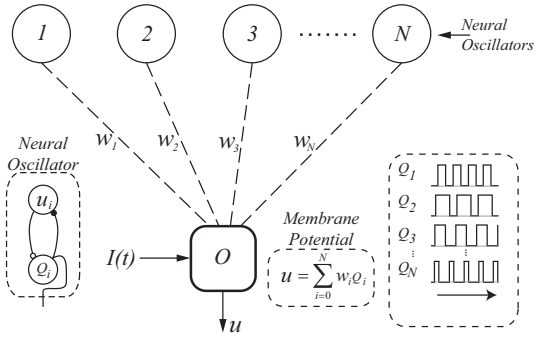

Figure 1: Temporal coding model.

is shown in Fig 1. The model consists of N neural oscillators (Q_i) with different oscillation frequencies and an output terminal cell O. One oscillator is composed of a pair of excitatory and inhibitory cells (u_i and v_i) based on the Wilson-Cowan model [2], [3]. All the oscillators are connected to the output cell O through synaptic connections. The input sequence $I(t)$ is given to the output cell as a supervisory signal. The synaptic weights, w_i, are strengthened (weakened) when the Q_i's oscillatory cells overlap (or not) with the input sequence $I(t)$, and then, the output cell O to reproduce the temporal sequences. The weights w_i are modified according to the gradient descent rule ($\delta w_i \sim -\partial E/\partial w_i$), where E is the *mean square error* of the learning given by:

$$E = \frac{1}{2T}\int_0^T [I(t) - u(t)]^2\, dt \tag{1}$$

where u is the membrane potential of O given by $u = \sum_{i=1}^{N} w_i V_{Q_i}$, and then δw_i becomes:

$$\delta w_i \sim -\frac{\partial E}{\partial w_i} = \frac{1}{T}\int_0^T [I(t) - u(t)] V_{Q_i}\, dt \tag{2}$$

Numerical simulations were conducted to confirm the operation of the model. The simulation results are shown in Fig. 2. The number of neurons was set to $N = 200$, and the results were obtained after completing 100 learning cycles. As can

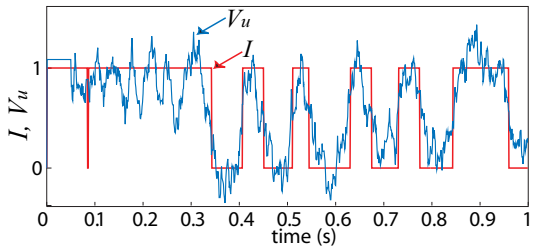

Figure 2: Model's simulation results. (N=200).

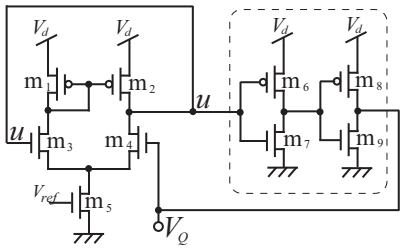

Figure 4: a) Neural oscillator circuit.

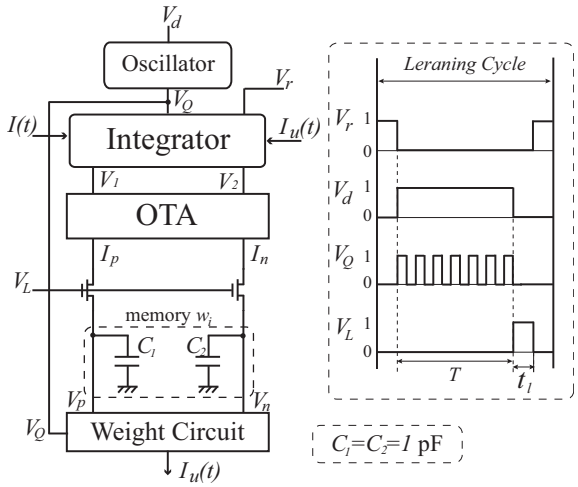

Figure 3: Single neuron circuitry.

be seen from the simulations, the time courses of membrane potential V_u are similar to those of input I.

3. CMOS circuits and operations

The basic structure of a single neuron of the temporal coding circuit is shown in Fig. 3. There is one oscillator with input V_d which acts as trigger signal for the oscillator. The output of the oscillator (V_Q) is given to the integrator, which calculates the weight difference δw (Eq. 2) by dividing the integral into two parts. Then, at the end of each learning cycle V_r is "1", and the integrator is reseted. The outputs of the integrator (V_1 and V_2) are given to the OTA which compares the two signals ($V_1 - V_2$) and outputs two currents, I_p for positive weight differences ($V_1 - V_2 > 0$) and I_n for negative weight differences ($V_1 - V_2 < 0$). Then, when V_L is "1" at the end of each oscillation cycle, T, the outputs (I_p and I_n) are integrated by capacitors C_1 and C_2 and thus converted to voltages (V_p and V_n). Finally these voltages are given to the weight circuit, which compares the two weights (positive and negative) and gives the output of the model $I_u(t)$.

3.1. Oscillators

The construction of a single neural oscillator [3] is illustrated in Fig. 4. The oscillator consists of a differential pair (m_3-m_4), one current mirror (m_1-m_2), a bias transistor (m_5), and a buffer circuit composed of two standard inverters (m_6-m_7 and m_8-m_9). The oscillations are controlled by turning on/off the power supply (V_d). When V_d is 0 there is no oscillation, and when V_d is "1", the circuit starts the oscillations.

3.2. Integrator

The integrator calculates the weight difference δw (Eq. 2) by dividing the integral into two parts:

$$V_1 = \int_0^T I(t) V_{Q_i}\, dt \tag{3}$$

$$V_2 = \int_0^T I_u(t) V_{Q_i}\, dt \tag{4}$$

The integrator circuit is shown in Fig. 5. The input current (I) is copied to node V_1 through current mirror (m_7-m_1), when transistor m_3 is turned on (or off) by applying "1" (or 0) to V_Q current I is integrated (or is not) by capacitor C_1. The result (V_1) equivalent to the operation performed by Eq. (3). The same process is carried out for the input I_u and the result (V_2) equivalent to that of Eq. (4). Results of the integration (V_1 and V_2) are reset at the end of each learning cycle by applying "1" to V_r.

3.3. OTA

In practical hardware, neuron devices have to be connected by special devices with both positive and negative resistive properties. However, implementing negative resistance is difficult, so we convert the signals into currents and divide the output into a current for positive weights and a current for negative weights, as shown in Fig. 6 (a).

The OTA subtracts one output given by the integrator from the other ($V_1 - V_2$) and separates the results into two currents, I_p (when $V_1 - V_2 > 0$) and I_n (when $V_1 - V_2 < 0$). The OTA circuit, which consists of a differential pair and current

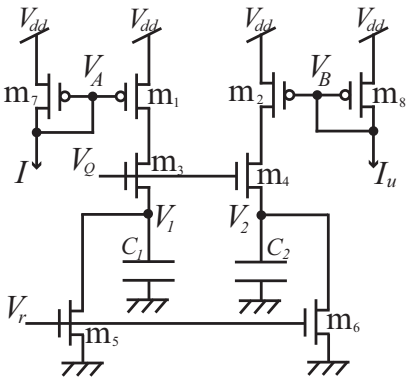

Figure 5: a) Integrator circuit.

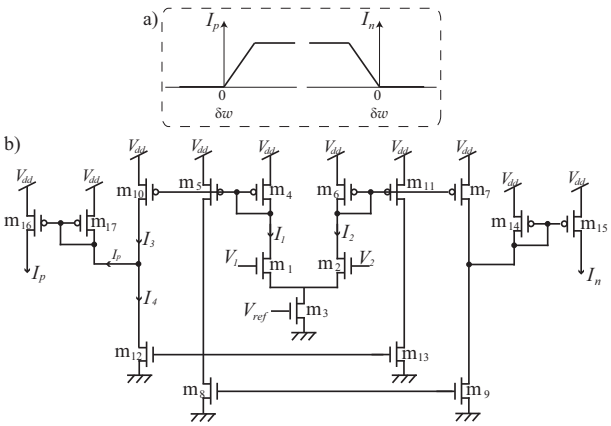

Figure 6: a) output characteristic for positive and negative weights, b) OTA circuit

mirrors, is shown in Fig. 6 (b). The current I_1 generated by V_1 is copied to I_3 by current mirror $m_4 - m_{10}$. At the same time current I_2 generated by V_2 is mirrored to I_4 by current mirrors $m_6 - m_{11}$ and $m_{13} - m_{12}$. When $V_1 > V_2$, current I_p ($I_p = I_3 - I_4$) flows and is copied to the output through current mirror $m_{17} - m_{16}$. The same process applies to output current I_n when $V_1 < V_2$.

3.4. Weight Circuit

At the end of the oscillation cycle, transistors m_1 and m_2 in Fig. 3 are turned on when V_L is "1". This updates weights V_p and V_n for positive and negative weights, respectively. These voltages are given to the weight circuit, which gives the output of the model ($V_B = \sum wV_{Q_i}$) by comparing the positive and negative weights, V_p and V_n. Our weight circuit is shown in Fig. 7. The circuit consists of a wide-range amplifier with

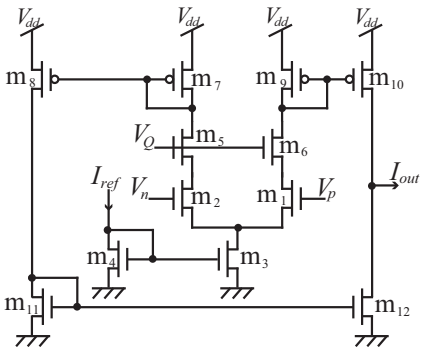

Figure 7: Weight circuit.

a small modification. Transistors m_5 and m_6 were added between the differential amplifier (transistors m_2 and m_1) and the current mirrors (transistors m_7 and m_9). In this way, the comparison of the weights ($V_p - V_n$) will be carried out only when V_Q is high.

4. Simulation Results

We conducted SPICE simulations of the complete model. We used TSMC 0.35 μm CMOS parameters. The number of neurons was set to 1. Figure 8 (a) shows the simulations of the oscillator. For the simulations we set $W/L = 2$ μm /0.24 μm for all transistors. V_{ref} was set to 450 mV. We observed from the simulations that at $t = 0.4$ μs V_d is turned on and the circuit starts the oscillation. Then, at $t = 0.8$ μs V_d is off. When V_d is turned on again and the circuit oscillates, "noticing that the oscillations start with the same phase as that of the previous oscillatory period is important". Simulation results of the integrator are shown in Fig. 8 (b). All transistor sizes were set to $W/L = 0.36$ μm/0.24 μm. Input currents for I and I_u were set to 1 μA and 2 μA, respectively. Capacitances C_1 and C_2 were set to 1 pF, and the supply voltage V_{dd} was set to 2.5 V. When V_r is equal to "1" (2.5 V) even if V_Q is "1", V_1 and V_2 are grounded and remain on 0. At $t = 0.25$ μs, V_r is 0 and V_Q remains "1". At this point currents I and I_u are integrated by the capacitors, so voltages at V_1 and V_2 increase. At $t = 0.5$ μs, V_Q is 0. There is no integration, and voltages V_1 and V_2 remain at the same voltages as those of the previous state. Then, V_r is "1" at $t = 0.75$ μs, and voltages V_1 and V_2 are reset to 0 (the capacitors were discharged). Simulation results for the OTA circuit are shown in Fig. 8 (c). Transistor sizes of m_7 and m_{10} were set to $W/L = 7.2$ μm/0.24 μm, m_9 and m_{12} to $W/L = 1.6$ μm/0.24 μm, and m_{14} and m_{17} to $W/L = 0.72$ μm/0.24 μm. The remainder of the transistors was set to $W/L = 0.36$ μm/0.24 μm. Voltage V_1 varies from 0 to 2.5 V. V_2 was set to 1.25 V. V_{ref} was set to 1 V, and the supply voltage was set to 2.5 V. When V_1 was less than V_2, current I_n is flowing and decreases as V_1 increases while I_p

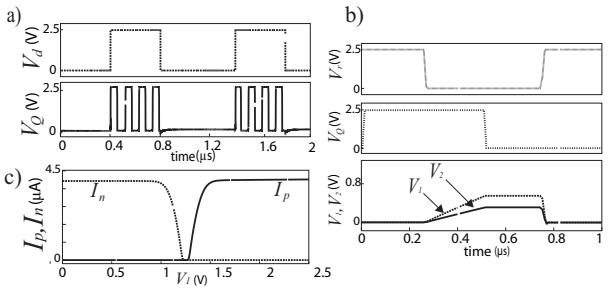

Figure 8: Simulation results of. a) oscillator, b) integrator, and c) OTA.

remains 0. When $V_1 = V_2$ both currents are 0. But as V_1 increases to a value greater than V_2, current I_p also increases while I_n remains 0 A.

We confirmed the operation of the model by converting the oscillator voltage V_Q into a curent I_Q and making the input current I equal to I_Q. Simulation results of the model are shown in Figs. 9 and 10. For the simulations, we set the leaning cycle to 1μs. Figure 9 (a) shows the corresponding V_q, V_r and V_L for one learning cycle. Capacitances C_1 and C_2 from Fig. 3 were set to 1 pF, and the supply voltage was set to 2.5 V. The output of the integrator is shown in Fig. 9 (b). We can observe that V_1 and V_2 are almost the same value after completing about ten learning cycles. This is because input I_u almost the same as input I, and the integrations of them (Eqs. 3 and 4) should also be the same. This confirms the operation of the model. The positive and negative weights (V_p and V_n) increase as currents I_p and I_n increase, as shown in Fig. 9 (c). As observed in Figs. 9 (b) and (c) when $V_1 > V_2$ the positive weight (V_p) increases, while when $V_1 < V_2$ the negative weight (V_n) increases, until both weights reach a point where none of them increases. The voltage on node V_A and voltage at node V_B (Fig. 5) are shown in Fig. 10. We can observe from the graphic that at the beginning of the learning V_A and V_B are different, but after about ten learning cycles the results are the same.

5. Conclusion

In this paper, we designed a neural circuit for temporal coding. The network circuit was designed using metal-oxide-semiconductor (MOS) devices. The model consists of N oscillatory units connected to an output cell through synaptic connections. To facilitate the implementation of the model, instead of using negative connections required for the implementation of negative weights, we used current signals and divide the weights into two currens: one for positive weights and one for negative weights. We demonstrate the operation of each component of the network separately using a simulation program with integrated circuit emphasis (SPICE). Finally, by making the input current equal to the oscillator current, we confirmed operations of the complete model with one neuron, and we confirmed that after ten leaning cycles the output and the input have the same phase.

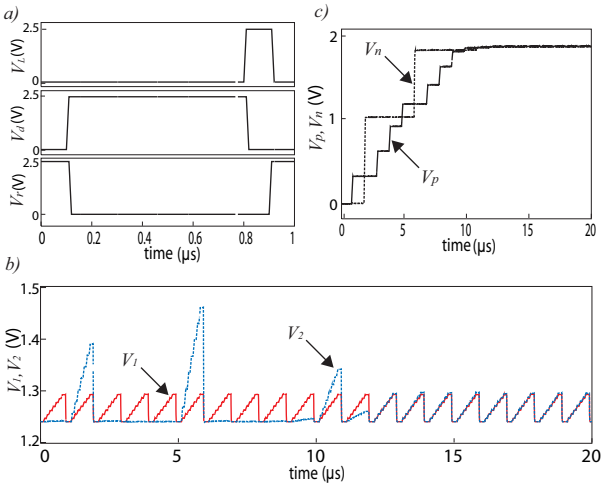

Figure 9: Simulation results. a) shows the plot of V_L V_d and V_r, b) integrator output V_1 and V_2, and c) positive and negative weights V_p and V_n.

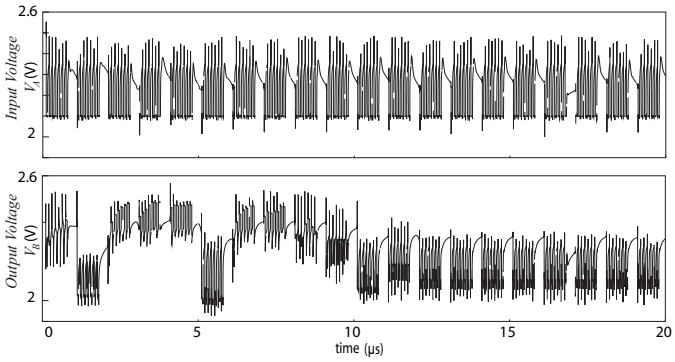

Figure 10: Input A and output V_u, simulation results.

References

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