Noise-induced Phase Synchronization in Digital Counters

Masakazu Matsuura*, Tetsuya Asai, and Masato Motomura

Graduate School of Information Science and Technology, Hokkaido University

Phase locking is very important task among isolated digital systems for their synchronous operations; *e.g.*, communication between two digital systems where a "sender" and a "receiver" are operating with the same clock frequency, but their initial phases are different, which may result in mis-capturing of data at the receiver. The present solution is to employ a "phase lock loop", which accepts a clock of the sender, compensates the difference between the sender's clock phase and the receiver's phase, and then acts as a clock source of the receiver. Noise-induced phase synchronization may be utilized in this phase-lock operation; *i.e.*, a "sender" and a "receiver" operating with the same clock frequency, but having different initial phases, could be synchronized by applying common noises. To confirm this, we designed a simple digital oscillator that can accept temporal noises.

To observe noise-induced phase synchronization, each oscillator has to implement the following features; i) the oscillator's state is represented by two logical values depending on the phase ϕ (state "0" for $0 < \phi < \pi$ and state "1" for $\pi < \phi < 2\pi$), ii) the oscillator accepts noises as a pulse at time t_i, iii) when $t = t_i$, the phase must be advanced if oscillator's state is "0", whereas the phase must be delayed if the oscillator's state is "1". We employ a conventional digital counter where the MSB (most significant bit) of the counter represents the oscillator's two states. In state "0", whenever the oscillator accepts noise pulses, the counter "up-counts" the noise pulse (the phase is advanced), whereas in state "1", the counter's clock input is suppressed by the noise pulse (the phase is delayed). Therefore the counter's input clock (CCK) is represented by $\overline{\mathrm{MSB}} \cdot n + \mathrm{CK} \cdot \overline{n}$, where MSB represents the most significant bit of the counter, n the noise pulse, and CK the system clock. When n = "0", the counter up-counts CK only, regardless of the value of MSB. When n = "1" and MSB = "0", the counter up-counts the noise pulse only, whereas CCK = "0" when n = "1" and MSB = "1", which result in blocking the up-counting. Figure 1 shows circuit diagrams of the oscillator.

In the experiments, we employed two 4-bit counters. Figure 2 shows experimental results (time evolution) of counter values of the circuits. They accepted a common system clock and common noises generated by a 16-bit M-sequence circuit (Galois LFSR). The initial phase difference was set at π. After around 3200 iterations, the circuits were synchronized. The synchronization may be disturbed when the phases of the system clocks of the oscillators are different, but one may expect that it may be compensated if one increases the counter's bits, because the phase difference is roughly given by $1/2^N$ where N represents the counter's bit. Figure 3 shows numerical simulation results exhibiting correlation values between the counter values versus the counter's bit (N), where the phase difference between the system clock was set at π (maximum). From this, we conclude that isolated digital oscillators having different clock phases could be synchronized if we employ 9-bit digital counters.

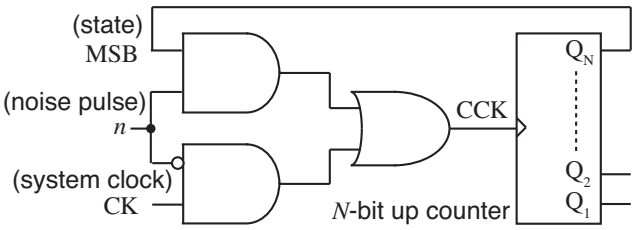

Fig. 1. Noise-driven digital oscillator (counter+α).

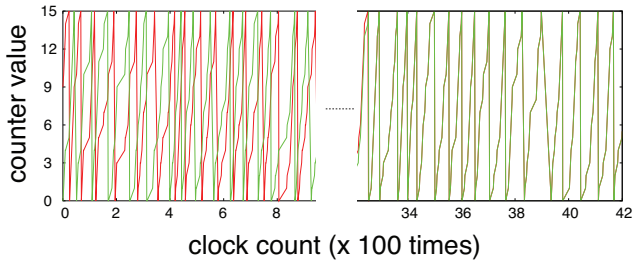

Fig. 2. Synchronization among two oscillators.

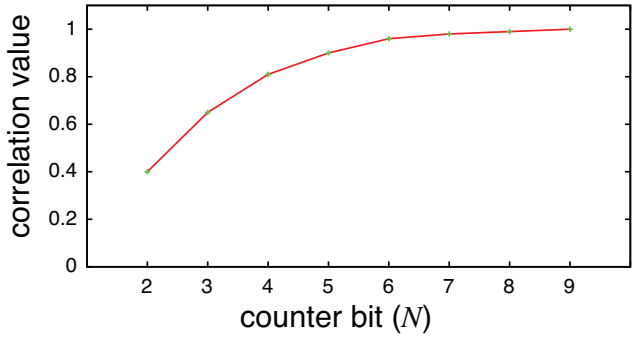

Fig. 3. Synchronization among isolated oscillators.

*email: matsuura@lalsie.ist.hokudai.ac.jp