A ReRAM-based analog synaptic device having spike-timing-dependent plasticity

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We propose an elemental device for possible brain-inspired hardware; i.e., analog synaptic devices (circuits) that consists of a bipolar ReRAM, an nMOS FET and a capacitor only. The device has an ability to update the synaptic conductance according to the spike timing of pre- and post neuron devices. We demonstrate the fundamental operations by using a fabricated ReRAM device of NiO thin films and discrete devices.

One of the key issues for implementing neural networks on semiconductor integrated circuits is "how we implement non-volatile analog synapses". Many engineers have tried to design analog synaptic devices based on existing flash-memory technologies, but they had difficulties in designing associate controllers for electron injection and ejection as well as increasing the limited frequency of the rewriting. Using possible memristive nano-junctions, a digital-controlled neural network has been introduced by Snider in 2007 [1]. We here propose yet-another analog approach; i.e., a ReRAM-based analog synaptic circuit, for possible neuromorphic computers. Our key idea is to assign a capacitor in one terminal of a ReRAM, as shown in Fig. 1. An input node of the ReRAM accepts voltage spikes (V1 in Fig. 1), and the other node is connected to a gate terminal of a MOSFET (M1) and a capacitor (C). This capacitor is charged or discharged by the input spike via the ReRAM. Because a MOSFET has nonlinear characteristics between the gate voltage and the drain current, by integrating the drain currents (IPSC in Fig. 1) on the other (membrane) capacitor, we obtain different membrane potentials for different conductance of the ReRAM. If the membrane potential exceeds a given threshold voltage, a post neuron circuit (standard integrate-and-fire circuit) generates a voltage spike (V2 in Fig. 1), and reset the membrane potential. At the same time, the gate node (PSP) is shunted by an additional MOSFET (M2). Therefore, due to the potential difference between two nodes of the ReRAM, the conductance is increased, which exhibits basic spike-timing-dependent plasticity (STDP) in our ReRAM synapse, i.e., the timing difference between pre-synaptic and post-synaptic spikes (Δt) results in the differential synaptic weights (differential conductance of the ReRAM). Figure 2 shows experimental results of our synaptic device. In the experiments, we used a fabricated bipolar ReRAM of NiO thin films (Pt-NiO-Pt) and a discrete MOS device (2SK1398) and a capacitor (0.1 μF). The result clearly showed that the differential conductance (Δg) was modified by the difference of spike timings of pre- and post-synaptic neurons (Δt).

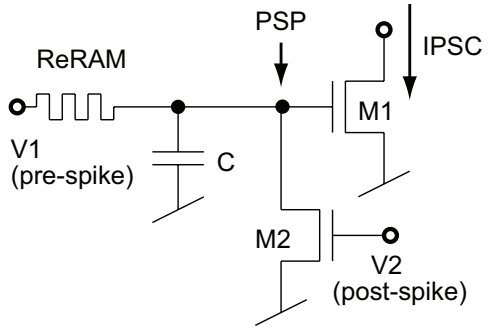

Fig. 1: Proposed STDP synapse circuit.

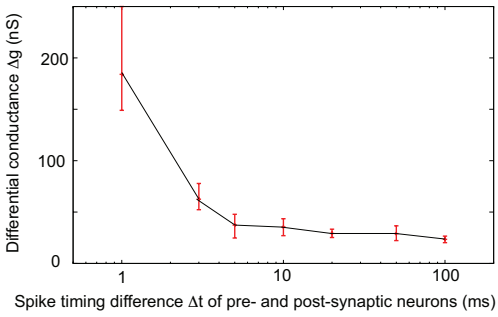

Fig. 2: Experimental results (STDP curve).

References

[1] G.S. Snider, Nanotechnology, **18**(36), 365202, 2007.