A MOS CIRCUIT FOR THE LOTKA-VOLTERRA CHAOTIC OSCILLATOR

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Abstract— *This paper presents an analog integrated circuit (IC) that implements the Lotka-Volterra (LV) chaotic oscillator. The LV system describes periodic or chaotic behaviors in prey-predator systems with a simple mathematical form. The proposed circuit consists of a small number of metal-oxide-semiconductor field-effect transistors (MOS FETs) operating in their subthreshold region, which is very suitable for large-scale IC implementation. A general method for implementing the LV system on analog ICs is also presented.*

I. INTRODUCTION

The design of chaotic oscillators has been a subject of increasing interest during the past few years [1]. Indeed, analog integrated circuits that implement chaotic oscillatory systems provide us important cues for exploring and discovering novel forms of information processing. Many designs of chaotic oscillators were introduced starting from the use of a coil in Chua's circuit to the use of large blocks such as operational amplifiers. In both cases, the fabrication area was very large. These designs were also dependent on the use of floating capacitors, the use of high supply voltage and high power dissipation, which is not preferred in fabrication due to the demanding need for portable devices in our world today. In this paper, we propose micropower analog MOS circuits that exhibit chaotic behaviors with very simple circuit construction.

II. ANALOG MOS CIRCUITS FOR THE LOTKA-VOLTERRA MODEL

The Lotka-Volterra (LV) model is one of the earliest predator-prey models to be based on sound mathematical principles. It forms the basis of many models used today in the analysis of population dynamics. We here employ a LV model that describes interactions between three species in an ecosystem, i.e.; one predator and two preys [2]. In addition to the predation of the preys, the two preys compete with each other for their feeding ground. The dynamics are given by

$$\tau \dot{x_1} = (1 - x_1 - x_2 - k\, y)x_1, \quad (1)$$

$$\tau \dot{x_2} = (a - b\, x_1 - c\, x_2 - y)x_2, \quad (2)$$

$$\tau \dot{y} = (-r + \alpha\, k x_1 + \beta\, x_2)y, \quad (3)$$

where x_1 and x_2 represent the prey population, y the predator population, τ the time constant, the rests (k, a, b, c, r, α and β) are control parameters.

By introducing three new variables:

$$X_1 = \ln x_1,\ X_2 = \ln x_2,\ Y = \ln y, \quad (4)$$

Eqs. (1), (2) and (3) can be transformed into:

$$\tau \dot{X_1} = 1 - \exp(X_1) - \exp(X_2) - k\exp(Y), \quad (5)$$

$$\tau \dot{X_2} = a - b\exp(X_1) - c\exp(X_2) - \exp(Y), \quad (6)$$

$$\tau \dot{Y} = -r + \alpha k \exp(X_1) + \beta \exp(X_2). \quad (7)$$

This transformation has two merit for analog MOS implementation: i) the resultant equations [(5), (6) and (7)] do not have multiplying terms of system variables and are described by linear combination of exponential functions, which enables us to design the circuit without any analog multiplier; ii) the exponential nonlinearity is essential characteristics of semiconductor devices, which enables us to design a circuit based on the intrinsic characteristics of semiconductors. We here use the exponential current-voltage characteristics of subthreshold MOS FETs [3].

In the subthreshold region of operation without body effect, the drain-source current of a saturated n-type MOS FET is given by

$$I_{\rm ds} = I_0\ \exp(\frac{\kappa}{V_T} V_{\rm gs}) \quad (8)$$

where $I_{\rm ds}$ represents the drain-source current, $V_{\rm gs}$ the gate-source voltage ($\geq 4V_T$ for saturation), κ the effectiveness of the gate potential, and $V_T \equiv kT/q \approx 26$ mV at room temperature (k is Boltzmann's constant, T the temperature, and q the electron charge), and I_0 the fabrication parameter. Typical parameter values for minimum-size devices fabricated in a standard 1.5-μm n-well process are $I_0 = 0.5 \times 10^{-15}$ A

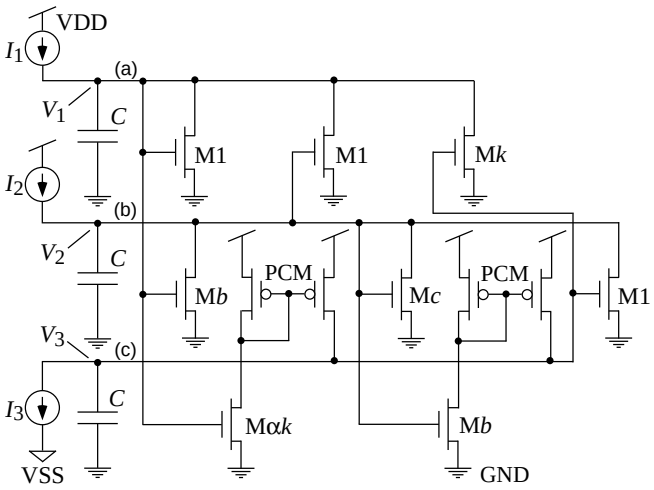

Fig. 1. Construction of LV circuit.

and $\kappa = 0.6$. Note that Eq. (8) is valid only when the MOS FET is saturated; i.e., $V_{\rm gs} \geq 4V_T$.

Figure 1 shows construction of the LV circuit. Applying KCL at node (a) and (b) in Fig. 1, we obtain

$$\begin{aligned} C\dot{V}_1 &= I_1 - I_0^{(\mathrm{M1})} \exp(\frac{\kappa}{V_T}V_1) - I_0^{(\mathrm{M1})} \exp(\frac{\kappa}{V_T}V_2) \\ &- I_0^{(\mathrm{M}k)} \exp(\frac{\kappa}{V_T}V_3) \qquad (9) \\ C\dot{V}_2 &= I_2 - I_0^{(\mathrm{M}b)} \exp(\frac{\kappa}{V_T}V_1) - I_0^{(\mathrm{M}c)} \exp(\frac{\kappa}{V_T}V_2) \\ &- I_0^{(\mathrm{M1})} \exp(\frac{\kappa}{V_T}V_3) \qquad (10) \end{aligned}$$

where $I_0^{(\mathrm{M}*)}$ the fabrication parameter. The node voltages V_1 and V_2 are also given to the gates of MOS FETs Mαk and M$_\beta$, respectively. Because the currents of Mαk and Mβ are copied to node (c) by two pMOS current mirrors (PCMs in Fig. 1), the node equation is represented by

$$\begin{aligned} C\dot{V}_3 = -I_3 + I_0^{(\mathrm{M}\alpha k)} \exp(\frac{\kappa}{V_T}V_1) + \\ I_0^{(\mathrm{M}\beta)} \exp(\frac{\kappa}{V_T}V_2). \qquad (11) \end{aligned}$$

Equations (9) to (11) become equivalent to Eqs. (5) to (7), respectively, when

$$\begin{aligned} V_i &= \frac{V_T}{\kappa}X_i,\ (i=1,2,3),\ \tau = \frac{CV_T}{i_0\kappa}, \qquad (12) \\ \frac{I_1}{i_0} &= 1,\ \frac{I_2}{i_0} = a,\ \frac{I_3}{i_0} = r, \qquad (13) \\ \frac{I_0^{(\mathrm{M1})}}{i_0} &= 1,\ \frac{I_0^{(\mathrm{M}k)}}{i_0} = k,\ \frac{I_0^{(\mathrm{M}b)}}{i_0} = b, \qquad (14) \\ \frac{I_0^{(\mathrm{M}c)}}{i_0} &= c,\ \frac{I_0^{(\mathrm{M}\alpha k)}}{i_0} = \alpha k,\ \frac{I_0^{(\mathrm{M}\beta)}}{i_0} = \beta, \qquad (15) \end{aligned}$$

where i_0 represents the normalized current.

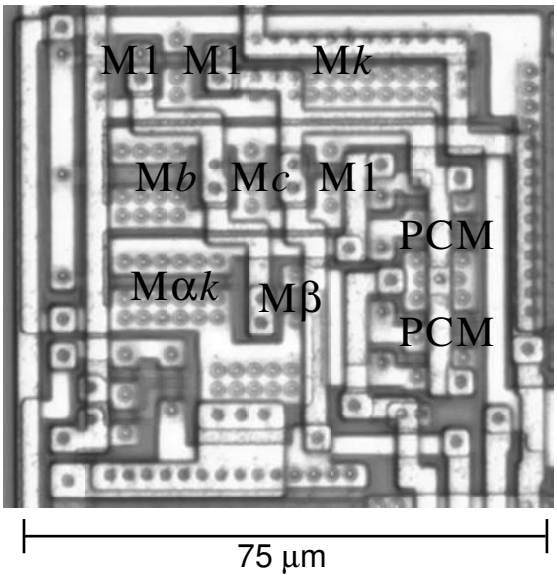

Fig. 2. Chip micrograph of a fabricated LV circuit (MOSIS, vendor: AMIS, n-well single-poly double-metal CMOS process, feature size: 1.5 μm, total area: 75 μm $\times$ 40 μm).

MOS FET	W (μm)	L (μm)
M1	4	1.6
Mb	12	3.2
Mc	4	1.6
Mk	40	1.6
Mαk	20	1.6
Mβ	4	3.2

TABLE I
SIZE OF NMOS FETS ON LV CHIP.

III. EXPERIMENTAL RESULTS

We fabricated a prototype circuit using a 1.6-μm scalable complementary-MOS (CMOS) rule (MOSIS, vendor: AMIS, n-well single-poly double-metal CMOS process, λ = 0.8 μm, feature size: 1.5 μm). Figure 2 shows a micrograph of the LV circuit. We employed the same parameter set of the LV system ($k = 10$, $b = 1.5$, $c = 1$, $\alpha k = 5$, $\beta = 0.5$) as in [2] where a stable focus bifurcates into chaotic oscillation via stable period-n cycles. The resultant size of nMOS FETs are listed in Tab. 1. The pMOS current mirrors (PCM) were designed with a dimension of W/L = 4 μm / 1.6 μm. The circuit took up a total area of 75 μm $\times$ 40 μm.

In the following experiments, we added external capacitors (C = 0.1 μF) out of the chip due to the time resolution of our measurement systems. We used Ag-

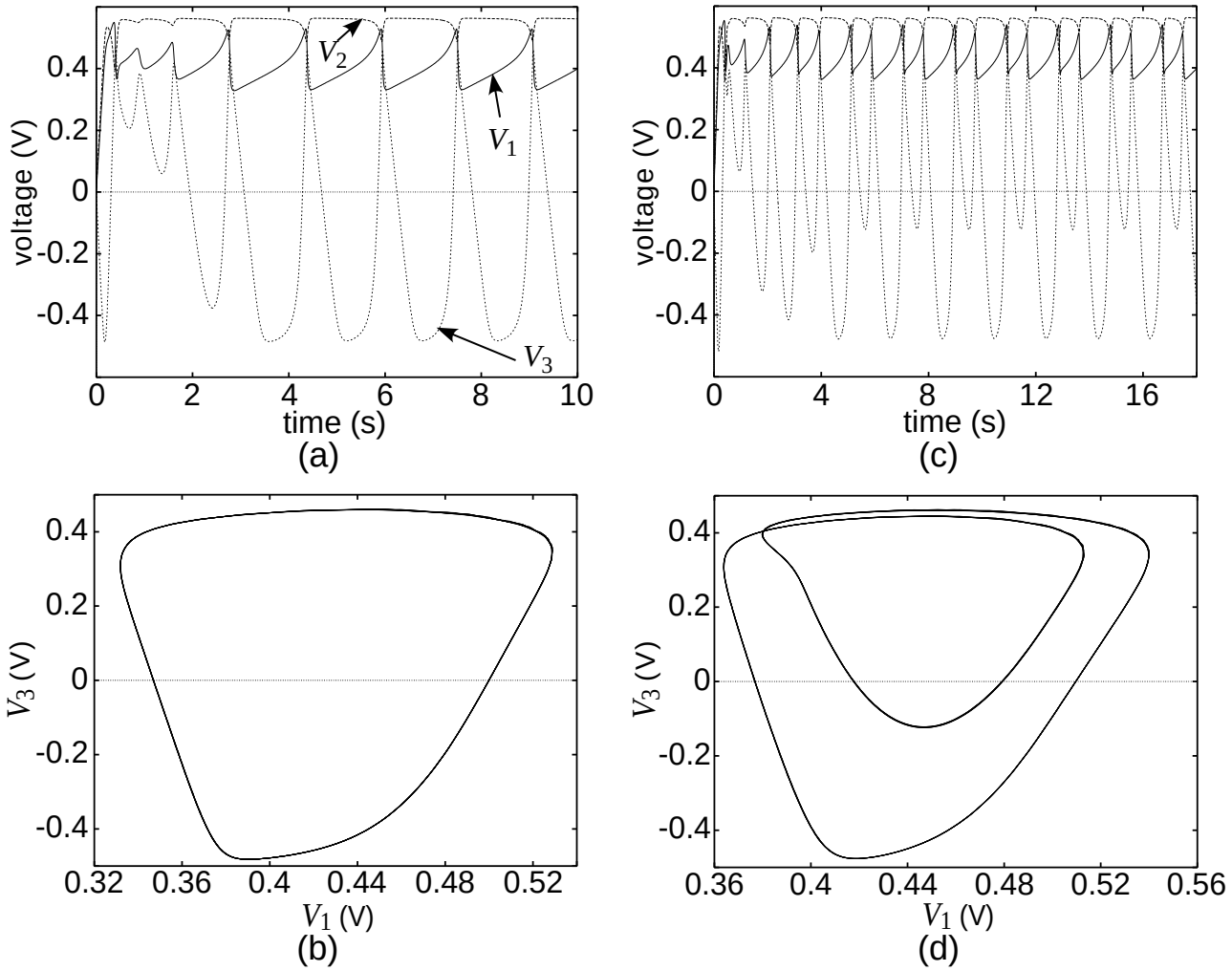

Fig. 3. Experimental results of fabricated LV circuit. (a) and (c) show time course of system variables (V_1, V_2 and V_3). (b) and (d) show trajectories on a V_1-V_3 plane. (a) and (b) represent results for I_3 = 320 nA, while (c) and (d) results for I_3 = 360 nA.

ilent 4156B as external current sources for the input. Time courses of V_1, V_2 and V_3 were sampled simultaneously by Agilent 4156B. The supply voltage (VDD) was set at 2.5 V. The input currents (I_1, I_2) were fixed at (250, 287) nA. We examined dynamic behaviors of the fabricated LV circuit by changing the rest input current I_3 that corresponds to the control parameter r in (3).

Figure 3 shows the measurement results. Figures 3(a) and 3(b) show the time course of the system variable (V_1, V_2 and V_3) and trajectories on a V_1-V_3 plane, respectively. In this experiment, I_3 was set at 320 nA. The LV circuit exhibited stable oscillation with period-1 cycles. In Figs. 3(c) and 3(d), which represent the time course of the system variable and trajectories on a V_1-V_3 plane, respectively, I_3 was set at 360 nA. The LV circuit exhibited stable oscillation with period-2 cycles. Figures 4(a) and 4(b) show the time course of the system variable and trajectories on a V_1-V_3 plane, respectively. In this experiment, I_3 was set at 420 nA. The maximum value of the Lyapunov exponents was 10.1, which indicated that the LV circuit exhibited chaotic oscillation.

We confirmed whether the qualitative behavior of the circuit is consistent with the theoretical analysis. According to [2], as the value of the control parameter r increases from r_1 to r_2, the Hopf bifurcation occurs at $r \equiv r_\alpha$ and $r \equiv r_\beta$ where the stable focus bifurcates ($r_1 < r < r_\alpha$) to the unstable focus with enclosing limit cycle ($r_\alpha < r < r_\beta$). Then the unstable focus bifurcates to the stable focus ($r_\beta < r < r_2$). We confirmed this transition (stable focus $\rightarrow$ unstable focus with enclosing limit cycle $\rightarrow$ stable focus) in the LV circuit during the increase of I_3 ($\sim r$). Figure 5 shows the bifurcation diagram obtained from the LV circuit. The diagram was created as follows: 1) when

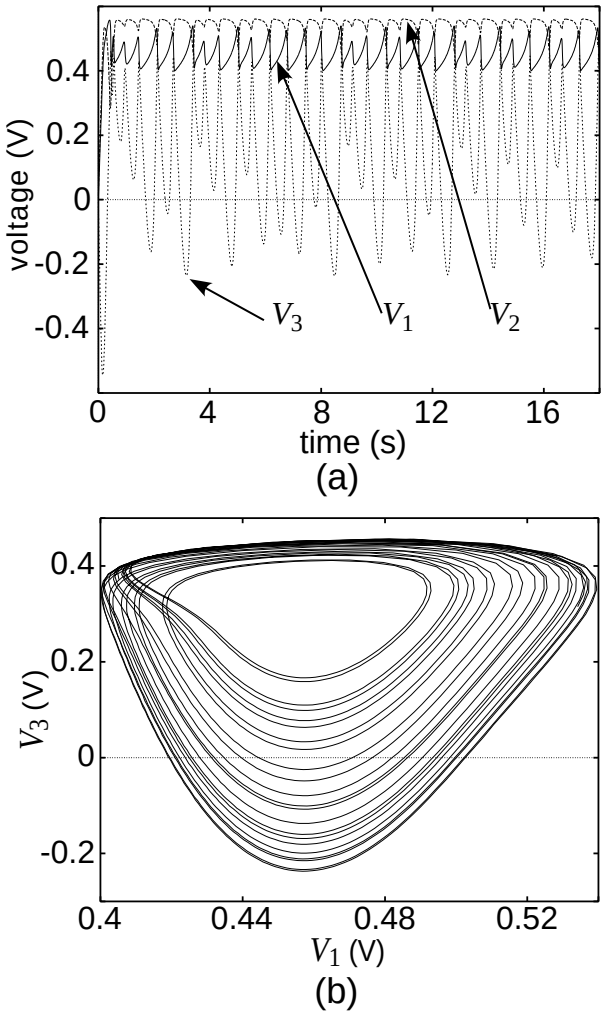

Fig. 4. Experimental results of fabricated LV circuit. (a) and (b) show time course of system variables (V_1, V_2 and V_3) trajectories on a V_1-V_3 plane, respectively, when I_3 = 420 nA.

the circuit had stable focus with a given I_3, the stable value of V_3 was plotted, 2) when the circuit oscillated with a given I_3, the value of V_3 at which $\dot{V}_3 = 0$ was plotted. When $I_3 < 182$ nA, the LV circuit did not oscillate (stable focus). The stable focus bifurcated at $I_3 \approx 182$ nA to stable period-1 cycles. Increasing the value of I_3, further bifurcations to period-2 cycles, period-4 cycles, chaotic cycles occurred around 370 nA $< I_3 <$ 450 nA. Finally, the unstable focus bifurcated to a stable focus again at $I_3 \approx 580$ nA.

The results in Fig. 5 indicates two important properties of the proposed LV circuit: 1) although we used practical subthreshold MOS FETs, the bifurcation property is qualitatively consistent with the result of theoretical analysis; 2) the LV circuit exhibits stable oscillation with period-n and chaotic cycles over a wide range of I_3; i.e., 182 nA $< I_3 <$ 580 nA,

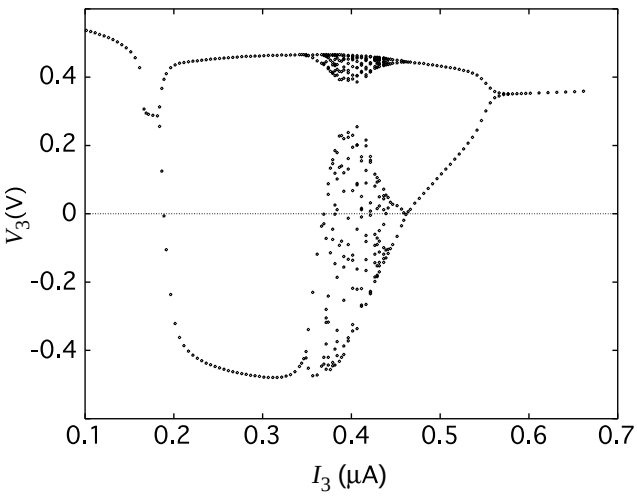

Fig. 5. Bifurcation diagram of LV circuit.

which allows the LV circuit to keep stable oscillation under noisy environment, even though the subthreshold MOS FETs were used in the circuit.

IV. Summary

We proposed an analog integrated circuit (IC) that implements the Lotka-Volterra (LV) chaotic oscillator. We designed very simple (just 12 transistors) circuit for the LV oscillator where all transistors operated in their subthreshold region. The LV oscillator was fabricated using a 1.6-μm scalable rule (MOSIS, vendor: AMIS, n-well single-poly double-metal process, λ = 0.8 μm, feature size: 1.5 μm). The circuit took up a total area of 75 μm $\times$ 40 μm. Although the quantitative results of the fabricated circuit were inconsistent with the theoretical analysis, the qualitative behavior (bifurcation property) agreed well with the result of theoretical analysis. Furthermore, the LV circuit exhibited stable oscillation with period-n and chaotic cycles over a wide range of control current, which enables us to design a stable oscillator that can operate under noisy environment, even though the subthreshold MOS FETs were used in the circuit.

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