Asynchronous Digital Circuit Design using Noise-Driven Stochastic Gates

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Abstract—
This paper presents a novel CMOS configuration of the basic logic gates using the concept of stochastic resonance (SR). In this framework, the SR effect applied to nonlinear electrical systems to build logical gates (SR gates) have been studied. These systems exhibit hysteresis; this property is crucial, because it ensures the stability of all logic states. Moreover, the application of an external bias, allows the selection of logic operation. However, in this configuration the timing is limited, which has been reviewed in this study; therefore, the most suitable applications of the SR gates are in asynchronous circuit design. The Huffman model is used to simulate the performance of a sequential circuit, designed with the SR gates. SPICE simulations are run using a 0.18-μm CMOS technology. The simulations results have proven the effective performance of the SR gates for an optimal amount of noise, despite the introduction of an intentional mismatch between the threshold voltages of the transistors.

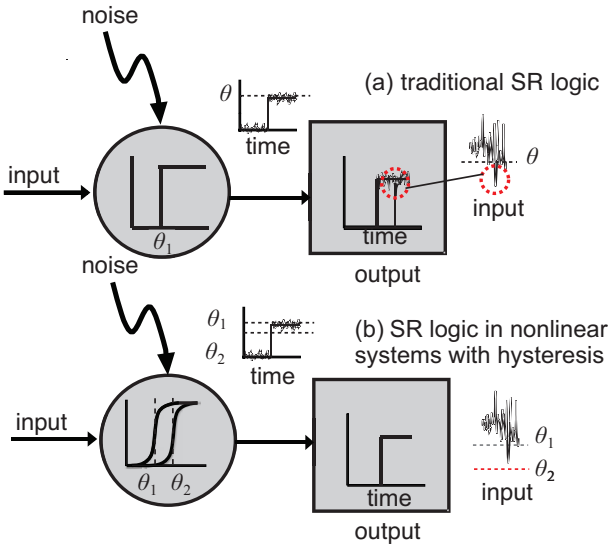

Figure 1: (a) Noise assistance in nonlinear systems with one threshold; (b) noise assistance in nonlinear systems exhibiting hysteresis.

1. Introduction

The use of an optimal amount of noise has proved to be an effective method to improve specific tasks. This effect is well-known as stochastic resonance (SR) [1]. One of the main applications of the SR effect is the improvement of the response of nonlinear systems to weak input stimuli [2]. A novel application of noise in nonlinear systems was proposed by Murali *et al*., where a certain range of noise serves to change the state in a bistable system; each state represents a logic state, and therefore the basic logic operations can be implemented by electrically modeling a double-well potential function with an additive Gaussian noise [4]; further, the precise values for the bias are necessary to set the logical operation, and this requires additional bias sources. Moreover, the implementation of this system is quite complex because it requires the use of several operational amplifiers and additional bias circuits, which is expensive in terms of VLSI. This paper proposes a novel configuration, by cooperative use of noise in nonlinear systems. The concept involves the electrical systems where the hysteresis phenomenon occurs. In this case, the presence of two thresholds prevents the activation of the output in the presence of large noise fluctuations. However, a main limitation is the timing of the SR gates. The delay time of the SR gate response is limited by the stochastic process; therefore, synchronization is the main limitation for the effective performance of high-complexity circuit configurations. However, a suitable alternative is the implementation of asynchronous circuits with the current SR gates, considering the lack of a common clock. This characteristic allows a more reliable design of the elements in the presence of delays, such as in the SR gate case. Further, the performance of the SR logic in a sequential asynchronous design has been demonstrated.

The reminder of this paper is organized as follows, Section 2 presents a description of the main idea of this work to design the stochastic resonance logic gates. The electrical simulations are presented also. Section 3 presents the simulation of one of the basic asynchronous models, the Huffman model, to demonstrate the performance of the current SR gates. Finally, Section 4 presents the conclusions of this work.

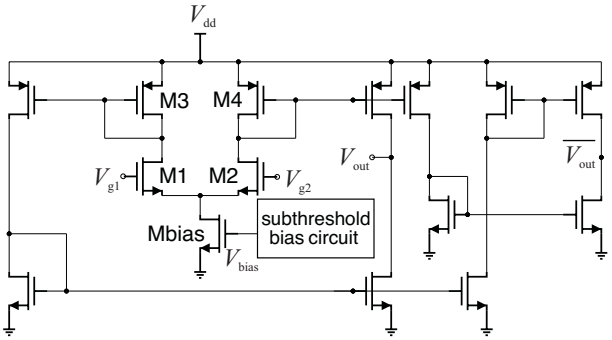

Figure 2: CMOS design of the SR gate.

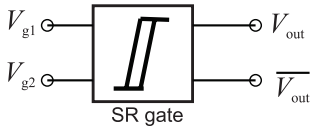

Figure 3: Generic symbol of SR gate.

Table 1: Selection of the logic operations according to V_{bias1} and V_{bias2}, and V_{out} and $\overline{V_{out}}$

V_{bias1}	V_{bias2}	$\overline{V_{out}}$	V_{out}
V_{dd}	0	OR	NOR
V_{dd}	V_{dd}	AND	NAND

2. Circuit Design of SR gates

The idea of this paper is based on the utilization of noise to build logic gates. The main design is based on electrical systems with hysteresis, which posses a double threshold. Traditionally, noise assistance has been used to improve weak signals detection in systems with one threshold. However, one evident problem is that a high-amplitude peak of the noise signal can trigger an unnecessary response (Fig. 1a). Generally this response has fluctuations and hazards; In our case, the double-threshold system avoids hazards as long as the noise amplitude remains lower than the difference between the two thresholds, therefore the logic state remains stable (Fig. 1b).

Figure 2 shows the proposed electrical diagram of the implementation of the SR gates. This configuration is a differential pair configuration where V_{g1} and V_{g2} denote the floating gates, and V_{out} and $\overline{V_{out}}$ are the outputs. V_{bias1} and V_{bias2} serve as selectors for the logic operations. The main concept is to indirectly vary the threshold of the transistors through an external bias. When the threshold varies, the input voltage required to activate the transistor of the differential pair, also varies. The generic symbol of a four-terminals SR gate is shown in Fig. 3. Table 1 lists the combinations of V_{bias1} and V_{bias2} to set either the NOR or the NAND operation with V_{out} as the output. By selecting $\overline{V_{out}}$ as the output, both the OR and the AND operations can be performed (Fig. 4). All the inputs of the differential pair are capacitively coupled, such as a floating gate MOSFET, and therefore the floating potential is the result of the weighted sum of their inputs. The introduction of noise (V_{noise}) aids in the detection of the weak input signals as well as to overcome the problem associated with the mismatch between the threshold voltages.

The circuit simulations are performed through a SPICE program using a 0.18μm CMOS technology. The power supply is set to 0.35 V and all the transistors are working in the subthreshold region. Additive Gaussian noise is introduced in V_{noise} with a mean value of 0, a standard deviation of 18mV and an offset voltage of V_{dd}. The SR effect is observed during simulations. For low values of standard deviation of noise, inputs do not exceed the threshold and there is no response; for high values of the standard deviation of noise, the circuit has unwanted spikes.

One well-known advantage of the subthreshold regimen is the reduction of the power consumption; however one implication, is the increase of the sensitivity of the threshold-voltage variations; particularly in the differential pair configuration, where a precise matching is required between the transistors. In this case, the introduction of noise actually helps to overcome this problem. During the simulations, the threshold voltage of M2 was intentionally varied by modifying it directly from its SPICE transistor model. Figure 5 shows the simulation results of the SR gates of the four basic logic gates.

On the other hand, the requirements of the asynchronous systems, differ from those of the synchronous ones. Therefore, in addition of the basic logic gates, there are some necessary configurations required to implement certain functions of the asynchronous logic. Such is the case of the C-element. This is a two-input configuration, where the output storages the previous state as long as both the inputs are different (Table 2). This configuration can be implemented as shown in Fig. 6 . In this case, the feedback allows the storage of the previous state, until both the inputs attain the same value. The simulation results are shown in Fig. 7 for a power supply of 0.35 V.

3. Design of asynchronous sequential circuits with SR gates

As mentioned in Section 1, the response of the stochastic logic gates is governed by the stochastic processes; therefore, the delay time of the SR gate response tends to be unpredictable for a certain time period. This timing limitation is crucial in circuits sharing a common clock, such as the synchronous circuits. In synchronous circuit designs, a precise synchronization among the signals must exist to ensure an effective performance. Therefore, SR gates find suitable applications in asynchronous circuits. The main characteristic of the asynchronous circuits is the use of handshaking among the circuit stages to achieve synchro-

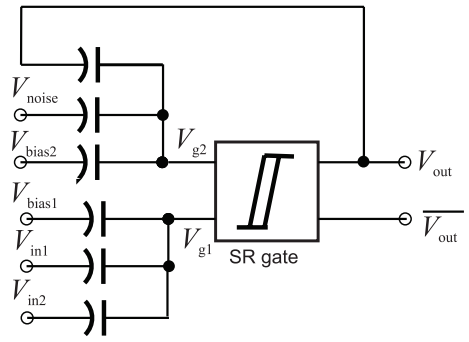

Figure 4: Configuration for the basic logic operations depends on the values of V_{bias1} and V_{bias2}.

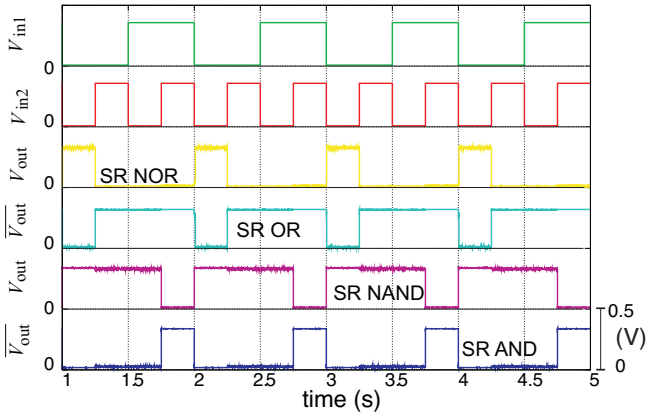

Figure 5: Simulation results of SR gate for NOR, OR, NAND and AND operations.

nization, to communicate with each other, and to complete all the tasks. Basically, by using the asynchronous logic, it is possible to model the existence of delays in the circuit elements. Such is the case of the Huffman asynchronous circuit model, which considers a bounded delay [0,U] for each element. This allows reliable circuit designs even in the presence of delays.

A simple sequential circuit design is presented in this paper, to prove the effective performance of the SR gates. This circuit design is based on the problem presented in [5], referring as the winery-shop-patron problem (Fig. 8), where the statement is as follows, the wine shop must request for wine to the winery (this action is denoted by the signal `req_wine`); once the wine arrives at the shop (the acknowledging of that request is denoted by `ack_wine`), the patron is called to pick the wine up (denoted by `req_patron`). Once the patron arrives to pick the wine up (acknowledging the request, denoted `ack_patron`), the process is complete. As shown in Fig. 8, the arrows denote the channels communications.

As the ”shop” is responsible for both the request (to the winery and the patron), it is said that the ”shop” is an active/active protocol. A common representation of these models is through asynchronous finite-state machine

Table 2: C-element state table

V_{in1}	V_{in2}	Y	Y_{next}
0	0	X	0
0	1	0	0
1	0	0	0
1	1	1	1
0	1	1	1
1	0	1	1
0	0	0	0

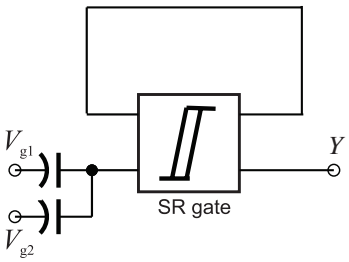

Figure 6: Configuration for the C-element.

(AFSM) diagram (Fig. 9). The circles denote the state and the arrows denote the transitions. It can be noted that a new variable state, `x` is introduced in order to reduce the number of states. The corresponding digital circuit can be obtained by Karnaugh map reduction. The implementation of the circuit is shown in Fig. 10, using the traditional logic gates. It can be noted that in this circuit, the delay elements are considered for all the components. In this case, any lack of desynchronization among the signals can be compensated by adding a feedback between the variables `x` and `X`. This feedback must contain the delay elements whose delay time is sufficient large to compensate for the internal delays.

Figure 11 shows the implementation of the active/active protocol by using the SR gates. In this circuit, the buffer can be implemented by using the same configuration as that of the SR-NAND with both the inputs connected to the same input. Similarly, a buffer can be implemented by using an SR AND, with one terminal connected to the logic 1. The simulation results are shown in Fig. 12, where the sequence of the winery problem is correctly performed.

4. Conclusion

The SR effect has been demonstrated to be an effective technique to detect weak stimuli in nonlinear systems. The main contribution of this study is the use the hysteresis characteristic of the differential pair configuration to avoid spontaneous hazards and high amplitude oscillations. Moreover, the proposed circuit can be used to implement the four basic logic gates, by simply varying the two external bias values, either to 0 or to V_{dd}. Owing to the fact that

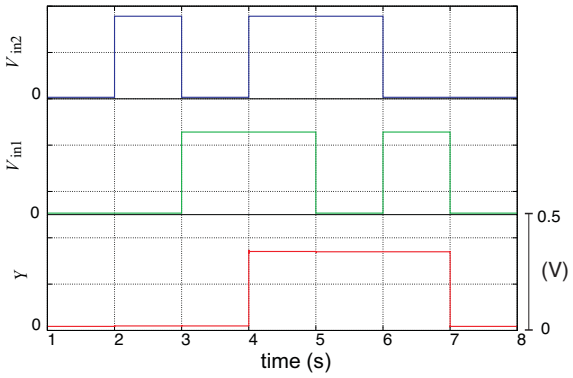

Figure 7: Simulation results for the C-element.

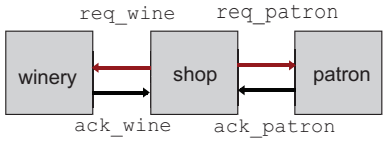

Figure 8: Block diagram for the winery-shop-patron problem

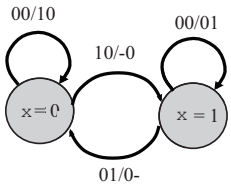

Figure 9: Asynchronous finite-state machine diagram of the active/active protocol

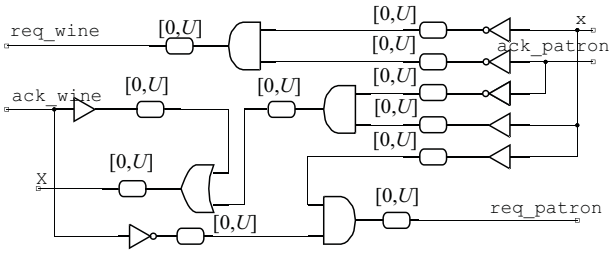

Figure 10: Circuit implementation (traditional logic gates) of the active/active protocol, based on Huffman model.

all the transistors are working in the subthreshold regime, the circuit achieves a low power consumption. According to the electrical simulations, power consumption is in the order of $\sim pW$. However a formal power and speed analysis will be done in further works for more complex configurations. Also the introduction of noise actually reduces the mismatch effect. The circuit simulations have demonstrated the effectiveness of using noise in the proposed configuration to build logical circuits. As a future work, asynchronous circuits with a higher level of complexity will be simulated by using the SR gates as a main element.

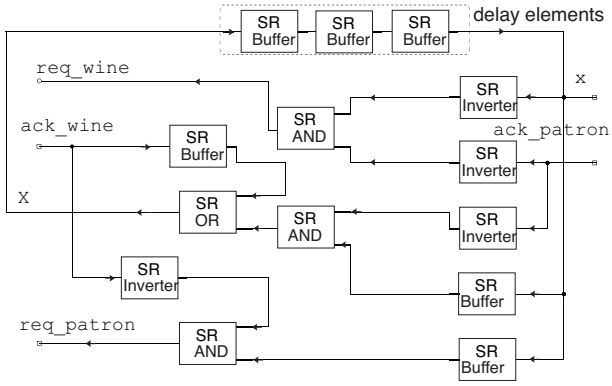

Figure 11: Circuit implementation of the active/active model with the SR logic gates

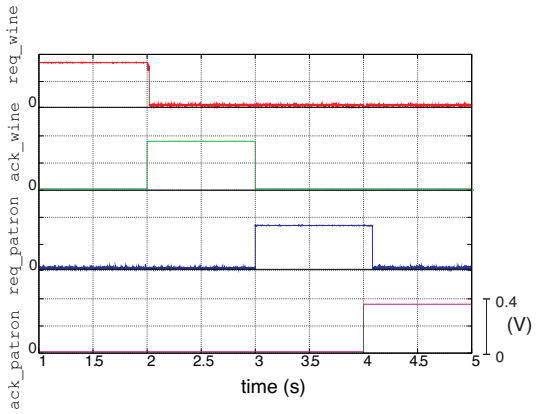

Figure 12: Simulation results for the active/active model using SR gates

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