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Stochastic Memory Devices with Simple Bistable Analog Circuits

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Abstract— In recent years, power-saving and compact Artificial Intelligence (AI) computers have become a necessity owing to their broad applications. Stochastic Computing (SC) is an economical approach to implementing multipliers and other required components for AI and processing them in parallel. However, SC-based computer architecture has issues in memory utilization. This study proposes a Stochastic Memory (SM) approach that addresses this issue using a simple bistable analog circuit. First, the operating principle required for the SM using potential diagrams is explained. Next, a circuit that satisfies the operating principle is explained, which can be realized using an operational amplifier and switches and latches. Finally, the evaluation of the proposed circuit as an SM is explained based on simulation results. We hope that this will provide a compact and power-efficient calculator based entirely on SC.

1. Introduction

Artificial Intelligence (AI) has been actively applied and researched in various fields such as speech recognition and image recognition [1], which can be attributed to the wisdom and ingenuity of numerous researchers. Currently, conventional AI requires high power consumption and long computation time using high-performance computers and large datasets. However, anticipating the increasing demand for AI in future, power-efficient AI computing devices will be required considering the strain on communication networks and the environmental impact. In contrast to cloud-based AI, edge AI [2], which utilizes end terminals for performing AI-based information processing, has also attracted attention. Edge AI requires much smaller and less power-consuming computers than those used in cloud AI.

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Stochastic Computing (SC) performs the calculation using the probability of the existence of "1" in the bit stream [3, 4]. This makes it possible to use only one AND gate as a multiplier, which is a compact and power-saving feature. Therefore, research is being conducted on implementation of SC in AI, neural networks, and neural computation [5–9].

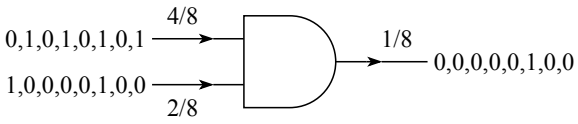


Figure 1: Multiplication in SC

However, using memory in calculations with SC necessitates the use of encoding and decoding circuits, owing to different data representations, which require a much larger circuit area and consume more power than the SC arithmetic circuits.

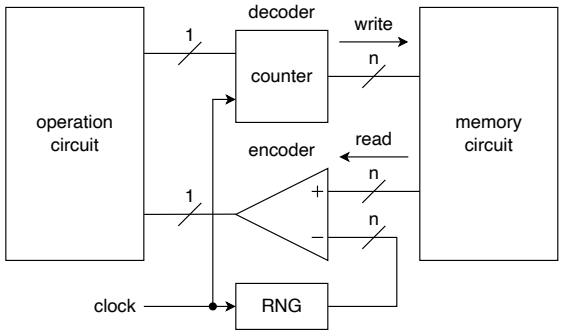


Figure 2: SC memory utilization

In addition, parallel processing is challenging with conventional memory owing to simultaneous access limitations. Therefore, by developing a **Stochastic Memory (SM)** that addresses these issues, a compact and power-efficient SC architecture can be implemented.

2. Stochastic Memory

2.1. The Operating principle

Ensuring proper operation of SM requires the output form to be "0" or "1" and that the probability of outputting "1" must be variable and storable. In this study, our proposed principle satisfies these criteria using a bistable system, noise, and noise offset.

Figure 3 shows the diagram of operating principle of SM. When the output voltage V_{out} of SM is a bistable system with a double-well potential, it is possible to output "0" and "1" as it is stable at two wells. If the initial value of V_{out} is set randomly by the noise voltage V_{noise}, the system outputs a binary value stochastically according to the relationship with the reference point V_m. Therefore, SM can be operated in a manner that yields a random bit stream signal for V_{out} , which serves as a suitable data representation for SC.

(1) Set initial value of V_{out} randomly with V_{noise}.

(2) V_{out} is stable at "0" or "1".

(3) Return to (1).

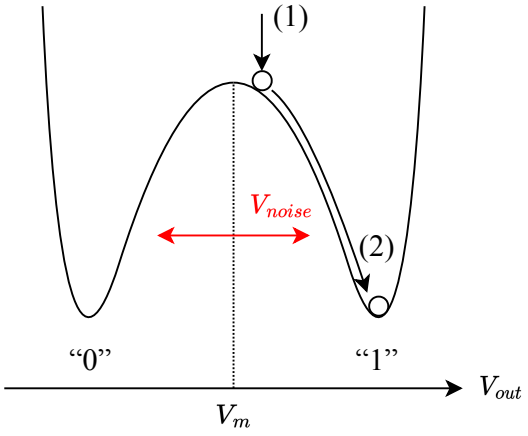


Figure 3: Potential-based SM operating principle

When the offset of V_{noise} is V_m, the range where $V_{noise} > V_m$ and the range where $V_{noise} < V_m$ are equal, the probability p_1 of outputting "1" is 0.5. However, when the offset is $V_m + \Delta V$, the range where $V_{noise} > V_m$ increases, so p_1 increases from 0.5. When the offset is $V_m - \Delta V$, the range where $V_{noise} < V_m$ increases, so p_1 decreases from 0.5. In this manner, varying p_1 is possible by the noise offset. Probability storage can be performed by holding the offset amount, the voltage value, in an analog memory.

2.2. The Proposed circuit

Figure 4 shows the proposed circuit diagram. SM is composed of three main elements.

Table 1: Relation between noise offset and p_1

noise offset	$V_m - \Delta V$		V_m		$V_m + \Delta V$
p_1	0	$\leftarrow$	0.5	$\rightarrow$	1

The bistable circuit in the lower right corner is a circuit where the output voltage V_{out} is a bistable system as shown in Figure 3. Therefore, an inverter latch or an operational amplifier (opamp) [10] can be used, which outputs a binary value in the supply voltage range $[0, V_{DD}]$.

$$V_{out} = \begin{cases} V_{DD} & (\text{"1"}) \\ 0 & (\text{"0"}) \end{cases} \tag{1}$$

The negative feedback opamp in the upper left corner functions as a voltage follower, that outputs the same voltage as its positive terminal. Typically, it is used as an impedance converter, however, a floating gate (FG) MOSFET [10] is used as an analog memory on this positive terminal. This allows the offset of V_{noise} to be varied by the floating gate layer voltage V_{fg}, and the voltage follower output V_{vf} is expressed as follows.

$$V_{vf} = V_{noise} + V_{fg} \tag{2}$$

The analog switch in the upper right corner is a circuit that turns the switch on and off by the control signal V_{con}. If V_{con} is V_{DD}, the switch turns on and connects input V_{vf} and output V_{out}. If V_{con} is 0, the switch turns off and V_{vf} and V_{out} are open. This changes V_{out} by V_{con} using V_{noise}. Thus, random initialization of V_{out} can be performed as explained in the principle of operation.

$$V_{out} = \begin{cases} V_{vf} & \text{if } V_{con} = V_{DD}, \\ V_{DD} \text{ or } 0 & \text{if } V_{con} = 0. \end{cases} \tag{3}$$

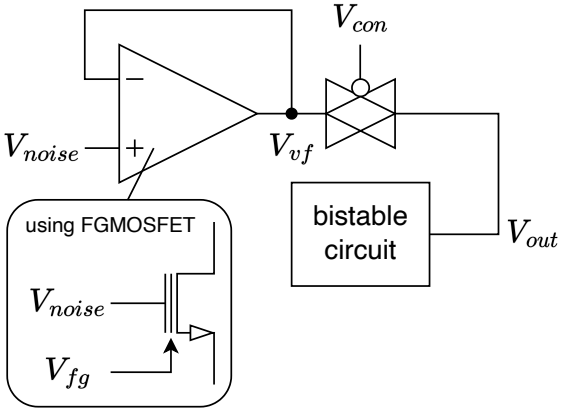


Figure 4: The proposed circuit for SM

3. Evaluations

3.1. Stochastic binary output

Figure 5 shows the simulation circuit with a positive feedback opamp. An opamp (Texas Instruments, LMC6482) and an analog switch (Texas Instruments, CD4066) were supplied with a supply voltage V_{DD} = 5 V. V_{bias} used a DC voltage source of 2.5 V. V_{noise} used a white noise source with RMS amplitude 500 mV and frequency 10 kHz. V_{con} used a square wave with period 1 ms, on-time 0.1 ms. The positive input pin of the front opamp was made floating by C_1 = 10 pF, and the initial value of V_{fg} was set to any value that results in a FGMOSFET. The feedback resistor R of the rear opamp was set to 1 kΩ.

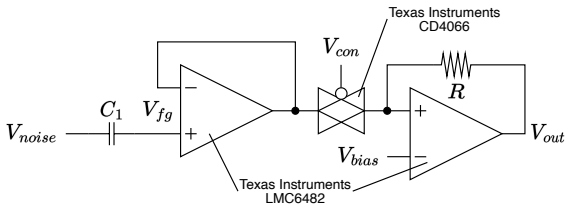
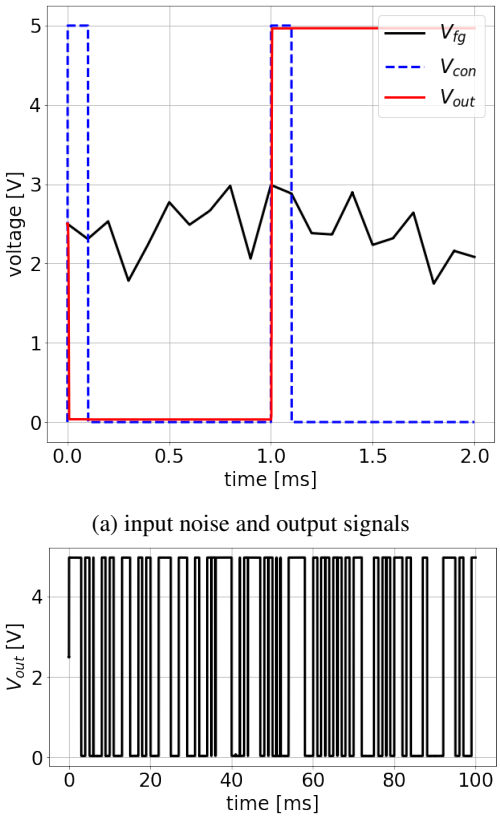


Figure 5: Simulation circuit using a positive feedback opamp

Figure 6a shows the transient analysis results using SPICE when $V_{fg,init}$ (initial value of V_{fg}) is set to 2.5 V. When V_{con} = 5.0 V, the analog switch is turned on and the voltage follower and positive feedback opamp are connected. A random value is then input to the positive feedback opamp by V_{noise}. Subsequently, when V_{con} = 0 V, the connection with the voltage follower is broken and V_{out} stabilizes at 5 V ("1") or 0 V ("0"). This satisfies the operating principle described in the section 2.1.

Figure 6b shows the waveform of V_{out} for a long-time analysis. In this simulation, the time V_{out} switch is the same as the V_{con} period of 1 ms. Consequently, running transient analysis for up to 100 ms, can yield stochastic binary outputs 100 times.. As V_{out} is a random binary sequence, we can confirm that it is the required data representation for SC.



(a) input noise and output signals

(b) stochastic binary output

Figure 6: Simulation results ($V_{fg,init}$ = 2.5 V)

3.2. Stochastic memory characteristics

The memory characteristics of the probability p_1 of V_{out} outputting "1" are evaluated. Calculate p_1 from V_{out} waveform data for 100 ms for each $V_{fg,init}$. Here, in addition to the circuit in Figure 5, a circuit with a CMOS inverter latch in Figure 7 was also simulated. The operation of this circuit is the same as a positive feedback opamp, where the connection between the voltage follower and latch is controlled by a switch, which enables V_{out} to operate as a stochastic binary output.

$$p_1 = \frac{\text{output count of "1"}}{100} \tag{4}$$

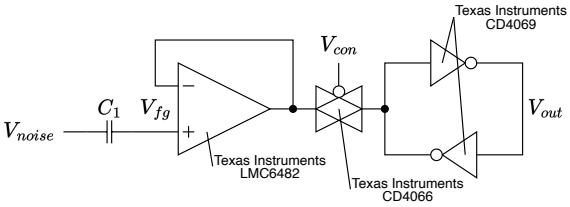


Figure 7: Simulation circuit using an inverter latch

Figure 8 shows the output probability characteristics. Here, $V_{fg,init}$ is varied in $[0, V_{DD}]$ by 0.1 V. In addition, each point is calculated from the equation 4, and the sigmoid function fitted based on those results is shown as a line. In addition, each point is calculated from the equation 4, and fitted with the equation 5, which is represented by a solid line.

$$p_1 = \frac{1}{1 + e^{-(aV_{fg,init}+b)}} \tag{5}$$

When a positive feedback opamp is used in the bistable circuit, p_1 changes along the same direction as the increase or decrease of $V_{fg,init}$. The coefficients in the fitting are $a = 4.3$ and $b = -10.6$. At this time, the range of change in $V_{fg,init}$ is approximately 2 V. As this is the peak-to-peak value range of V_{noise}, it is possible to adjust the width of $V_{fg,init}$ variation based on the noise intensity.

When a latch is used in the bistable circuit, p_1 changes in the opposite direction against the increase or decrease of $V_{fg,init}$. The coefficients in the fitting are $a = -4.5$ and $b = 9.6$. The V_{out} in Figure 7 is an inverter output, therefore, the change characteristic is opposite to that of a positive feedback opamp. The above evaluation confirmed that SM is possible by using the FGMOSFET as analog memory in the proposed circuit.

Assuming that the V_{fg} rewriting circuit with 8-bit precision is used, the minimum change in V_{fg} will be about 20 mV. Therefore, as p_1 is divided by about 100, SM will have a 7-bit precision.

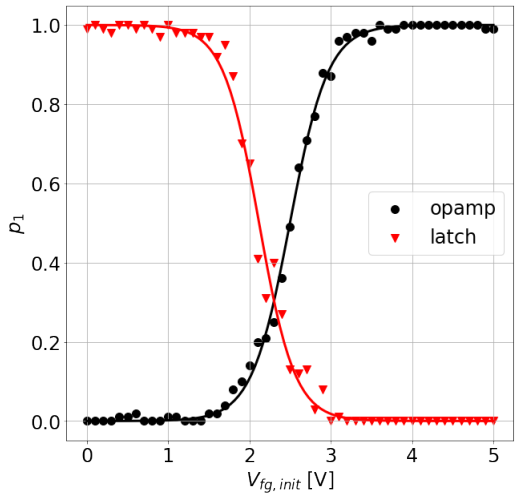


Figure 8: Stochastic memory characteristics in each bistable circuit

4. Conclusion

For efficient memory utilization of SC, we proposed a SM that outputs a random bit stream while storing the output probability. First, based on a double-well potential, a stochastic binary output was represented by noise initialization. Next, the output probability was varied by a noise offset, and the SM was represented by holding the offset value in an analog memory. Finally, the circuit based on these operating principles was evaluated using SPICE. The results showed that a simple analog circuit can be used to implement SM with an adequate range of variation, although dependent on the input noise intensity.

Acknowledgments

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