A Majority-Logic Device Using a Single-Electron Box

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Purpose

One of the challenges for nanoelectronics is the development of integrated circuits on the basis of single-electron circuit technology. For this purpose, we propose a majority-logic device that consists of a single-electron box. The device has a simple structure and is therefore suitable for constructing integrated circuits.

Unit function of majority logic

Majority logic is a way of implementing digital operations based on the principle of *majority decision*. The logic element, a majority gate, has an odd number of binary inputs and a binary output; the gate symbol and logic operation for a three-input majority gate are shown in Fig. 1. The output is a logical 1 when the majority of the inputs is logical 1 and a logical 0 when the majority of inputs is logical 0. Any digital function can be implemented by a combination of majority gates and binary inverters. Majority logic provides a concise implementation of most digital functions encountered in logic-design applications.

Single-electron box using a double tunneling junctions

The main component of the majority-gate device we are proposing is a single-electron box that uses a double tunneling junction (a multiple tunneling junction can also be used). At the low temperatures at which the Coulomb-blockade effect is established, the double-junction box shows bistable operation as illustrated in Fig. 2. It stores excess electrons on node 1 (Fig. 2(a)) and changes the number n of the electrons as a function of bias voltage Vd. Electron number n is a hysteretic staircase function shown in Fig. 2(b); it changes from 0 to 1 when Vd is increased above a threshold $V2$, and returns from 1 to 0 when Vd is decreased below a threshold $V1$. Owing to the discrete changes of n, the voltage at node 1 is a hysteretic sawtooth function of Vd, as shown in Fig. 3.

Constructing a majority-gate device

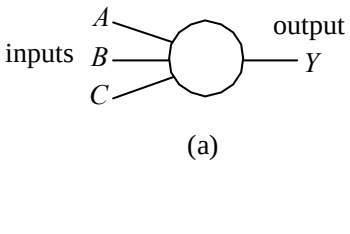
We used the double-junction box to construct a majority-gate device shown in Fig. 4. The majority gate consists of a double-junction box (CL and Cj), three input capacitors $C1$, and an output capacitor $C2$. Three input voltages, $V1$, $V2$, and $V3$, are applied to node 1 through the input capacitors. The double-junction box produces the corresponding logic output on node 1 as illustrated later, and the output is retrieved through the output terminal. In operating the majority gate, we use a positive voltage and a negative voltage of equal amplitude to represent the binary logic values, 1 and 0.

The majority gate works in the following way. We start by grounding the output terminal and then increase bias voltage Vd. At low values of Vd, no excess electron exists on node 1, so the voltage at the node is positive and increases with increasing Vd. When Vd is increased further, an electron tunnels from the ground to node 1 and, consequently, the voltage at the node turns negative. The value of Vd at which electron tunneling occurs depends on the mean of the three input voltages, as shown in Fig. 5. In operating the gate, we increase Vd to such a value ($V0$ in the figure) that electron tunneling occurs if two or three input voltages are positive or logical 1. Thus, the gate produces the majority-logic output on node 1. Strictly speaking, the gate produces the *complement output* of majority logic; that is, the output voltage is negative (logical 0) if two or three input voltages are positive (logical 1).

Simulating the operation of the majority gate

We confirmed the operation of the gate for all input combinations by computer simulation. Figure 6 shows some of the results simulated with this set of parameters: CL = 2 aF, Cj = 20 aF, $C1$ = $C2$ = 2 aF, tunneling-junction conductance = 1 μS, and zero temperature. Bias voltage Vd is a two-step clock pulse shown in the upper plot of Fig. 6. Three inputs, $V1$, $V2$, and $V3$, are applied synchronously with this bias clock, Vd. They are rectangular pulses, positive for logical 1 and negative for 0 (the middle plot of in Fig. 6). In the figure, four sets of inputs, (0, 0, 0), (0, 0, 1), (0, 1, 1), and (1, 1, 1), are sequentially entered, and the outputs, 0, 0, 1, and 1, are produced in response (the bottom plot of Fig. 6). With a 0 output, the output voltage initially goes high for a short time with the rise of bias voltage Vd, and then turns negative as electron tunneling takes place. The output established in each clock cycle is maintained after the input pulses have been turned off, until the bias voltage has fallen below a threshold for holding the output.

Various logic functions can be implemented by combining identical gates into a cascade, with the output capacitor of one gate acting as the input capacitor of the succeeding gate. The majority gate we propose is bilateral, so we control the direction of signal flow by gating it with a three-phase clock (this is analogous to Esaki-diode pair circuit and the quantum-flux-parametron circuit). We designed several subsystems by using the majority gates and confirmed their operation by computer simulation.



inputs			output
A	*B*	*C*	*Y*
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

(b)

Fig. 1 A three-input majority gate: (a) symbol and (b) logic operation.

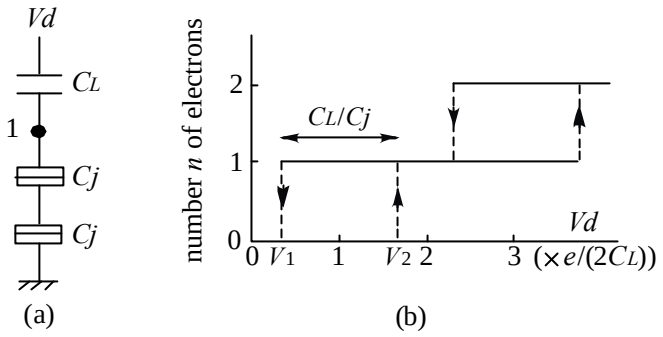


Fig. 2 The single-electron box using a double tunneling junction: (a) circuit configuration and (b) the static number *n* of extra electrons on node 1.

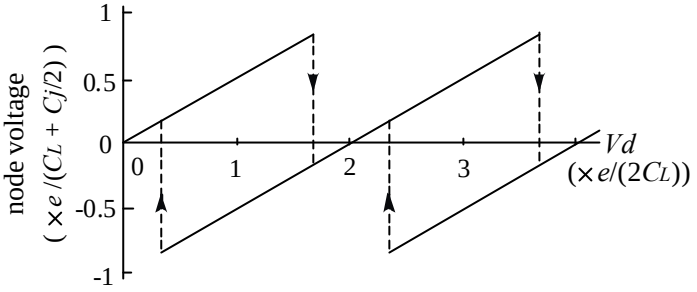


Fig. 3 The voltage at node 1 of the double-junction box as a function of *Vd*.

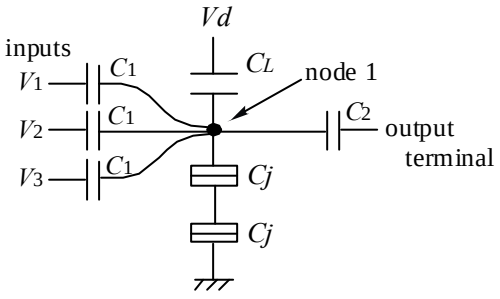


Fig. 4 A majority gate device.

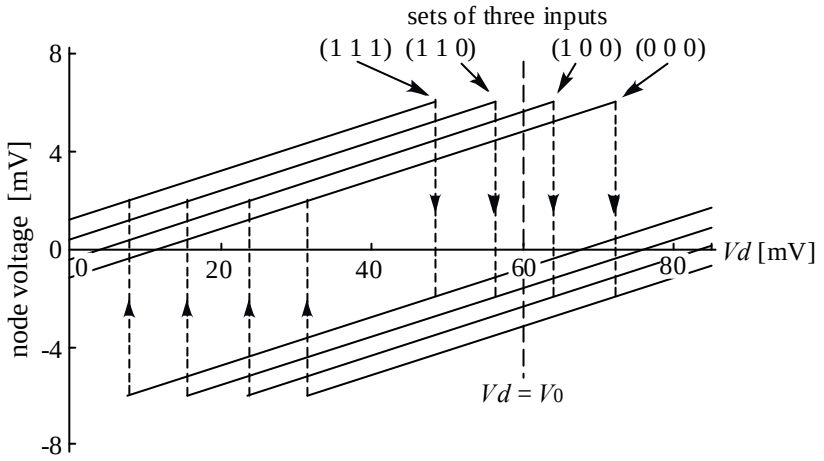


Fig. 5 The voltage at node 1 of the majority gate device as a function of *Vd*, for four sets of inputs (simulated). Inputs '1' and '0' mean input voltages of 4.0 mV and −4.0 mV.

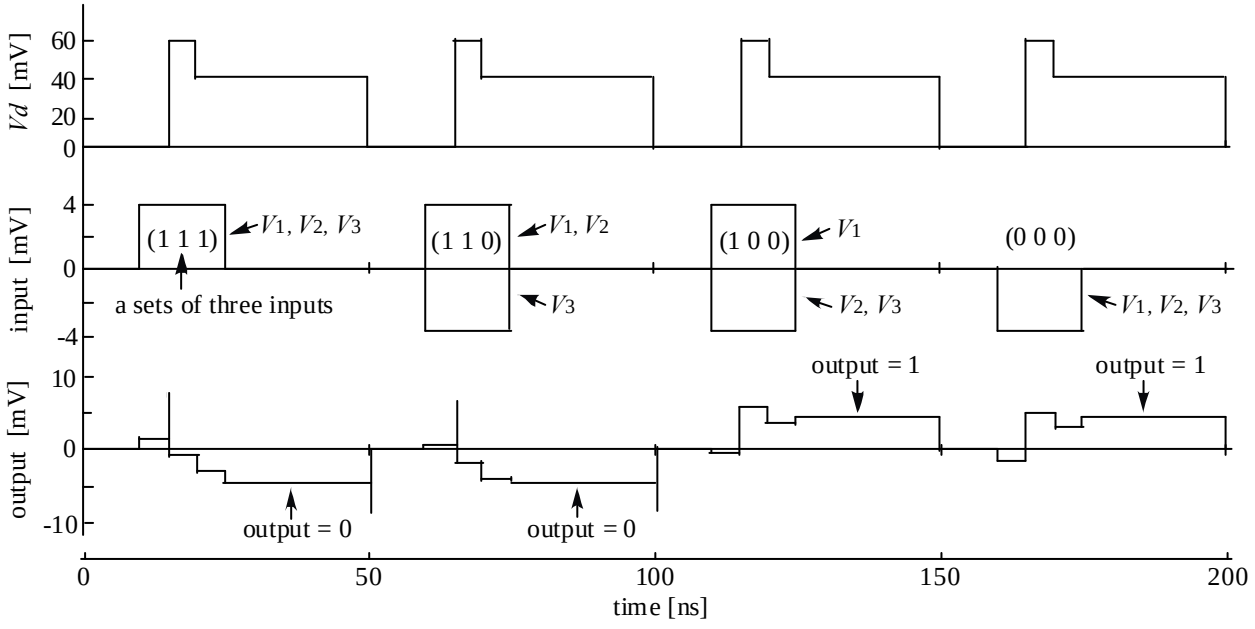


Fig. 6 Majority-logic operation (simulated). The output is the complement of majority logic.