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Current Reference Circuit for Subthreshold CMOS LSIs

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I. INTRODUCTION

Intelligent network systems for the future will require a great number of smart sensor LSIs that measure various physical data in surroundings. These LSIs have to operate with a low power, tens of microwatts or less, because they will probably be placed in non-ideal environments where energy for operation cannot be obtained sufficiently. To achieve such ultra-low power operation, CMOS circuits in sensor LSIs have to be operated in the subthreshold region of MOSFETs. For this purpose, we need to develop a circuit that provides a small reference current of less than tens of nanoamperes for the subthreshold CMOS circuits. We propose such a reference current circuit that is insensitive to temperature and power supply voltage.

Current references for subthreshold CMOS circuits have been proposed by Oguey and Aebischer [1], and Hirose and others [2, 3]. The former current reference, however, shows a positive temperature coefficient of output current. The latter shows a zero temperature coefficient but consists of a complex circuit with many MOSFETs. Therefore, they are unsuitable for our purpose. The current reference circuit we propose will solve these problems and can be used for low-power subthreshold MOS LSIs. The following describes the details of our current reference circuit.

II. CIRCUIT CONFIGURATION

A. Operation Principle

Figure 1 shows the current reference circuit we propose. The circuit consists of a bias-voltage subcircuit and a current-source subcircuit. Bias voltage V_B for MOS resistor M_3 is generated by a diode-connected transistor M_4. The current-source subcircuit accepts bias voltage V_B and generates reference current I_{OUT}. All MOSFETs are operated in the subthreshold region except for transistors M_3 and M_4.

The current I_D in a subthreshold-operated MOSFET can be given by

$$I_D = KI_0 \exp\left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right), \tag{1}$$

where K is the aspect ratio (=W/L) of the MOSFET, I_0 (=$\mu C_{OX} (\eta - 1) V_T^2$) is a process-dependent parameter, μ is the mobility, C_{OX} is the gate-oxide capacitance, η is the subthreshold slope factor, V_{TH} is the threshold voltage, V_T (=$k_B T/q$) is the thermal voltage, k_B is the Boltzmann constant, T is the absolute temperature, and q is the elementary charge [4].

Current I_{BIAS} flowing in each path of the bias-voltage subcircuit is determined by the ratio of the aspect ratios of M_1 and M_2 and the resistance of MOS resistor M_3. The current is given by

$$I_{BIAS} = K_3 \mu C_{OX} (V_B - V_{TH}) \eta V_T \ln(K_2/K_1) . \tag{2}$$

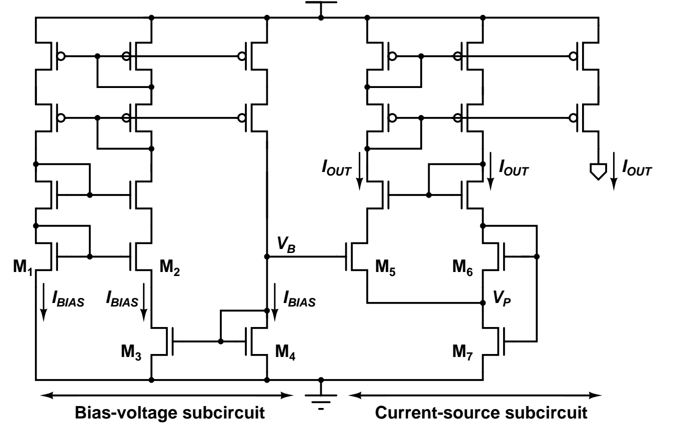

Fig. 1. Schematic of the proposed current reference circuit.

The diode-connected transistor M_4 is operated in the strong inversion and saturation region. Its drain current I_{BIAS} is given by

$$I_{BIAS} = \frac{K_4 \mu C_{OX}}{2} (V_B - V_{TH})^2 . \tag{3}$$

Because the currents in transistors M_3 and M_4 are the same, Eqs. (2) and (3) show that V_B is

$$V_B = V_{TH} + \frac{2K_3}{K_4} \eta V_T \ln\left(\frac{K_2}{K_1}\right) . \tag{4}$$

Output current I_{OUT} through transistor M_5 operating in the subthreshold region can be given by

$$I_{OUT} = K_5 I_0 \exp\left(\frac{V_B - V_P - V_{TH5}}{\eta V_T}\right) . \tag{5}$$

The source voltage V_P of transistor M_5 can be given by

$$V_P = V_{GS7} - V_{GS6} = \eta V_T \ln\left(\frac{2K_6}{K_7}\right) - \Delta V_{TH76} , \tag{6}$$

where ΔV_{TH76} is the difference between the threshold voltages of M_6 and M_7 (including the body effect in the transistors). From Eqs. (4), (5), and (6), we find that

$$I_{OUT} = K_5 I_0 \exp\left(\frac{\Delta V_{TH}}{\eta V_T}\right) \cdot \frac{K_7}{2K_6} \left(\frac{K_2}{K_1}\right)^{2K_3/K_4} , \tag{7}$$

where ΔV_{TH} (=$\Delta V_{TH76} - \Delta V_{TH54}$) is the difference between the threshold voltages of transistors M_4-M_7. This way, we can obtain a small reference current of nanoamperes.

B. Temperature Dependence

The temperature dependence of the mobility μ can be given by $\mu(T) = \mu(T_0)(T/T_0)^{-m}$, where $\mu(T_0)$ is the carrier

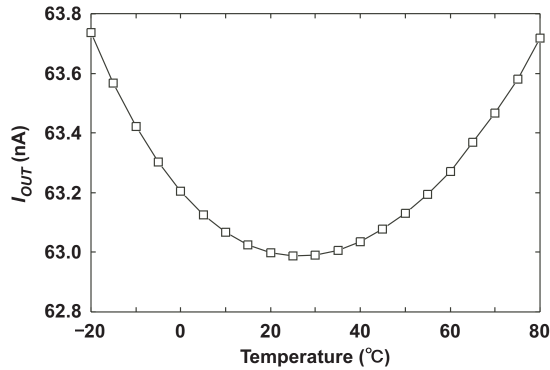

Fig. 2. Output current I_{OUT} simulated as a function of temperature.

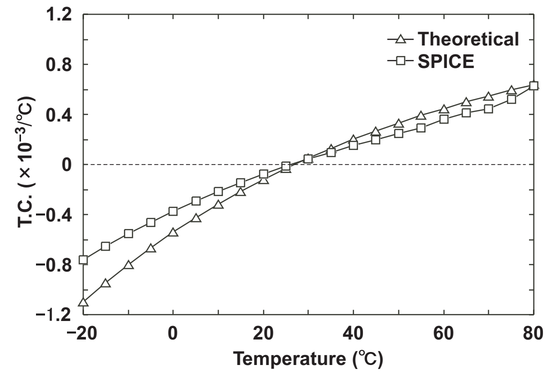

Fig. 3. TC of output current I_{OUT} as a function of temperature; theoretical value obtained from Eq. (11) and SPICE simulated value.

mobility at room temperature T_0, and m is the mobility temperature exponent. The temperature coefficient (TC) of reference current I_{OUT} in Eq. (7) is given by

$$TC = \frac{1}{I_{OUT}} \frac{dI_{OUT}}{dT} = \frac{2 - m - \frac{\Delta V_{TH}}{\eta V_T}}{T} \quad . \tag{8}$$

Therefore, the condition for a zero temperature coefficient can be given by

$$2 - m - \frac{\Delta V_{TH}}{\eta V_T} = 0. \tag{9}$$

Setting ΔV_{TH} to an appropriate value can provide a zero TC at room temperature. The value of V_{TH} can be adjusted by a bias voltage V_B. A sample circuit we designed showed a zero TC at $\Delta V_{TH} = 47$ mV.

III. RESULTS

We confirmed the operation of our reference circuit with the aid of SPICE simulation. We used the SPECTRE level 53 model with a parameter set for the 0.35-μm 2P4M standard CMOS process. The power supply voltage was set to 3 V.

Figure 2 shows output current I_{OUT} of the circuit as a function of temperature. The output current was about 63 nA and almost constant at temperatures –20 to 80 °C. The temperature dependence and temperature coefficient were 7 pA/°C and 115 ppm/°C. Figure 3 shows a TC calculated from Eq. (8) and a TC simulated with SPICE, plotted as a function of temperature. The results obtained with Eq. (8) and SPICE simulation results correspond with each other.

To verify the stability of the circuit operation in device variation, we performed a corner analysis, using parameters provided by the manufacturer. The worst corners of nMOS and pMOS transistors (S: slow, T: typical, and F: fast) were taken into consideration. Figure 4 shows output current I_{OUT} for five different process corner conditions. The value of I_{OUT} changed with process corners. This is so because the difference in threshold voltages ΔV_{TH} depends on the process corners of nMOS devices. However, the reference current I_{OUT} has little temperature dependence in each process corner condition.

Table I summarizes the performance of our reference circuits. The simulations showed the maximum power consumption of 1.9 μW at 80 °C. The line sensitivity was

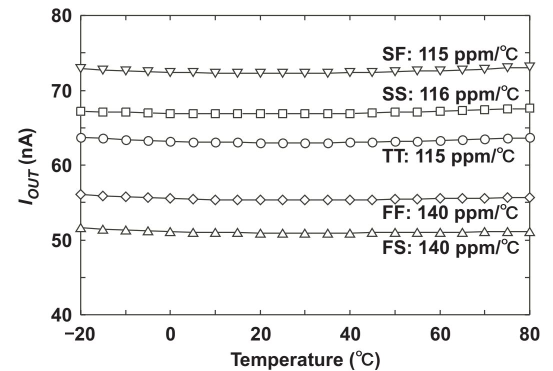

Fig. 4. Output current I_{OUT} simulated with corner analysis. Process corners of nMOS and pMOS transistors were taken into consideration.

TABLE I. Performance summary

Process	0.35-μm, 2-poly, 4-metal CMOS
Temperature range	–20 – 80 °C
V_{DD}	2 – 3 V
I_{OUT}	63.3 nA (Typical)
Power	1.9 μW (V_{DD}=3 V, T=80 °C)
TC	115 ppm/°C
Line sensitivity	0.08 %/V (V_{DD}=2 – 3 V)

0.08 %/V in a V_{DD} range of 2 – 3 V. The lower limit of supply voltage can be reduced less than 2 V by using an operational amplifier instead of the cascode current mirrors we used in this example. Our circuit is useful as a reference current circuit for micro-power LSIs.

REFERENCES

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