Low-voltage Power Supply Regulator for Subthreshold-operated CMOS Digital LSIs

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Abstract

A power supply regulator for subthreshold-operated logic LSIs was developed using a 0.35-μm standard CMOS process technology. The regulator accepted a battery voltage (1–3.3 V) and produced a minimum supply voltage (in a range of 0.5–1.2 V) for operating subthreshold logic circuits at a speed determined by a CR reference, regardless of variations in temperature and MOSFET parameters. Experimental results showed stable operation with a frequency line regulation of 5.8 %/V, a frequency load regulation of 74 ppm/μA, and a quiescent current of 0.6 μA at 1.55-V battery voltage. Our regulator can be used as a voltage supply for subthreshold-operated digital LSIs.

Keywords: Power supply regulator, Subthreshold logic, Power-aware LSIs, Ultra-low power, Process compensation

Introduction

One promising area of research in microelectronics is the development of ultra-low power digital LSIs consisting of subthreshold-operated CMOS circuits. As an indispensable component for such LSIs, we propose a voltage regulator that converts a battery voltage to a well-controlled low supply voltage for subthreshold CMOS logic circuits. Subthreshold LSIs have attracted growing attention in recent years [1] because they are the most suitable device for energy-constrained applications such as micro-sensor network nodes [2], radio-frequency identification tags, and implantable medical devices. To construct practical subthreshold LSIs, we must take two requirements into consideration. First, such LSIs have to be operated with low energy consumption to obtain long battery lifetimes. Therefore, a supply voltage for them should be as low as possible. Second, the LSIs have to operate at a speed needed for their applications. This means that a supply voltage cannot be lowered without restriction but should be set to a value enough to attain the required speed capability.

Several low-power supply regulators for subthreshold logic LSIs have been proposed [3, 4]. The circuits can provide regulated voltages lower than threshold voltages and have low-power configurations. However, these circuits cannot satisfy the second requirement. To meet this dual requirement, we propose a low power voltage regulator to provide a supply voltage to subthreshold CMOS logic circuits. The regulator accepts a battery voltage and produces a minimum supply voltage for operating the logic circuits at a speed determined by a reference CR circuit, regardless of variations in temperature and MOSFET parameters.

Power supply regulator for monitoring the delay

Figure 1 shows a circuit configuration of our voltage regulator, together with load digital LSIs. The regulator accepts a battery voltage (V_{EX}) and produces a lowered voltage (V_{DD}), a supply voltage for the LSIs, through a MOSFET variable resistor (M_R). To monitor the gate delay of the LSIs, the regulator has a ring oscillator consisting of the same gates as LSIs' and operates the ring oscillator with supply voltage V_{DD}. A frequency comparator accepts the oscillation frequency (f_{RO}) of the ring oscillator to produce a switched-capacitor resistance $1/(f_{RO}C_S)$ and compares it to a reference resistor R_{REF} in the comparator. That is, the comparator compares f_{RO} to the time constant of the capacitor-resistor ($C_S R_{REF}$) reference. The comparator detects the difference between $1/f_{RO}$ and time constant $C_S R_{REF}$ and adjusts the gate voltage (V_{CTR}) for MOSFET resistor M_R. (A pMOSFET is used as M_R because it can operate even if battery voltage V_{EX} decreases to 0.8-0.9 V.) If $1/f_{RO} < C_S R_{REF}$, the comparator increases gate voltage V_{CTR}. This lowers supply voltage V_{DD} to decrease oscillation frequency f_{RO} of the ring oscillator. If $1/f_{RO} > C_S R_{REF}$, the comparator decreases V_{CTR} to increase V_{DD}, thereby increasing f_{RO}. Through this feedback operation, supply voltage V_{DD} is adjusted to a value that operates the ring oscillator at a frequency equal to $1/(C_S R_{REF})$. In other words, the supply voltage is set to a value such that the loop delay of the ring oscillator will be equal to $C_S R_{REF}$. This way, the regulator can provide an appropriate supply voltage such that the gate delay in the digital LSIs is set equal to $C_S R_{REF}/(2n)$, where n is the number of inverters that compose the ring oscillator. This can be attained regardless of variations in temperature and MOSFET parameters.

Results

We confirmed the operation of the circuit using a SPICE simulation with a set of 0.35-μm standard CMOS parameters with threshold voltage of 0.5 V for nMOSFET and 0.7 V for pMOSFET. Battery voltage V_{EX} was set to 1.55 V (the nominal voltage of silver oxide batteries). To verify the stability of the circuit operation under process variations, we performed Monte Carlo analysis assuming both die-to-die variations (uniform distribution: -0.1 V < ΔV_{TH} < 0.1 V) and within die variations (Gaussian distribution: σV_{TH}) for all MOSFETs in the circuit. Figure 2 shows a scatter plot and the distribution of the propagation delay of a 100-stage subthreshold operated NAND inverter chain supplied by our regulator. The result for a fixed supply voltage, instead of the regulated supply voltage, is plotted for comparison. The delay for the fixed supply voltage changes broadly with process variation, while the delay with our regulator shows little dependence on the die-to-die threshold voltage variation. This is so because regulated voltage V_{DD} of our circuit changes with the variation of threshold voltage so that the gate delay in the inverter chain will be equal to $C_S R_{REF}/(2n)$.

Figure 3 shows the micrograph of our prototype. The active area of the regulator occupies 0.06 mm^2. Figure 4 (A) shows measured supply voltage V_{DD} and ring oscillator frequency f_{RO} as a function of reference resistance R_{REF}. Changing the value of R_{REF} from 0.1 to 100 MΩ was able to control the frequency in a wide range of 0.02–20 MHz (corresponding to a supply voltage change from 0.5 V to 1.2 V). These results were consistent with $f_{RO} = (R_{REF} C_S)^{-1}$. Figures 4(B) and 4(C) show measured oscillation frequency f_{RO} and supply voltage V_{DD} as a function of battery voltage V_{EX} and load current I_{LOAD}. The line regulations for f_{RO} and V_{DD} were 4.5 %/V and 0.7%/V. The load regulation of f_{RO} and V_{DD} were 74 ppm/μA and 70 ppm/μA. These results were sufficiently small for practical use. Table I summarizes the performance of our regulator. The temperature coefficient of f_{RO} was 70 ppm/°C. The power dissipation of our regulator was 1 μW, with a 1.55-V battery voltage and a 10-MΩ reference resistor.

This way, we developed a low-voltage power supply regulator for subthreshold-operated CMOS digital LSIs. Our regulator can be implemented with digital LSIs on a chip and is useful to construct power-aware digital LSI systems.

References

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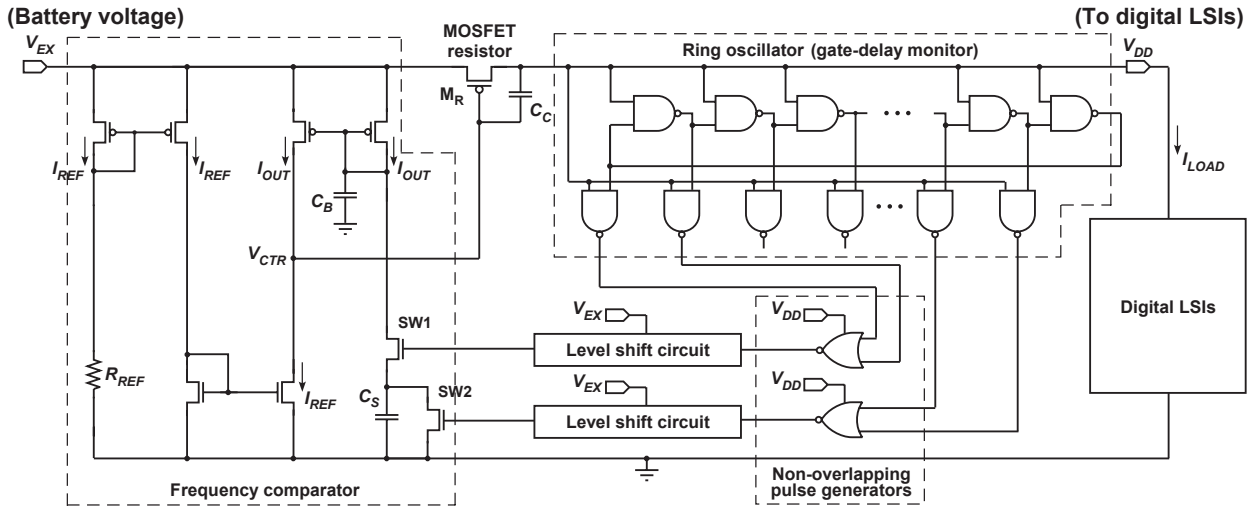

Fig. 1. Circuit configuration of power supply regulator consisting of frequency comparator, ring oscillator, and MOSFET resistor.

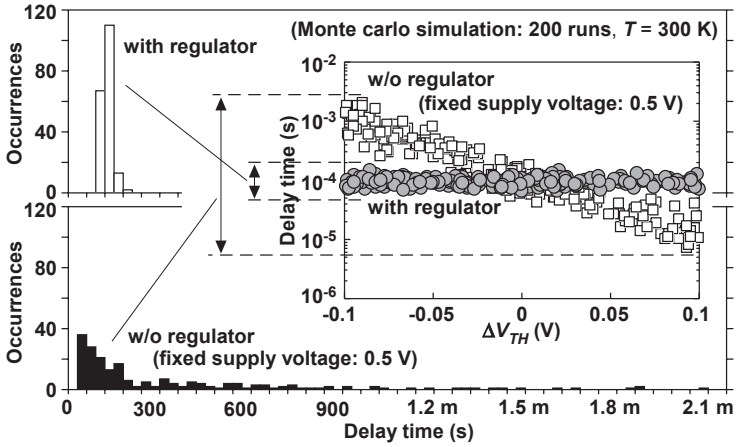

Fig. 2. Simulated delay variation of 100-stage subthreshold operated inverter chain.

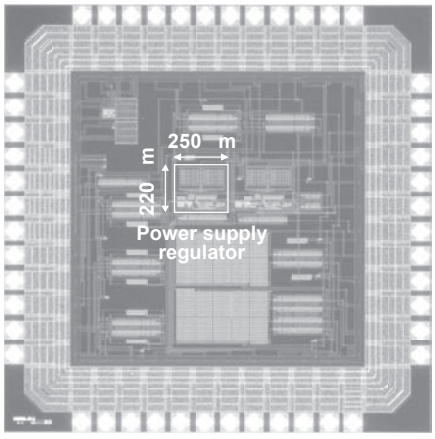

Fig. 3. Chip micrograph. The circuit occupies 0.06 mm^2.

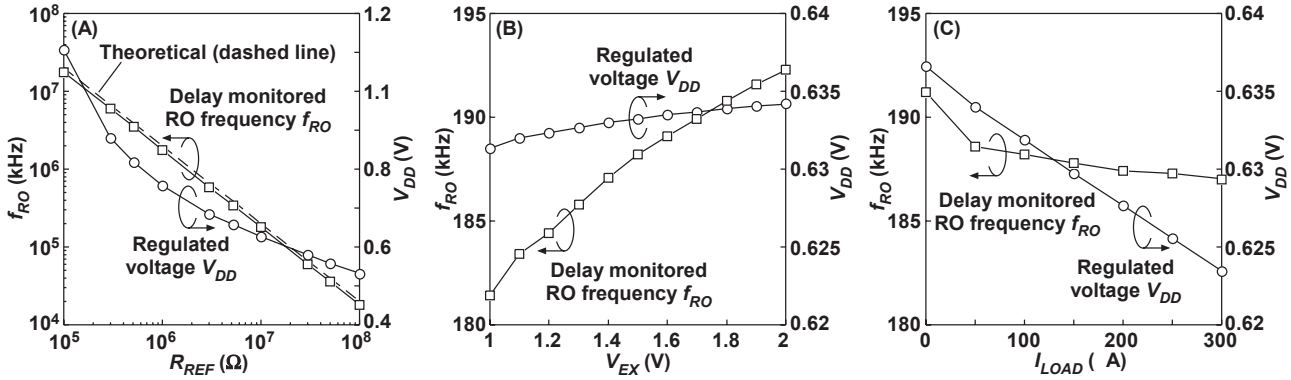

Fig. 4. Experimental results of f_{RO} and V_{DD}. (A) f_{RO} and V_{DD} as a function of R_{REF}, (B) Line regulation, (C) Load regulation.

Table 1. Performance summary of our supply regulator.

Process	0.35 m, standard CMOS	Frequency line reg.	5.8%/V (@ V_{EX} = 1 - 2 V)
Temp. range	-20 - 80 degC	Voltage line reg.	0.4%/V (@ V_{EX} = 1 - 2 V)
V_{EX}	1 - 3.3 V	Frequency load reg.	74 ppm/ A (@ I_{LOAD} = 0 - 300 A)
V_{DD}	0.5 - 1.2 V	Voltage load reg.	70 ppm/ A (@ I_{LOAD} = 0 - 300 A)
f_{RO}	0.02 - 20 MHz	Delay variation (σ/) of load circuits	11% (Monte Carlo simulation)
Quiescent current	0.34 - 1.8 A (@ V_{EX} = 1 - 2 V, R_{REF} = 10 MΩ)		
Power	0.34 - 3.6 W (@ V_{EX} = 1 - 2 V, R_{REF} = 10 MΩ)	*T.C.* of f_{RO}	70 ppm/degC (T = -20 - 80 degC)