TEMPERATURE-TO-FREQUENCY CONVERTER CONSISTING OF SUBTHRESHOLD MOSFET CIRCUITS FOR SMART TEMPERATURE-SENSOR LSIS

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ABSTRACT

An ultra-low-power temperature sensor circuit has been developed using a 0.35-μm standard CMOS process. The circuit consists of a proportional-to-absolute-temperature (PTAT) current generator and a frequency-locked loop, and generates a PTAT clock frequency. The PTAT current generator is the key component of the sensor and was constructed by using the characteristics of a MOSFET in the subthreshold region. Theoretical analyses and experimental results showed that the circuit can be used as a temperature sensor with ultra-low-power consumption of 10 μW or less. The accuracy of the sensor output was within ±1.8°C in a temperature range from 10°C to 80°C. Our sensor would be suitable for use in subthreshold-operated, power-aware LSIs.

KEYWORDS

CMOS, Temperature sensor, PTAT, Frequency-locked loop, Subthreshold current, Weak inversion, Ultra-low power, Power-aware LSI

INTRODUCTION

Intelligent network systems with various smart-sensor devices are expected to be developed in the near future and to spread all over the world to enable infrastructures to be constructed for the information age. Such network systems require a huge number of sensor devices that measure various physical data in our surroundings, store and process the measured data, and output the data on demand. As these sensors must operate for long periods, the available energy resources—whether micro-batteries, energy harvesting devices, or both—limit their overall operation. One possible method of reducing the energy consumption of such sensors is to fabricate the sensors with CMOS circuits that operate in the subthreshold region of MOSFETs [1].

This paper focuses on ultra-low-power temperature sensors and, to produce such sensors, we propose a subthreshold CMOS circuit that produces a proportional-to-absolute-temperature (PTAT) clock frequency. The PTAT characteristics can be used as a temperature sensor. Many temperature sensors consisting of CMOS circuits have been reported [2-4], but they are unsuitable for use in intelligent network systems because of their large power consumption of several hundred microwatts. The sensor circuit we propose will solve this problem and can be used for ultra-low-power temperature sensor applications. Our sensor consists of subthreshold CMOS circuits and can operate with an ultra-low power of ten microwatts or less. It generates clock output with a frequency proportional to the absolute temperature. The following describes the details of our PTAT clock generator.

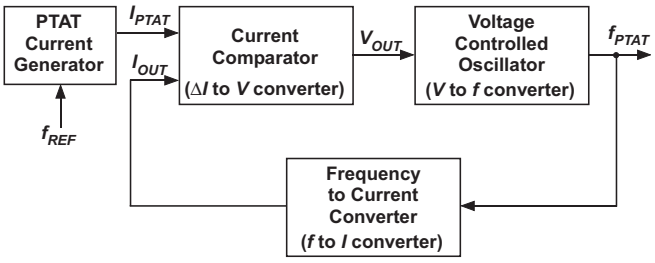

Fig. 1: Block diagram of proposed PTAT clock generator.

CIRCUIT CONFIGURATION

Figure 1 shows a block diagram of our temperature sensor, which generates a PTAT clock frequency using a frequency-locked loop technique. It consists of a PTAT current generator, a current comparator, a voltage-controlled oscillator (VCO), and a frequency-to-current converter. The current comparator, VCO, and frequency-to-current converter form a feedback loop. The current comparator detects the difference between the output current I_{PTAT} of the PTAT current generator and the output current I_{OUT} of the frequency-to-current converter, and generates output voltage V_{OUT} proportional to the difference. The VCO accepts V_{OUT} and produces oscillation pulses with frequency f_{PTAT} as a function of V_{OUT}. The frequency-to-current converter accepts the oscillation pulses and generates I_{OUT} that is proportional to f_{PTAT}. Then, the current comparator again compares I_{OUT} with I_{PTAT} to produce readjusted V_{OUT}. This feedback operation is repeated to make I_{OUT} equal to I_{PTAT}. The resulting clock frequency f_{PTAT} is proportional to the absolute temperature.

Figures 2 and 3 show the circuit configuration of our temperature sensor. All MOSFETs in the circuit are operated in the subthreshold region to achieve ultra-low-power consumption. The following sections describe the operation of the sensor circuit in detail.

1. PTAT Current Generator

Figure 2 shows a PTAT current generator. The circuit is based on a β–multiplier self-biasing circuit and uses a

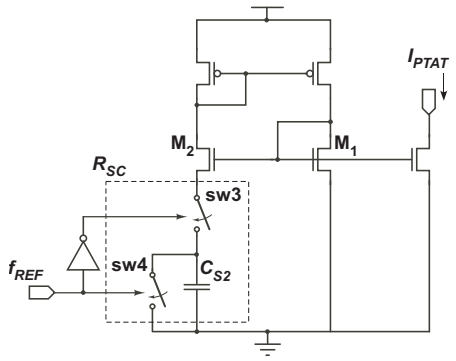

Fig. 2: PTAT current generator consisting of subthreshold MOSFETs and switched capacitor resistor.

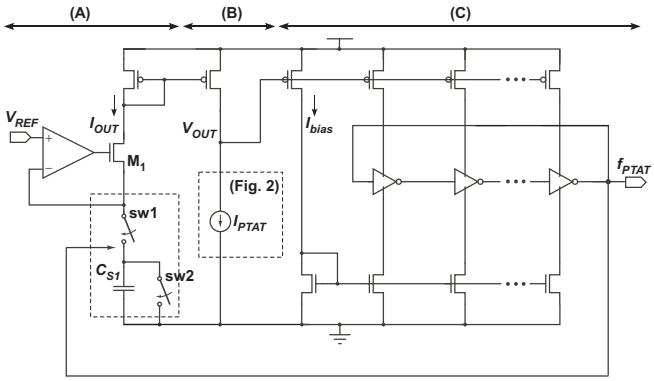

Fig. 3: Simplified schematic of proposed PTAT clock generator.

switched capacitor circuit instead of an ordinary passive resistor [5]. The switched capacitor circuit consisting of a capacitor C_{S2} and two switches (sw3, sw4) can establish an average resistance R_{SC} equal to $(C_{S2} \cdot f_{REF})^{-1}$ between the source of transistor M_2 and ground. The circuit works as follows.

The subthreshold MOSFET current I_{DS} for a drain-source voltage higher than 0.1 V is given by

$$I_{DS} = KI_0 \exp\left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right), \tag{1}$$

where K is the aspect ratio (=W/L) of the transistor, μ is the carrier mobility, C_{OX} is the gate-oxide capacitance, $V_T(=k_BT/q)$ is the thermal voltage, k_B is the Boltzmann constant, T is the absolute temperature, and q is the elementary charge, V_{TH} is the threshold voltage of a MOSFET, and η is the subthreshold slope factor [6], [7].

In the circuit in Fig. 2, gate-source voltage V_{GS1} in M_1 is equal to the sum of gate-source voltage V_{GS2} in M_2 and the voltage drop ($I_{PTAT} \cdot R_{SC}$) of the switched-capacitor resistor, i.e.,

$$V_{GS1} = V_{GS2} + I_{PTAT}R_{SC}. \tag{2}$$

Because currents I_{PTAT} in M_1 and in M_2 are equal, Eq. (2) can be rewritten as

$$I_{PTAT}R_{SC} = \eta V_T \ln(K_2/K_1). \tag{3}$$

From Eqs. (2) and (3), the current I_{PTAT} though M_1 and M_2 is given by

$$I_{PTAT} = \frac{\eta V_T \ln(K_2/K_1)}{R_{SC}} = f_{REF} \cdot C_{S2} \cdot \frac{\eta k_B T}{q} \ln\left(\frac{K_2}{K_1}\right). \tag{4}$$

Because f_{REF} is independent of temperature, output current I_{PTAT} is a PTAT characteristics.

Therefore, we can obtain a PTAT current with an ultra-low level of current.

2. Current Comparator (block (B) in Fig. 3)

The current comparator is a common-source circuit used to detect the difference between the PTAT current I_{PTAT} of the PTAT current generator and the output current I_{OUT} of the frequency-to-current converter. It generates output voltage V_{OUT} proportional to the difference between the two currents.

3. Voltage Controlled Oscillator (block (C) in Fig. 3)

The VCO consists of a current-starved ring oscillator as shown in Fig. 3. The circuit is used for producing oscillation pulses that are dependent on the output voltage V_{OUT} of the current comparator. Oscillation frequency f_{RTAT} depends on applied current I_{bias} and is given by

$$f_{PTAT} = \frac{I_{bias}}{2mAC_LV_{DD}} = \frac{I_0}{2mAC_LV_{DD}} \exp\left(\frac{V_{DD} - V_{OUT} - V_{TH}}{\eta V_T}\right), \tag{5}$$

where m is the number of inverters in the oscillator, C_L is the load capacitance for each inverter, A is a delay fitting parameter [8]. Oscillation frequency f_{PTAT} depends on V_{OUT}.

4. Frequency to Current converter (block (A) in Fig. 3)

The frequency-to-current converter is a voltage-to-current converter combined with a switched-capacitor resistor. The circuit is used to produce output current I_{OUT} proportional to the oscillation frequency f_{PTAT} of the VCO. The voltage of one end of the switched-capacitor resistor is fixed to reference voltage V_{REF} with an operational amplifier and a MOSFET, where the reference voltage is supplied by a voltage reference circuit. The switched-capacitor resistor consists of capacitor C_{S1} and two switches (sw1, sw2) driven with the oscillation pulses from the VCO, and operates as a resistor with a resistance of $(C_{S1} \cdot f_{PTAT})^{-1}$. Therefore, the output current I_{OUT}

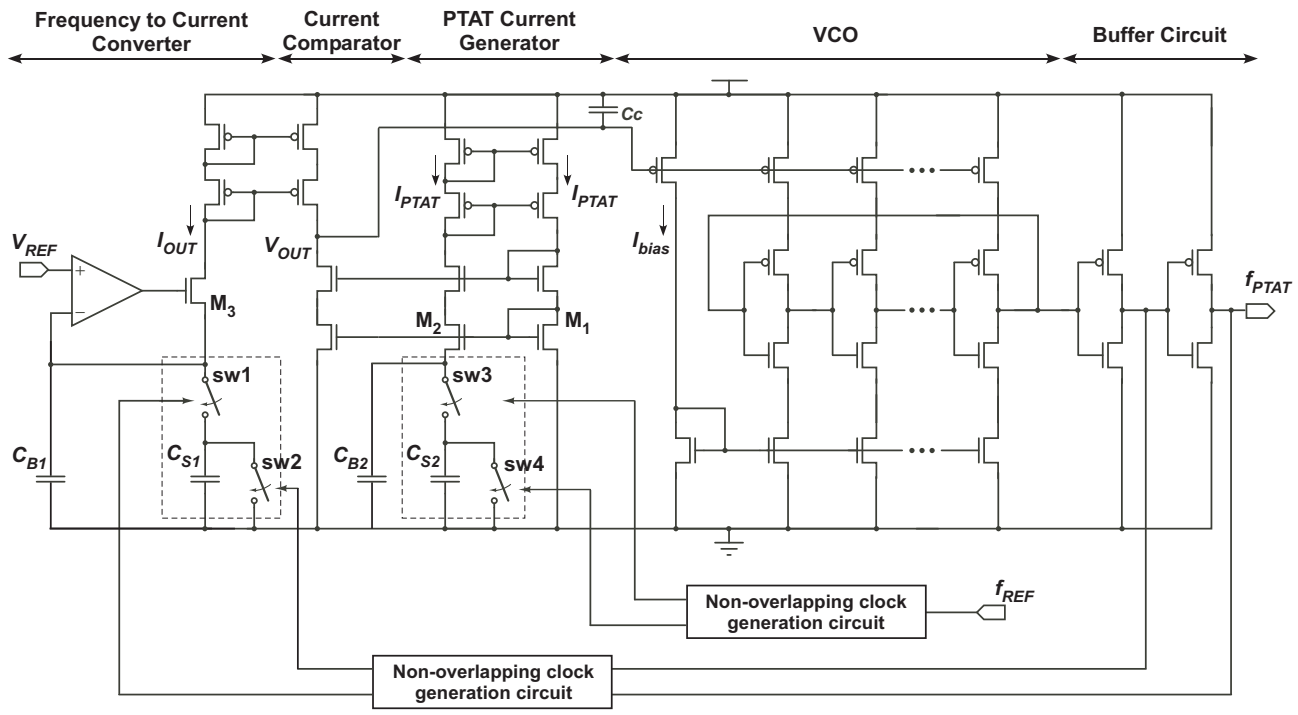

Fig. 4: Schematic of proposed PTAT clocke generator. All subcircuits are operated in subthreshold region.

of the frequency-to-current converter is

$$I_{OUT} = f_{PTAT} \cdot C_{S1} \cdot V_{REF}. \quad (6)$$

This current is copied into the current comparator through a current mirror. Because of feedback operation, the circuit operates so that output current I_{OUT} will be equal to PTAT current I_{PTAT}, and consequently, oscillation frequency f_{PTAT} will be

$$f_{PTAT} = \frac{C_{S2}}{C_{S1}} \cdot \frac{f_{REF}}{V_{REF}} \cdot \frac{\eta \cdot k_B T}{q} \ln\left(\frac{K_2}{K_1}\right). \quad (7)$$

Because f_{REF} and V_{REF} are independent of temperature, output frequency f_{PTAT} is a PTAT characteristics.

This way, a PTAT clock frequency can be obtained.

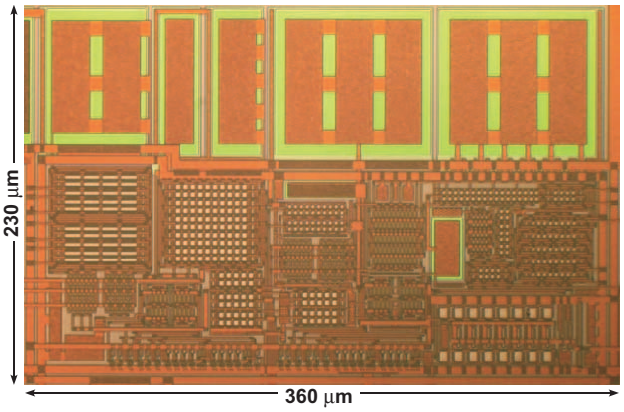

Fig. 5: Chip micrograph. Area is 0.08 mm^2.

5. Entire Configuration

Figure 4 shows the entire construction of our temperature sensor. The VCO consists of seven current-starved inverters connected in a ring. Non-overlapping clock generators of the PTAT current generator and the frequency-to-current generator were used to prevent switches (sw1-sw2 pair and sw3-sw4 pair) from simultaneously being turned on.

EXPERIMENTAL RESULTS

We fabricated a prototype chip with a 0.35-µm, 2-poly, 4-metal standard CMOS process. Figure 5 shows a micrograph of our prototype chip. The chip area is 0.08 mm^2(=230 µm × 360 µm). The supply voltage was set to 3 V (the nominal voltage of lithium-ion batteries). Reference voltage V_{REF} was set to 0.75 V and reference clock f_{REF} was set to 1 MHz. Capacitors C_{B1}, C_{B2}, and C_C remove high-frequency noise resulting from switching operation.

To evaluate the tolerance to device-parameter variations of the circuit, we measured three samples on different chips from the same wafer. Figure 6 shows the results, showing output frequency f_{PTAT} as a function of temperature in a range from 10°C to 80°C. As expected from Eq. (7), the value of f_{PTAT} increased linearly with temperature. The average temperature coefficient of the

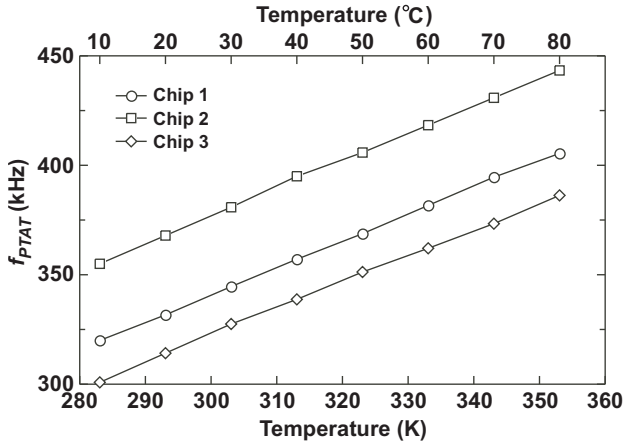

Fig. 6: Measured oscillation frequency f_{PTAT} as a function of temperature.

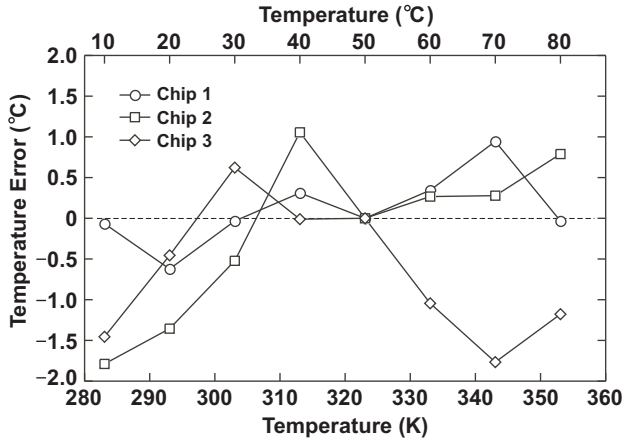

Fig. 7: Calculated temperature error after one-point calibration at 50°C.

three samples was 1.2 kHz/°C.

Strictly speaking, the measured value of f_{PTAT} had a small offset that depended on individual chips. In other words, the right side of Eq. (7) actually had an additional term that was independent of temperature. This was caused by the threshold voltage mismatch of transistor pairs (M_1, M_2) in the PTAT current generator. To reduce the offset error, we performed one-point calibration so that the offset at 50°C would be 0. With this calibration, we were able to assess the temperature from the value of f_{PTAT} within a small error of ±1.8°C as plotted in Fig. 7.

Table I summarizes the performance of our circuit. The power consumption was about 10 μW at a 2.2-V supply voltage. The line regulation was 0.8%/V. Our circuit would be useful for smart temperature-sensor LSIs that are required to operate with ultra-low-power consumption.

Table I: Performance Summary

Process	0.35 μm 2P4M CMOS
Supply Voltage	2.2 - 3.0 V
Temp. Range	10℃ - 80℃
T.C.	1.2 kHz/℃
Temp. Error	± 1.8℃
Line Regulation	0.8%/V
Power	10 μW (V_{DD} = 2.2 V)
Area	0.08 mm^2

CONCLUSION

We developed an ultra-low-power temperature sensor circuit consisting of subthreshold MOSFET circuits. The device generated a PTAT clock frequency. We made a prototype chip, using a 0.35-μm CMOS process, and demonstrated its operation through measurements. The accuracy of sensor output was within ±1.8°C in a temperature range from 10°C to 80°C, and the power dissipation was about 10 μW. Our sensor would be suitable for use in subthreshold-operated, power-aware LSIs.

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