

Image Sensor/Digital Logic 3D Stacked Module featuring Inductive Coupling Channels for High Speed/Low-Noise Image Transfer

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Abstract

This paper proposes 3D stacked module consisting of image sensor and digital logic dies connected through inductive coupling channels. Evaluation of a prototype module revealed radiation noise from the inductive coils to the image sensor is less than 0.4-LSB range along with ADC code, *i.e.*, negligible. Aiming at high frame rate image sensor/processing module exploiting this attractive off-die interface, we also worked on resolving another throughput-limiter, namely power consuming TDC used in column parallel ADCs. Novel intermittent TDC operation scheme presented in this paper can reduce its power dissipation 57% from conventional ones.

Introduction

Stacking image sensor and digital logic dies are getting wide attractions for 1) reducing image sensor die area, 2) optimizing sensor/logic fabrication process through functional separation, and 3) achieving faster image transfer (more than 1,000 fps) needed for smarter image processing. Unlike conventional approaches using TSVs, the paper proposes stacking the dies using parallel inductive coupling channels, called Through Chip Interfaces (TCIs), for achieving better cost, manufacturability, and energy consumption [1]. One of major contributions of this paper is to show there is actually no TCI-oriented radiation noise observed on an image sensor, allowing them to be placed near the pixel read circuits.

Integration Concept

Fig. 1 explains our 3D module concept. Since a single TCI can achieve more than 4Gbps throughput [1], top/bottom rows of TCIs operating in parallel can resolve bandwidth bottleneck in achieving 1,000 fps and higher inter-chip image transfer. We have test-cased single-TCI-domain image sensor/digital logic into one die, and then stacked two of them with 180 degree rotation. As our goal is to commoditize high speed image transfer by using TCI, we have also developed new column ADCs which can substantially enhance parallel column readability as explained in the following.

Circuit Configuration

Fig. 2 shows a micro-photograph of our fabricated chip using 0.18- μm 1P4M CIS process. The chip is divided into two halves. The left half (Tx side) consists of an image sensor, an asynchronous parallel to serial converter (P2S) that serializes 12-bit parallel pixel data, and a TCI-Tx. In the right half (Rx side), the received serial data at TCI-Rx are converted into 12-bit (parallel) pixel data by an asynchronous serial to parallel converter (S2P). The TCI-Tx includes two sets of coils/drivers (TCI Tx cir) for transferring a pair of data and clock, whereas the TCI-Rx includes a corresponding set of coils/amplifiers (TCI Rx cir). In addition to these pairs of Tx/Rx, 9 coils and drivers/amplifiers were placed just beneath the image sensor (350/280/170 μm coils x 150/120/120 μm distance, see also Fig.7, top right), in order for evaluating potential radiation noise interference from TCI circuits to the image sensor.

Single-slope ADCs (SS-ADCs) with a time-to-digital converter (TDC) have been proposed for high-speed single-slope ADC [2][3]. Conventional TDCs need to run continuously, where numbers of delay cells and D-FFs being driven by a high speed multi-phase clock, in order to keep the consistency between the stages of the ADC operation and to maintain robustness against meta-stability. This

results in high power consumption which becomes a limiter when applying TDC to column-parallel pixel read circuits for achieving higher frame rate.

We propose an intermittent TDC operation scheme that can reduce its power dissipation drastically (Fig. 3). The TDC runs continuously until the PWM signal of the SS-ADC falls. A “high” period of the PWM signal is defined as T_{PWM} . Here, we focus on the timing of the T_{PWM} falling edge and consider the delay signal, $T_{\text{PWM}} + \Delta T_{\text{PWM}}$, which is generated from T_{PWM} through normal delay cells. Then, we can make a time window ΔT_{PWM} and restrict the TDC to work only in this period. Fig. 4 shows detail circuit composition of the proposed ADC.

Experimental results

Fig. 5 shows an experimental setup for the 3D stacked module. The test board is controlled by a Xilinx Kintex-7 FPGA board through FMC connectors. Fig. 6 shows measured characteristics of sensor side. The ADC has 11-bit resolution with 1-bit redundancy. The DNL is +0.26/-0.23 LSB, and the INL is +7.5/-14.5 LSB. Degradation of the INL is caused by non-linearity of the ramp-wave generator. We also confirmed image capturing with 3ms exposure (in Fig. 6) and correct TCI communication in the 3D stacked module. Table 1 summarizes the chip characteristics. The ADC parts achieved 57% reduction of power dissipation from the conventional architecture [2-4].

Fig. 7 shows measured TCI-radiation-noise characteristics. In the noise evaluation, we supplied pseudorandom noise, which was synchronized to A/D-conversion timing, to only one selected TCI and measured LSB shift of the ADC code from the selected column ADC. Since the noise sequence is same in the SS-ADC period, the noise component doesn't disappear through averaging. We obtained 16,384 samples and averaged at each noise-interference measurements. Since radiation noise decreases in proportion to the cube of the distance, the interference component should have dependencies on (A)ADC-code, (B)Tx power, as well as (C)coil locations (TOP / CENTER / BOTTOM). Measured results show no such dependencies, meaning no radiation noise interference detected. Approximately -3 LSB offsets was observed (See also Fig.7, LSB shift of all measurements), however, compared with the TCI noise-free condition. We consider this offset is caused by minute IR drops which should have been solved by better power line design.

Conclusion

In the 3D stacked imager module featuring TCI, radiation-noise dependencies were not observed. It indicated that the presented geometry was one of the possible configuration for low-noise image transfer by using TCIs, and will be valuable for subsequent design of 3D-stacked imager/logic modules featuring TCIs. Combining the intermittent TDC architecture gathers high-speed readout and low power consumption for pixel data transfer.

Acknowledgment

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References

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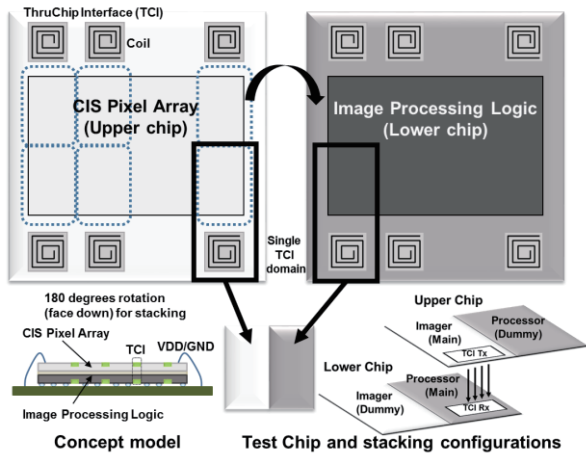


Fig. 1 Imager/logic 3D stacked module concept

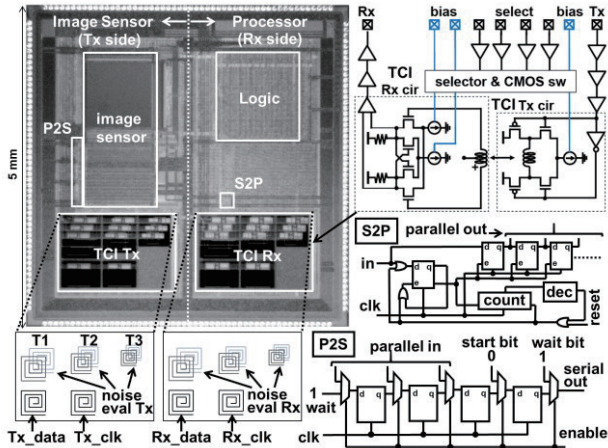


Fig. 2 Facilitated chip and TCI.

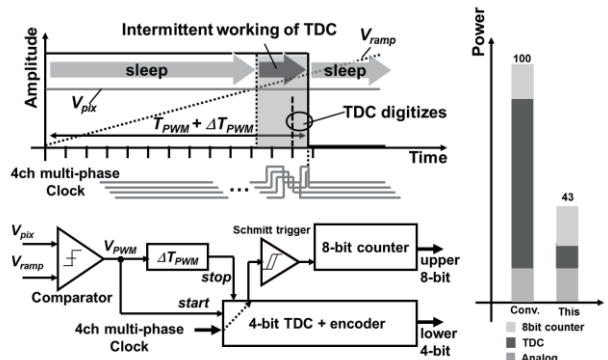


Fig. 3 Configuration of proposed column ADC.

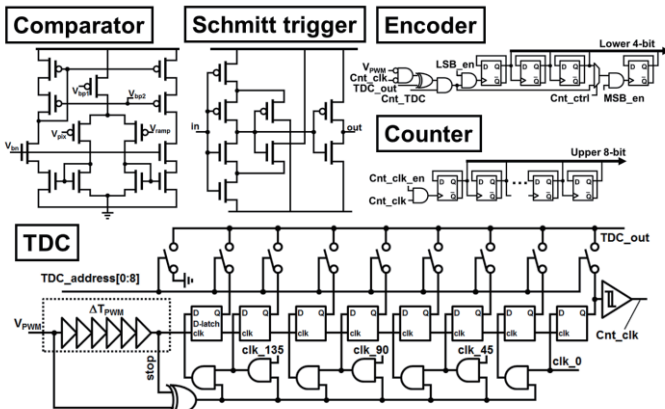


Fig. 4 Detail circuits composition of proposed ADC

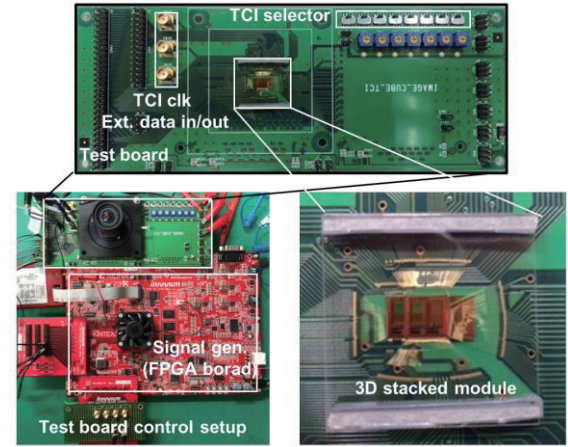


Fig. 5 Prototype board of 3D stacked module with TCI.

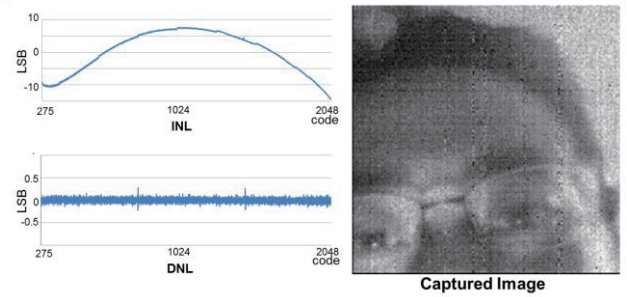


Fig. 6 Measured characteristics of sensor side.

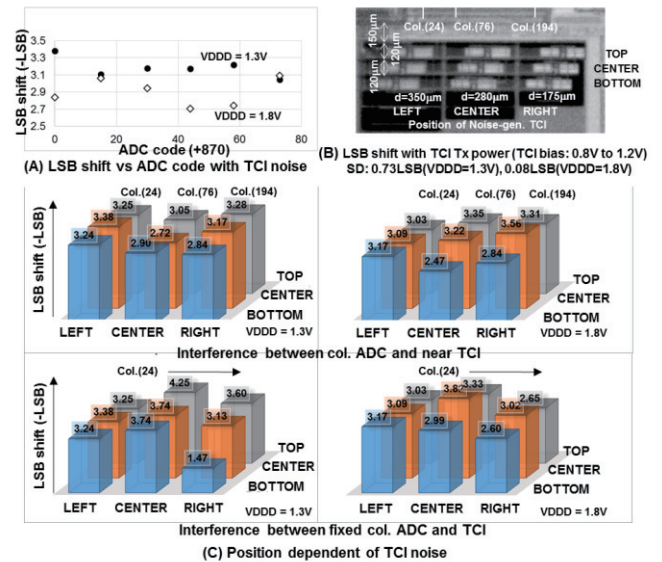


Fig. 7 Measured characteristics of TCI noise.

TABLE I
CHIP CHARACTERISTICS

Process	0.18- μ m CMOS 1P4M
Pixel pitch, res.	5 μ m, 200x200
Voltage supply	3.3V(analog) / 1.8V to 1.3V(digital)
ADC, TDC res.	11 bits (+ 1 bit), 625ps
Sampling rate	200kS/s@100MHz
ADC power	108 μ W/col. (This work)
VDDD=1.8V	247 μ W/col. (Normal SSADC+TDC)
ADC power	71 μ W/col. (This work)
VDDD=1.3V	141 μ W/col. (Normal SSADC+TDC)
DNL, INL	+0.26/-0.23, +7.6/-14.5