Noise-Tolerant Analog Circuits for Sensory Segmentation based on Symmetric STDP Learning

Gessyca Maria Tovar, Tetsuya Asai, and Yoshihito Amemiya

Graduate School of Information Science and Technology, Hokkaido University
Kita 14, Nishi 9, Kita-ku, Sapporo, 060-0814 Japan
gessyca@sapiens-ei.eng.hokudai.ac.jp,
http://lalsie.ist.hokudai.ac.jp/

Abstract. We previously proposed a neural segmentation model suitable for implementation with complementary metal-oxide-semiconductor (CMOS) circuits. The model consists of neural oscillators mutually coupled through synaptic connections. The learning is governed by a symmetric spike-timing-dependent plasticity (STDP). Here we demonstrate and evaluate the circuit operation of the proposed model with a network consisting of six oscillators. Moreover, we explore the effects of mismatch in the threshold voltage of transistors, and demonstrate that the network was tolerant to mismatch (noise).

Key words: Analog circuits, Neural networks, Spiking neurons, STDP, Neural segmentation, Noise tolerance

1 Introduction

One of the most challenging problems in sensory information processing is the analysis and understanding of natural scenes, i.e., images, sounds, etc. These scenes can be decomposed into coherent "*segments*". The segments correspond to different components of the scene. Although this ability, generally known as sensory segmentation, is performed by the brain with apparent ease, the problem remains unsolved. Several models that perform segmentation have been proposed [1]-[3], but they are often difficult to implement in practical integrated circuits. In [4] we proposed a simple neural segmentation model that is suitable for analog CMOS circuits. The model consisted of mutually-coupled neural oscillators. The oscillators were coupled with each other through positive or negative synaptic connections.

In this paper, we demonstrate and evaluate the circuit operation of the proposed model with a network consisting of six oscillators. Moreover, we conduct Monte-Carlo simulations to study the effects of threshold mismatch among transistors in our network using three oscillators, and we demonstrate that the network is tolerant to the mismatch (noise).

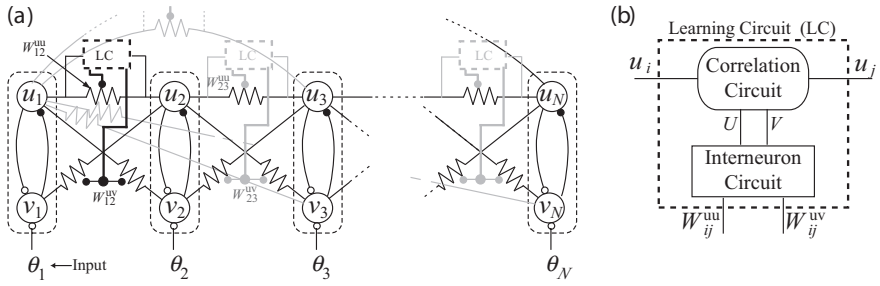

Fig. 1. a) network construction of segmentation model, and b) learning circuit model.

2 The model

Our segmentation model is shown in Fig. 1(a). The network has N Wilson-Cowan type neural oscillators (u_i output of i-th activator and v_i output of i-th inhibitor). The oscillators are coupled with each other through resistive synaptic connections. The dynamics are defined by

$$\tau \frac{du_i}{dt} = -u_i + f_{\beta_1}(u_i - v_i) + \sum_{j \neq i}^{N} W_{ij}^{\mathrm{uu}} u_j, \tag{1}$$

$$\frac{dv_i}{dt} = -v_i + f_{\beta_2}(u_i - \theta_i) + \sum_{j \neq i}^{N} W_{ij}^{\mathrm{uv}} u_j, \tag{2}$$

where τ represents the time constant, N is the number of oscillators, θ_i is the external input to the i-th oscillator, and $f_{\beta_i}(x)$ is the sigmoid function defined by $f_{\beta_i}(x) = [1 + \tanh(\beta_i x)]/2$. Also, W_{ij}^{uu} represents the connection strength between the i-th activator and j-th activator, and W_{ij}^{uv} the strength between the i-th activator and the j-th inhibitor. Each neuron accepts external inputs, e.g., sound inputs, and oscillates (or does not oscillate) when the input amplitude is higher (or lower) that a given threshold. For a more detailed explanation, refer to [4].

The easiest way to segment neurons is to connect the activators belonging to the same (or different) group with positive (or negative) synaptic weights. However, circuits that implement positive and negative weights may occupy a large area on analog LSIs, which prevents us from implementing large-scale networks. Therefore, instead of using negative weights, we used positive synaptic weights between the activator and inhibitors [4]. These weights are updated by learning circuits. As shown in Fig 1(a), the learning circuits (LCs) are located between two activators. Each of them consists of a correlation circuit and an interneuron circuit (see Fig. 1(b)). Therefore, let us start with the explanation of the correlation circuit. In our model, neurons should be correlated (or anti-correlated) if they receive synchronous (or asynchronous) inputs. Based on

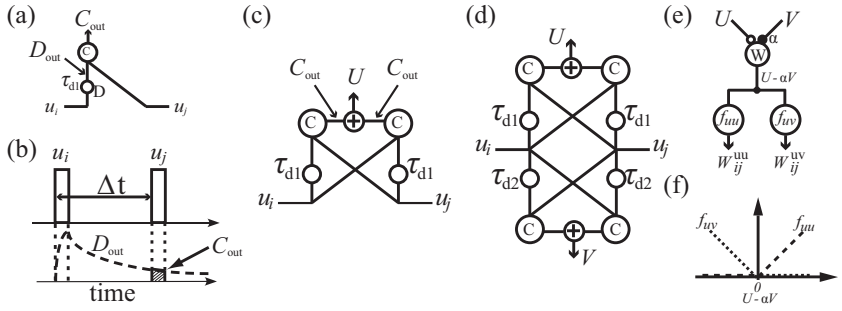

Fig. 2. a) basic unit of Reichardt's correlation network, b) Reicherdt's network operation, c) unit pair, d) correlation circuit, e) model of interneuron circuit, and f) input-output characteristics of piecewise linear functions (f_{uu} and f_{uv}).

this assumption, the synaptic weights are updated on the basis of symmetric spike-timing-dependent plasticity (STDP) using Reichardt's correlation neural network [5]. The basic unit is illustrated in Fig. 2(a). It consists of a delay neuron (D) and a correlator (C). The delay neuron produces blurred (delayed) output $D_{\rm out}$ from spikes produced by activator (u_i). The dynamics are given by $\tau_{\rm d1} dD_{\rm out}/dt = -D_{\rm out} + u_i$, where $\tau_{\rm d1}$ represents the delay time constant. The correlator accepts $D_{\rm out}$ and spikes produced by activator (u_j), and outputs $C_{\rm out}$ ($\equiv D_{\rm out} \times u_j$). The operation is illustrated in Fig. 2(b). Since this basic unit can calculate correlation values only for positive inter-spike intervals Δt, we used a unit pair consisting of two basic units, as shown in Fig. 2(c). The output (U) is obtained by summing the two $C_{\rm out}$s. Through temporal integration of U, we obtained a Gaussian-type response for Δt [4]. The sharpness of this response increased as $\tau_{\rm d1} \rightarrow 0$, so introducing two unit pairs with different time constants, e.g., $\tau_{\rm d1}$ and $\tau_{\rm d2}$ ($\tau_{\rm d1} \ll \tau_{\rm d2}$), we obtained two responses for U and V with different sharpness. Then, the weighted subtraction ($U - \alpha V$) produced the well-known Mexican-hat characteristic that we used as STDP in the oscillator network [4]. The correlation circuit is shown in Fig. 2(d).

The two outputs (U and V) of the correlation circuits are given to the interneuron circuit shown in Fig. 2(e). Interneuron W receives outputs of the correlation circuit (U and V), and performs the weighted subtraction ($U - \alpha V$). When $U - \alpha V$ is positive, neurons u_i and u_j in Fig. 2(d) should be correlated, and the weight between activators ($W_{ij}^{\rm uu}$) should be increased. On the other hand, when $U - \alpha V$ is negative, the neurons should be anti-correlated, and the weight between the activator and inhibitor ($W_{ij}^{\rm uv}$) should be increased. The output of interneuron W is given to two additional interneurons (f_{uu} and f_{uv}). The input-output characteristics of these interneurons are shown in Fig. 2(f). The outputs of these interneurons are given to the weight circuit (represented by resistors in the model; Fig. 1(a)) in order to modify the positive resistances. For a more detailed explanation and simulation of the model refer to [4].

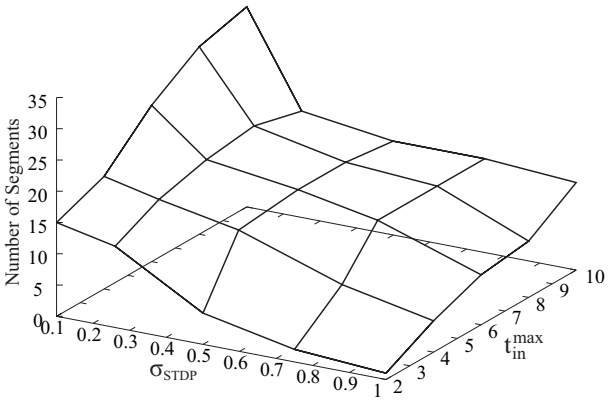

Fig. 3. simulation results showing segmentation ability of the network

We newly carried out numerical simulations to evaluate the "segmentation ability," which represents the number of survived segments after the learning. The number of segments as a result of the network's learning strongly depends on the STDP characteristic as well as the input timing of neurons (Δt). Let us remember that neurons that fire "simultaneously" should be correlated. "Simultaneously" is to be defined by some "time windows of coincidence" that we call σ_{STDP}. Thus, neurons that receive inputs within the time windows should be correlated. Simulation results are shown in Fig. 3. The number of neurons (N) was set to 50. The neurons received random inputs within time $t_{\mathrm{in}}^{\mathrm{max}}$ (maximum input timing). We observed that when σ_{STDP} was 1 and neurons received their inputs within time 2, the number of segments was about 2. The contrary was observed when σ_{STDP} was 0.1 and $t_{\mathrm{in}}^{\mathrm{max}}$ was 10, where the number of segments was about 35.

3 CMOS circuits

Construction of a single neural oscillator is shown in Fig. 4(a). The oscillator consists of two standard differential amplifiers (a differential pair and a current mirror) and two additional capacitors C_1 and C_2. A circuit implementing Reichardt's basic unit (see Fig. 2(a)) is shown in Fig. 4(b). The circuit has a delayer and a correlator. The delayer consists of a bias current source (I_1), current mirrors (m_1-m_2 and m_5-m_6) and a pMOS source-common amplifier (m_2-m_4). The correlator consists of three differential pairs (m_{12}-m_{13}, m_{14}-m_{15} and m_{16}-m_{17}), a pMOS current mirror (m_{19}-m_{20}), a bias transistor (m_{18}) and a bias current source (I_2). We employed floating gate MOS FETs for m_{12}, m_{14} and m_{17} to decrease the gain of the differential pairs. Detailed operations and simulation results of these two circuits are explained in [6].

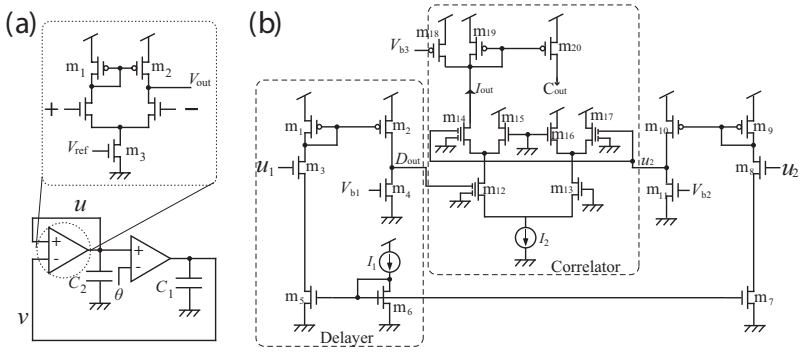

Fig. 4. a) neural oscillator circuit [6], and b) Reichardt's basic unit circuit [6]

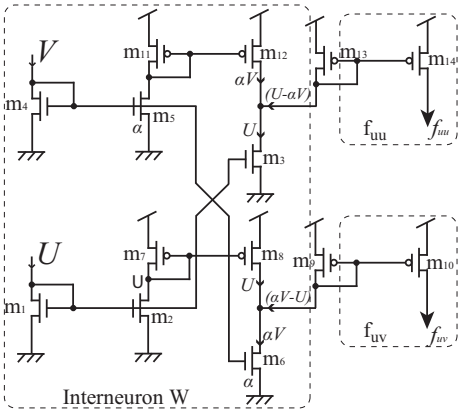

Fig. 5. interneuron circuit

A basic circuit implementing the interneurons (W, f_{uu} and f_{uv}) is shown in Fig. 5. The circuit consists only of current mirrors. Input current U (from Reichardt's circuit; correlation circuit) is copied to m_3 by current mirror m_1-m_3, and is copied to m_8 by current mirrors m_1-m_2 and m_7-m_8. At the same time, input current V is copied to m_6 by current mirror m_4-m_6, and is copied to m_{12} by current mirrors m_4-m_5 and m_{11}-m_{12}. Recall that we need the subtraction of $U - \alpha V$ to produce the Mexican-hat characteristic. Therefore, we set the weight (α) as $\alpha \equiv W_5/L_5 \cdot L_4/W_4 = W_6/L_6 \cdot L_4/W_4$, where W_i and L_i represent the channel width and length of transistor m_i, respectively. So, when current U is higher than current αV, current f_{uu} is outputted by current mirror m_{13}-m_{14}. Otherwise, current f_{uv} is outputted by current mirror m_{11}-m_{12}.

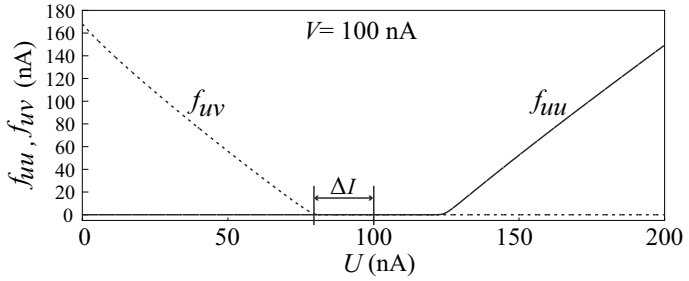

Fig. 6. circuit simulation results of interneuron circuit

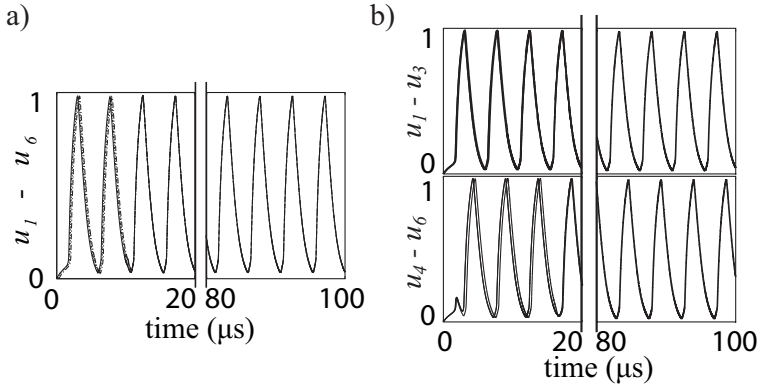

Fig. 7. circuit simulation results for a) inter-spike interval $\Delta t = 0$, and b) $\Delta t = 3$ μs.

4 Simulation results

First we carried out circuit simulations for the interneuron circuit. The parameters used for the transistors were obtained from MOSIS AMIS 1.5-μm CMOS process. Transistors sizes (W/L) were 4 μm/1.6 μm for m_1-m_4, 10 μm/1.6 μm for m_5 and m_6, 4.5 μm/16 μm for m_8 and m_{12}, 3.5 μm/16 μm for m_{13}, and 4 μm/16 μm for the rest transistors. The supply voltage was set to 5 V. Input current V was set to 100 nA, and input current U varied from 0 to 200 nA. The simulation results are shown in Fig. 6. When $U + \Delta I < V$ where $\Delta I \approx 20$ nA, output current f_{uv} flowed and f_{uu} was 0. When $U - V < \Delta I$, both f_{uu} and f_{uv} were 0. When hen $U - \Delta I > V$, f_{uu} flowed while f_{uv} remained at 0.

Next, we carried out circuit simulations of the circuit network with $N = 6$. Transistor sizes (W/L) for the Recichardt's basic circuit (see Fig. 4(b)) were 4 μm/1.6 μm for nMOS transistors and m_{20}, and 4 μm/16 μm for the rest of the transistors. Voltages V_{b2} and V_{b3} were set to 550 mV and 4.08 V respectively, while V_{b1} was set to 510 mV for delay τ_{d1}, and was set to 430 mV for delay τ_{d2}.

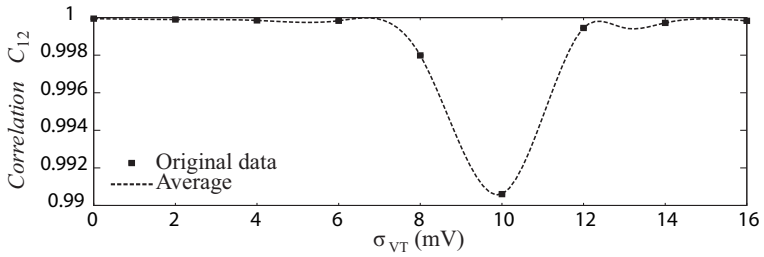

Fig. 8. correlation values between neurons u_1 and u_2 for different σ_{VT}.

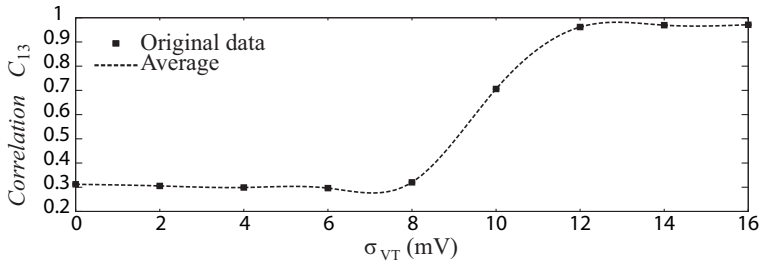

Fig. 9. correlation values between neurons u_1 and u_3 for different σ_{VT}.

With these settings, we obtained positive W ($U - \alpha V$; see Fig. 2(e)) for $|\Delta t| \leq 1$ μs, and obtained negative W for $|\Delta t| > 1$ μs. In other words, when $|\Delta t| \leq 1$ μs, neurons should be correlated, otherwise, they should be anti-correlated, as explained before.

The normalized time courses of u_is ($i = 1 \sim 6$) are shown in Figs. 7(a) and (b). As shown in Fig. 7(a), at $t = 0$, external inputs θ_i ($i = 1 \sim 6$) were 2.5 V, which is equivalent to Δt=0. We observed that all neurons were gradually synchronized. On the contrary, Fig. 7(b) shows that at $t = 0$ external inputs $\theta_{1,2,3}$ were set to 2.5 V, and inputs $\theta_{4,5,6}$ were set to 0. Then, at $t = 3$ μs $\theta_{4,5,6}$ were set to 2.5 V, which is equivalent to $\Delta t = 3$ μs. We observed that $u_{1,2,3}$ and $u_{4,5,6}$ were desynchronized without breaking synchronization among neurons in the same group that were gradually synchronized. This indicated that segmentation of neurons based on the input timing was successfully achieved.

To consider the noise tolerance of the network, we carried out Monte-Carlo simulations in our circuit network with $N = 3$. The parameter V_{th} (threshold voltage) of all transistors was varied using Gaussian noises with standard deviation σ_{VT}. When $t = 0$, external inputs to neurons (θ_1, θ_2, θ_3) were set to (2.5,0,0)V. Then, at $t = 1$ μs, (θ_1, θ_2, θ_3) were set to (2.5,2.5,0)V, whereas they were set to (2.5,2.5,2.5)V at $t = 2.4$ μs. In other words, neurons u_1 and u_2 should be synchronous with each other, and they should be asynchronous with u_3 because of Δt=1.4 μs. To evaluate the performance of the network, we calculated

correlation values C_{ij} between neurons u_i and u_j given by

$$C_{ij} = \frac{\langle u_i u_j \rangle - \langle u_i \rangle \langle u_j \rangle}{\sqrt{\langle u_i^2 \rangle - \langle u_i \rangle^2} \sqrt{\langle u_j^2 \rangle - \langle u_j \rangle^2}}. \quad (3)$$

We calculated C_{12} and C_{13} to evaluate the synchronicity between segments. Figures 8 and 9 show the simulation results. As observed in the figures, when σ_{VT} <10 mV neurons u_1 and u_2 were correlated, while the correlation value (C_{13}) between neurons u_1 and u_3 was low, i.e., they were anti-correlated. Due to imperfections of the CMOS fabrication process, device parameters, e.g., threshold voltage, etc., suffer large variations [7]. These variations among transistors cause a significant change in general analog circuits. Nevertheless, the results obtained in Figs. 8 and 9 showed that our network successfully segmented neurons for σ_{VT}s lower than 10 mV, which indicated that the network is tolerant to threshold mismatch among transistors.

5 Conclusion

Previously, we proposed a neural segmentation model that is suitable for analog VLSIs using conventional CMOS technology. We proposed a novel segmentation method based on a symmetric spike-timing dependent plasticity (STDP) using Reichard's correlation neural networks. In this paper, we evaluated the segmentation ability of the network through numerical simulations. In addition we proposed and evaluated basic circuits for constructing segmentation hardware. We demonstrated the operation of the circuit network using six neurons. Finally, we explored the effect of threshold mismatches among transistors in our network with three oscillators, and showed that the network was tolerant to device mismatches.

References

1. Han, S. K., Kim, W. S., Kook, H.: Temporal segmentation of the stochastic oscillator neural network. Physical Review E. 58, 2325–2334 (1998)
2. Von der Malsburg, C., Schneider, W.: A neural cocktail-party processor. Biological Cybernetics. 54, 29–40 (1986)
3. Wang D. L., Terman, D.: Locally excitatory globally inhibitory oscillator networks. IEEE Trans. on Neural Networks. 6(1), 283–286 (1995)
4. Fukuda, E. S., Tovar, G. M., Asai, T., Hirose, T., Amemiya, Y.: Neuromorphic CMOS Circuits Implementing a Novel Neural Segmentation Model Based on Symmetric STDP Learning. J. Signal. Procc. 11(6), 439–444 (2007)
5. Reichardt, W.: Principles of Sensory Communication. Wiley, New York (1961)
6. Tovar, G. M., Fukuda, E. S., Asai, T., Hirose, T., Amemiya, Y.: Analog CMOS Circuits Implementing Neural Segmentation Model Based on Symmetric STDP Learning. In: 14th International conference on Neural information Processing, pp. 306–315. Japan (2007)
7. Pelgrom, M. J. M., Duinmaijer, A. C. J., Welbers, A. P. G.: Matching Properties of MOS Transistors. J. Solid-State Circuits. 24(5), 1433–1440 (1989)