

# Depressing Properties of a Hardware Synapse on a Single-Layer Nanodot Array

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## Abstract

A simple single-electron circuit on a single-layer nanodot array for depressing synapses is proposed. The circuit can be used as a unit element on spiking neural networks and its applications. Although our synapse circuit consists of only three single-electron oscillators, they emulate fundamental properties of depressing synapses. We verify operations of our depressing synapse circuits by using computer simulation. Furthermore, we demonstrate collective operations of the circuits in contrast-invariant pattern classification and synchrony detection.

## 1. Introduction

Synaptic depression, network dynamics and their applications have attracted recently the attention of many modelers who mainly focused on the dynamic implications of neural systems. Abbott *et al.*, for example, reported a striking feature of synaptic transmission between neurons where post-synaptic firing rates for input spike trains are limited upto some value because of short-term synaptic depression [1]. On the other hand, interesting applications on various neural networks with depressing synapses have been proposed [2], [3], [4], and several hardware synapses on neuromorphic CMOS devices have been fabricated [5], [6]. Such neuromorphic devices will act as novel information processing devices in the future. In this report, we design a single-electron depressing synapse (SEDS) that is contrived to be constructed on a single-layer nanodot array, and show that device implementation of the SEDSs on such nanodot array is much easier than that of depressing synapses on CMOS VLSIs.

## 2. Single-electron depressing synapse circuit

To design a depressing synapse circuit, we use a pair of single-electron oscillators (Fig. 1 (a)) that has been proposed for an excitable media [7] and a spiking neuron circuit [8]. The oscillator consists of a tunneling junction ( $C_j$ ), a conductive device ( $g$ ), and a bias voltage source ( $V_{dd}$ ). The oscillator has an island node  $n_i$  where excess electrons are stored.

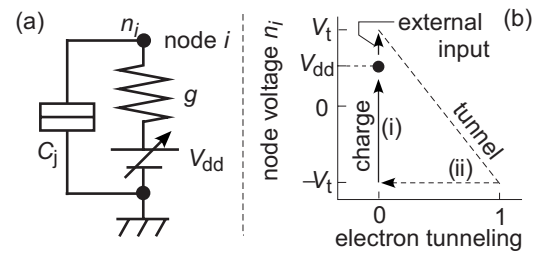


Figure 1: Single-electron oscillator and phase diagram.

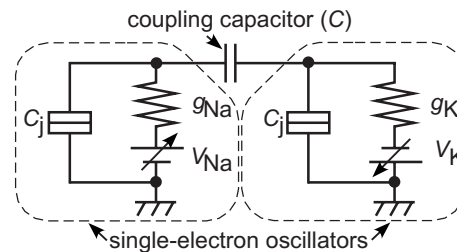


Figure 2: Depressing synapse circuit with single-electron oscillator.

Figure 1 (b) is a nominal phase diagram of this circuit for positive  $V_{dd}$ . The vertical and horizontal axes represent node voltage  $n_i$  and a tunneling phenomenon [= 1 (when an electron tunnels), 0 (else)] at  $C_j$ . Note that trajectories between the tunneling phenomenon (0 and 1) in the figure do not have any quantitative physical meaning but have been used only to explain this circuit's operation. We have assumed that  $V_{dd} < e/2C_j$  ( $\equiv V_T$ : tunneling threshold voltage of junction  $C_j$ ). Since tunneling junction  $C_j$  is charged by  $V_{dd}$  [(i) in Fig. 1 (b)], the circuit is stable when  $n_i = V_{dd}$ . Under this resting condition, if  $n_i$  is further increased by an external input and exceeds  $V_T$ , an electron tunnels from the ground to node  $i$  through junction  $C_j$ , which results in the sudden decrease of  $n_i$  from  $V_T$  to  $-V_T$  [(ii) in Fig. 1 (b)]. Then  $V_{dd}$  starts charging  $C_j$  and the circuit become stable again [(i) in Fig. 1 (b)]. Note that there is a time lag from when the junc-

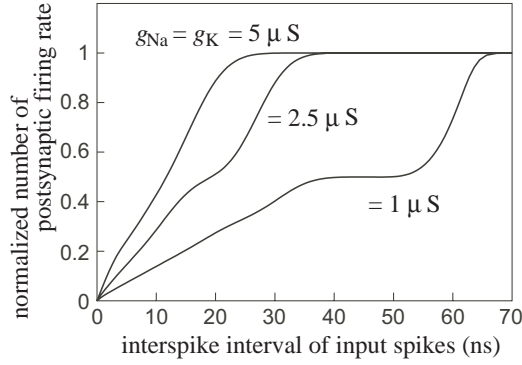


Figure 3: Changes in postsynaptic firing rate of depressing synapse circuit against interspike interval of input spikes.

tion voltage exceeds  $V_T$  to when tunneling actually occurs. We utilized this “monostable” (excitable) oscillatory property to produce depressing characteristics of synapses; i.e., we regard an array of oscillators as a depressing synapse because input spike trains are depressed by each neuron operating in its refractory period. Therefore, we can use an array of single-electron oscillators to construct the SEDS (Fig. 2). It should be noted that the term of the refractory period increases as values of  $g_{Na}$  and  $g_K$  increase [7].

There exists a neuromorphic relationship between the proposed SEDS and electronic Hodgkin-Huxley (H-H) models: i) a tunneling junction ( $C_j$ ) corresponds to a membrane capacitance and voltage-controlled gates in H-H models, ii) nonlinear chemical reactions between  $Na^+$  and  $K^+$  can be mediated by a coupling capacitance ( $C$ ) because of the neuron’s dielectric inside the soma.

### 3. Results

We examined depressing properties of a single SEDS by numerical simulations. We used typical parameter values for the single-electron circuit [7], except for  $g_{Na}(=g_K) = 5 \mu S, 2.5 \mu S$  and  $1 \mu S$ . Figure 3 shows synaptic conductivities ( $\sim$  the number of postsynaptic spikes) for interspike intervals (ISI) of input spike trains. As the ISI increases, the conductivity increases because each SEDS can easily be recovered from its depressed (refractory) period as the ISI increases. Because the depressed period increases as  $g_{Na}$  and  $g_K$  increase, the SEDS’s conductivity for increasing ISIs decreases significantly.

In the following subsections, we consider two applications of our synapse circuit. Section 3.1 describes an application to the Bugmann’s neural network for contrast-invariant pattern classification [2]. Section 3.2 describes an application to the Senn’s neural network for synchrony detection [3].

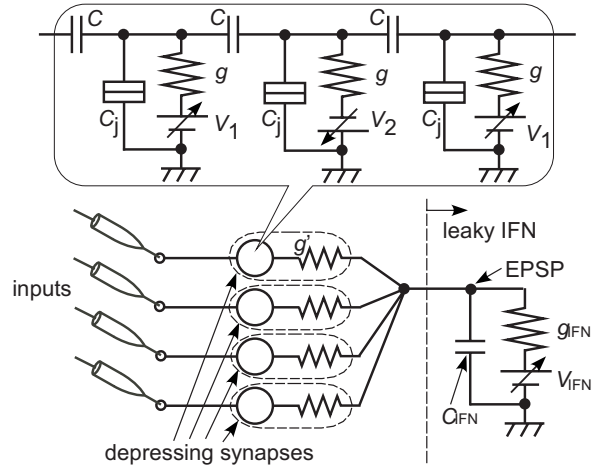


Figure 4: Circuit configuration of depressing synapses with leaky IFN circuit.

#### 3.1. Application to the Bugmann’s Neural Network

Bugmann showed that the strength of a time-averaged current injected into the soma by using a spike train tends to be independent of its frequency, which implies that the response strength of a target neuron depends only on the number of active inputs [2]. We here demonstrate it by using our depressing synapse circuits.

Let us assume a simple circuit, as shown in Fig. 4. The circuit is designed based on the construction of the Bugmann’s neural network. The right part represents a leaky integrate-and-fire neuron (IFN) and the left part represents its dendrite with our synapse circuits. The IFN consists of a membrane capacitance ( $C_{IFN}$ ) and a leak conductance ( $g_{IFN}$ ) with a bias voltage source ( $V_{IFN}$ ). In this paper, a threshold ( $V_{th}$ ) detector is omitted from our IFN circuit; i.e., our IFN circuit never fires. The IFN accepts spike inputs from excitatory neurons through depressing synapses. If the IFN circuit has a firing function, it outputs a spike when its EPSP  $> V_{th}$ , and resets the EPSP after the firing. In this setup, average values of the EPSP increases in proportion to the number of presynaptic active neurons. Therefore, it can detect the number of presynaptic active neurons by setting appropriate threshold  $V_{th}$  corresponding to the number of active neurons. On the other hand, the EPSP also increases in proportion to firing rate of spiking neurons. Therefore, the performance to discriminate the number of presynaptic active neuron largely deteriorates if the firing rate is not constant value.

It is shown that this discrimination performance is improved by using the depressing synapse [2]. If input spikes are given to the depressing synapse successively in a short period, the efficiency to increase the EPSP per spikes drops. Even if the number of input spikes increases with the increase in firing rate, the value of EPSP does not change greatly be-

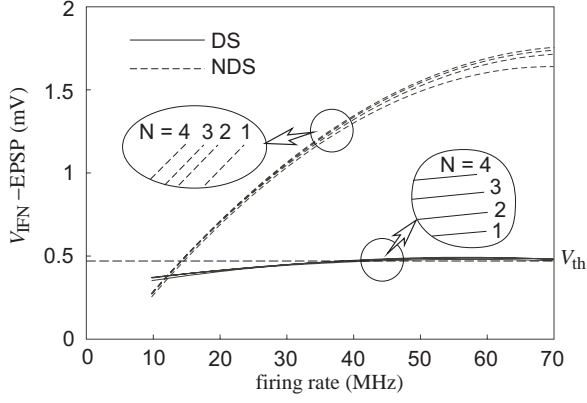


Figure 5: Changes in EPSP of IFN against the number of active presynaptic neuron and their firing rates.

cause the efficiency per spike is lowered by the synaptic depression. Namely, the discrimination performance of the network tends to be independent of firing frequency. To demonstrate this, we construct a network in which four synapse circuits are connected to the IFN circuit. We compared the operation of the neuron circuit with nondepressed- and depressed circuit as the number of active presynaptic neurons increases (Fig. 5). In the figure,  $N$  represents the number of active inputs. In case of the nondepressed synapse ( $g_{Na} = g_K = 5 \mu S$ , and it is labeled as NDS in the figure), averaged value of the EPSP increased monotonically as the firing rate of postsynaptic neurons increased. The value also increased as  $N$  increased. On the other hand, in case of the depressed synapse ( $g_{Na} = g_K = 1 \mu S$ , and it is labeled as DS in the same figure), the EPSP increased nonmonotonically as the firing rate of postsynaptic neurons increased. Now, we define the firing threshold of the IFN as  $V_{th} = 0.48$  mV. The firing rates when the EPSP exceeded the threshold to the number of active neurons were plotted in Fig. 6 for both depressed (DS) and nondepressed (NDS) synapse circuits. The result indicates that the dependence of the postsynaptic neuron with depressed synapses on presynaptic firing rates is smaller than of nondepressed synapses.

### 3.2. Application to the Senn's neural network

Senn showed that an easy way to extract coherence information among cortical neurons by projecting spike trains through depressing synapses onto a postsynaptic neuron [3]. We here demonstrate it by using our synapse circuits.

Let us consider the same IFN as shown in Fig. 4. We here employ burst neurons as inputs to the IFN, as in the Senn's original work. During a burst input, the output current of the depressing synapse circuit that flows via a conductance ( $g'$ ) rapidly decreases for successive spikes due to the refractory properties of the single-electron oscillator. But during a non-

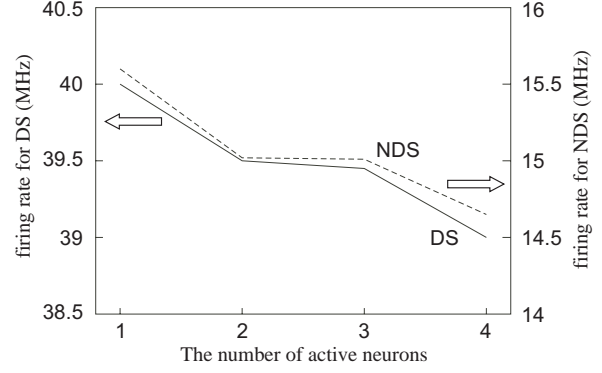


Figure 6: Results for dependence of IFN on the firing rate of presynaptic neurons (4 neurons).

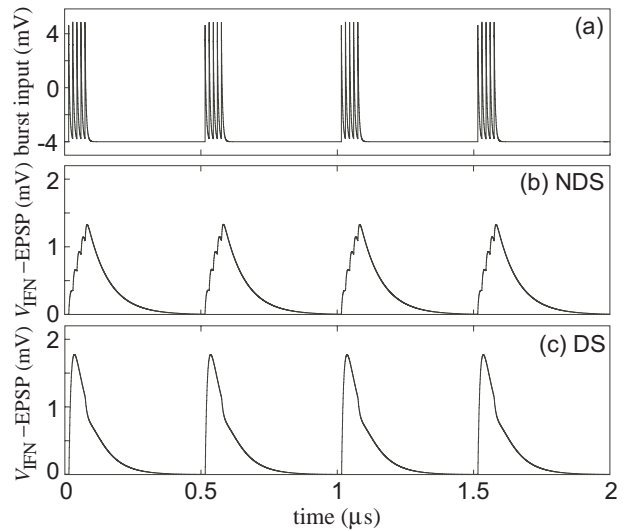


Figure 7: Responses of EPSP for single burst input (a) via nondepressed (b) and depressed synapse circuit (c).

bursting period, the oscillator has time to be a state of a resting period, and this results in a strong EPSP at the onset of the next burst. If we compare this dynamic response with that for a nondepressed synapse evoking on average the same EPSP, the depressed synapse will have a larger response at the burst onset and smaller response toward the end of the burst.

Figure 7 show the response of the EPSP with bursting inputs (a) for a nondepressed synapse (b) and depressed synapse circuit (c). The result ensures that the EPSP caused by the depressed synapse circuit has a larger response at the burst onset, as compared with nondepressed synapse circuit.

Now we demonstrate that the depressing synapse circuit is able to detect the synchrony in the burst times. We employ two bursting neurons as the input of the IFN that receive the burst inputs through depressed or nondepressed synapses.

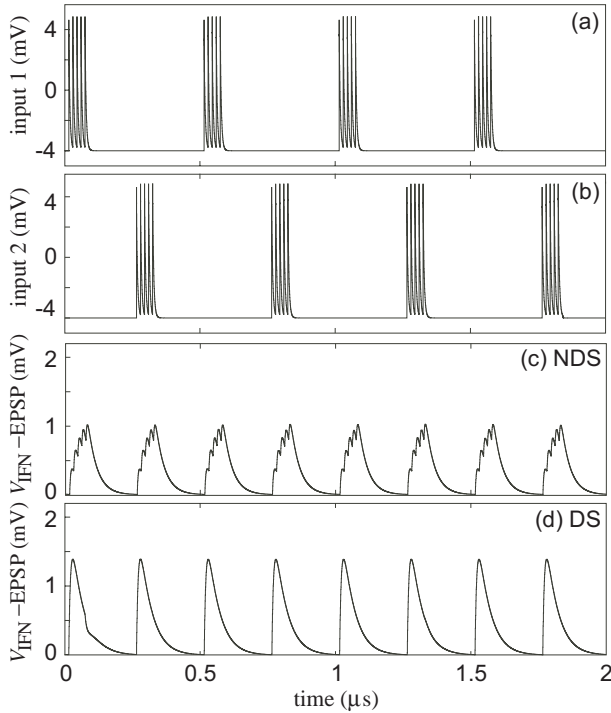


Figure 8: Responses of EPSP for asynchronous burst input [(a) and (b)] via nondepressed (c) and depressed synapse circuit (d).

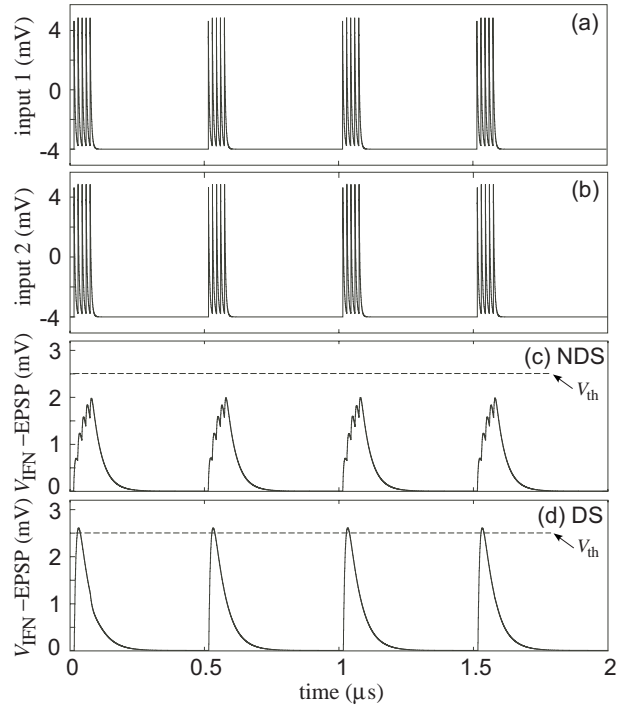


Figure 9: Responses of EPSP for synchronous burst input [(a) and (b)] via nondepressed (c) and depressed synapse circuit (d).

Figure 8 and 9 show the results. When the input bursts are not synchronized [Fig. 8 (a) and (b)], the peak EPSPs evoked by nondepressed [Fig. 8 (c)] and depressed synapses [Fig. 8 (d)] were both around 1 mV. But, when the input bursts are synchronized [Fig. 9 (a) and (b)], the peak EPSPs evoked by depressed synapses [Fig. 9 (d)] was significantly larger than the nondepressed synapses [Fig. 9 (c)]. Therefore, defining an appropriate threshold  $V_{th}$  of the IFN; e.g.,  $V_{th} = 2.5$  mV in the experiments, the IFN with the depressing synapse circuit can fire when the burst inputs are synchronized.

#### 4. Conclusions

We proposed an electrical depressing synapse with a single-electron circuit. The circuit was designed by using only three single-electron oscillators. By using the synapse circuit, we demonstrated two functional neural networks. Conventional computing with single-electron devices are generally based on binary logic decision. Such devices, however, bring us up some issues of device failure or thermal noise. In contrast, by mimicking computing structure of noise- and fault-tolerant neural networks on single-electron circuit, we may obtain possible solutions to the device issues in conventional single-electron computing.

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