within an acceptable range, the output signal is considered synchronised with the reference one. The phase-shift waveforms of such a PSS with $m=3$ are shown in Fig. 3.

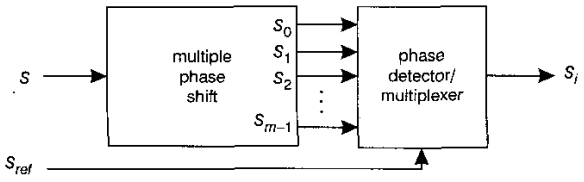

Fig. 2 *Scheme of PSS*

The multiple phase shift unit has multiple outputs $S_0, S_1, S_2, \ldots, S_{m-1}$ with same frequency but different phases. The phase detector/multiplexer detects phase between S_{ref} and each of $S_0, S_1, \ldots, S_{m-1}$. The output signal is the one with minimum phase difference from S_{ref}

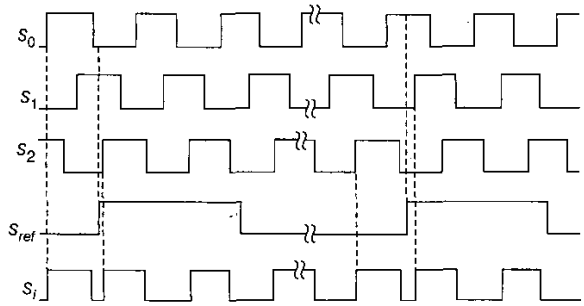

Fig. 3 *Phase-shift waveforms of proposed PSS*

Signals S_0, S_1 and S_2 are outputs of multiple phase shift unit. In this example, the unit produces three step phase shift. Each step is T/m (with $T=1/f$ and $m=3$). This phase difference between S_0 and S_1, or S_1 and S_2 is $T/3$. The phase detector acts at each rising edge of S_{ref}

The maximum phase error of the proposed PSS is $\phi_e = T/m$, where T is the cycle time of S. The phase error ϕ_e is inversely proportional to m. It should be noted that, if the required frequency of the output signal is low, the corresponding T will be long. In this case, to achieve a small ϕ_e, m has to be a large number, which implies a complex circuit structure. To keep m small and ϕ_e minimum at the same time when the required output frequency is low, a frequency division (FD) unit is added to the PSS as shown in Fig. 4. With this scheme, if the cycle time of the output signal is T_{out} and the coefficient of the frequency division is N, the cycle time of S will be $T = T_{out}/N$ and then $\phi_e = T_{out}/(mN)$, instead of $\phi_e = T/m$. Thus, the precision of the synchronisation is increased by N times compared to the case without frequency division.

The diagram in Fig. 4 is the basic scheme of the proposed open-loop phase locking (OLPL) approach to signal synchronisation. It should be noted that the synchronisation process in this scheme is completed within one cycle of the reference signal, whereas such a process can last many cycles in a conventional PLL for achieving a stabilised output.

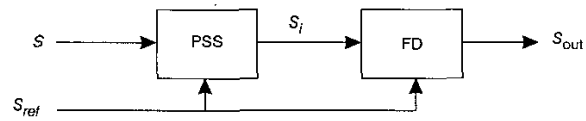

Fig. 4 *Basic scheme of proposed OLPL approach*

A frequency division unit $(1/N)$ is added so that cycle time of signal S or S_i is N times shorter than that of S_{out}

Design example and simulation results: To verify the effectiveness of the proposed scheme, a circuit of OLPL is designed and simulated with the transistor models of a 0.18 μm CMOS technology. A pulse signal with a frequency ranged 1–2 GHz is used as the input clock signal S. The multiple phase-shift unit is implemented using 11 buffers. The detector/multiplexer unit is composed of 12 registers, 11 XOR gates, and other logic gates. A 3-bit synchronous counter is used to perform a frequency division of $N=8$. The counter is reset by the rise (or fall) edges of the reference signal, and the output signal of the counter is thus synchronised with the reference signal.

The simulation results shown in Fig. 5 are obtained with the input clock frequency of 2.16 GHz, i.e. the cycle time of $T=463$ ps, and the output frequency of 2.16 GHz/8 = 270 MHz. The cycle time of the reference signal S_{ref} is $T_{ref} = KT - 3$ ps, where $K=12$. We have chosen this relatively small number of K instead of a large one in order that the phase adjustment can be observed within a short period of time. The curve shown in Fig. 5 illustrates that the phase error between the output and reference signals is 59.13 ps peak-to-peak or 14.26 ps rms.

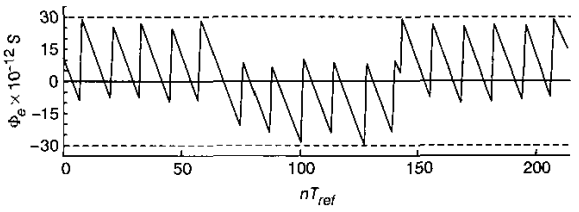

Fig. 5 *Simulation results, number of cycles of reference signal against the phase error*

Frequency of input clock S is 2.16 GHz and that of S_{out} is 270 MHz

Conclusion: A signal synchronisation scheme is proposed. This scheme uses a digital open-loop approach involving multiple phase shift and selection operations to achieve fast signal synchronisation. In particular, in case that the frequency of the output signal needs to be much higher than that of the reference signal, this open-loop scheme avoids the problem of phase error due to the weak feedback of a PLL circuit. The output signal of the circuits designed with this scheme can have a larger frequency range than those of PLL. A synchronisation circuit based on this scheme has been designed and simulated using the transistor models of a 0.18 μm technology. With a clock signal of 2.16 GHz, the output frequency of 270 MHz and a reference frequency about 22.5 MHz, the phase error is within 59.13/14.26 ps peak-to-peak/rms. It is also proved that the OLPL circuit can be implemented with simple structure and operates with high precision and high speed.

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Single-electron logic device with simple structure

T. Oya, T. Asai and Y. Amemiya

A logic gate device is described that can be used to develop single-electron LSIs. The device consists of five capacitors and two tunnelling junctions. It accepts two binary inputs and produces NAND or NOR logic output by making use of the voltage shift in its tunnelling threshold caused by the input signals. Computer simulation of a sample subsystem, or a full adder, consisting of the device demonstrated that it operates correctly.

Introduction: A promising area of research in nanoelectronics is the development of single-electron LSIs, which have larger scales of integration and lower levels of power dissipation than CMOS LSIs. To proceed toward this goal, we propose a single-electron logic gate that is simple in structure and therefore suitable for LSI applications.

The single-electron logic gate is an electronic circuit designed to manipulate logic functions by controlling the transport of individual electrons [1]. It consists of tunnelling junctions and capacitors. The smaller the number of these elements the better for LSI applications. Several types of single-electron gates have been proposed. The leading examples are Tucker's gate (consisting of 7 junctions and 9 capacitors for NAND logic) [2], the binary-decision-diagram gate (9 junctions and 7 capacitors for NAND) [3], and the capacitively coupled gate (16 junctions and 13 capacitors for NAND) [4]. In this Letter we propose a simple, compact single-electron gate consisting of only 2 junctions and 5 capacitors. The gate performs either NAND or NOR logic depending on bias voltage.

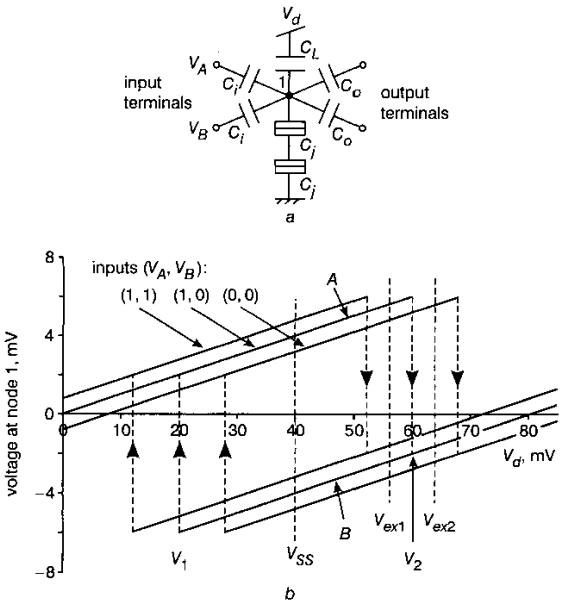

Fig. 1 *Gate device: circuit configuration and voltage at node 1 against V_d*
a Circuit configuration
b Voltage at node 1 against V_d
Inputs (V_A, V_B) and $C_j = 20$ aF and $C_L = C_i = C_o = 2$ aF. With these values, logical inputs 1 and 0 correspond to input voltages of 4 mV and −4 mV; e.g. inputs (1, 0) mean that one input is 4 mV and other is −4 mV.

Circuit structure: As shown in Fig. 1*a*, the gate device we propose consists of a single-electron trap (two identical tunnelling junctions, C_j, connected in series, a bias capacitor, C_L, and a bias voltage, V_d) with two input capacitors (C_i) and two output capacitors (C_o). The gate has an island node 1 that stores electrons. At the low temperatures at which the Coulomb-blockade effect occurs, the number of electrons, n, stored on node 1 changes with bias voltage V_d and takes a value such that the electrostatic energy in the circuit is locally minimised. The value of n is 0 at $V_d = 0$ and changes discretely with V_d because of electron tunnelling between node 1 and the ground through tunnelling junctions C_j. In this device, n changes from 0 to 1 when V_d is increased and returns from 1 to 0 when V_d is decreased; i.e. it is a hysteretic function of V_d (the single-electron trap is explained elsewhere [1]). The voltage at node 1 is therefore a hysteretic sawtooth function of V_d, as shown in Fig. 1*b*. If the input and output terminals are grounded, the node voltage increases along line A with increasing V_d; when V_d exceeds threshold V_2, the voltage changes from positive to negative and jumps to line B. The node voltage then decreases along line B with decreasing V_d, and jumps back to line A when V_d drops below threshold V_1. (We can use a multi-junction trap instead of the double-junction trap because a similar hysteretic curve can also be obtained with a multi-junction trap.)

The thresholds change with input voltages V_A and V_B. The hysteretic curve of the node voltage is shown in Fig. 1*b* for three possible input combinations. We use a positive voltage and a negative voltage of equal amplitude to represent the binary logic values, 1 and 0; therefore, input combination. (V_A, V_B) = (1, 0), for example, means that one input voltage is positive and the other is negative. The Figure shows that the thresholds become higher or lower based on the sum of the inputs. We make use of this characteristic for logic operations.

We operate the device as follows. We first ground the output terminals, apply the input voltages, and set V_d to 0. Then, for NAND operation, we increase V_d to exciting value V_{ex1} (see Fig. 1*b*) so that the gate is excited only when both inputs are logical 1, i.e. (V_A, V_B) = (1, 1). After exciting the gate, we decrease V_d to holding value V_{ss} and observe the voltage at node 1, the output voltage. The output voltage is negative (logical 0) if both inputs are 1 and positive (logical 1) if one or both inputs are 0. The output is transported to the following gates through output capacitors C_o. NOR operation can be similarly obtained by increasing V_d to higher exciting value V_{ex2}.

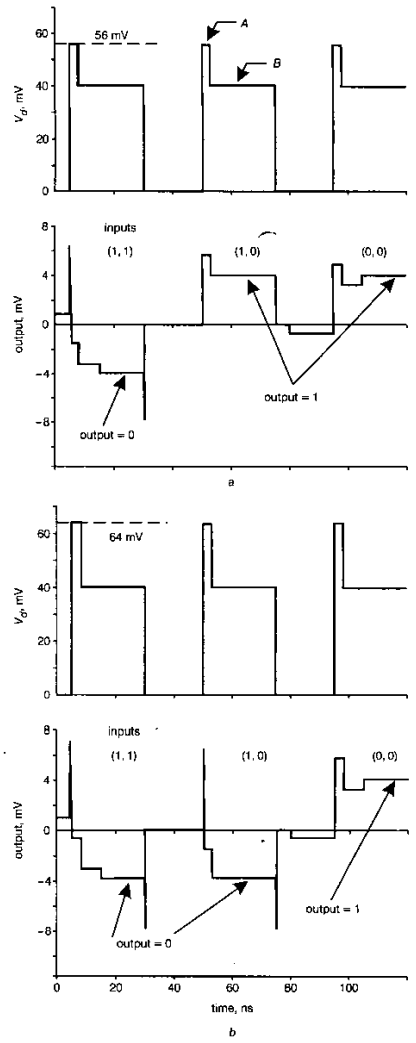

Fig. 2 *Simulated logic operations with same parameter settings as in Fig. 1, with tunnelling junction conductance = 1 μS and zero temperature*
a NAND logic gate operation with exciting voltage $V_d = 56$ mV
b NOR logic gate operation with $V_d = 64$ mV

Simulation results: We tested gate operation by computer simulation, using a Monte Carlo method. Fig. 2 shows the results for a sample set of parameter values. Bias V_d is a two-step clock pulse, shown in the upper plots in Fig. 2*a* (NAND operation) and *b* (NOR operation). First, V_d is set to exciting value A, and the gate determines its logic output according to the sum of the inputs. Next, V_d is set to holding value B, and the gate maintains its logic output. For NAND operation, the exciting value is V_{ex1}, shown in Fig. 1*b* (56 mV in this example);

for NOR operation, the exciting value is V_{ex2} (64 mV). The value of V_{ss} is 40 mV for both logic operations. The inputs (V_A, V_B) are applied synchronously with the bias clock. In Fig. 2*a* and *b*, the three sets of inputs (1, 1), (1, 0), and (0, 0) were applied in sequence. Depending on the input voltages, the voltage at node 1 changed from 0 V to positive (logic 1) or to negative (logic 0), as shown in the bottom plot in Figs. 2*a* and *b*.

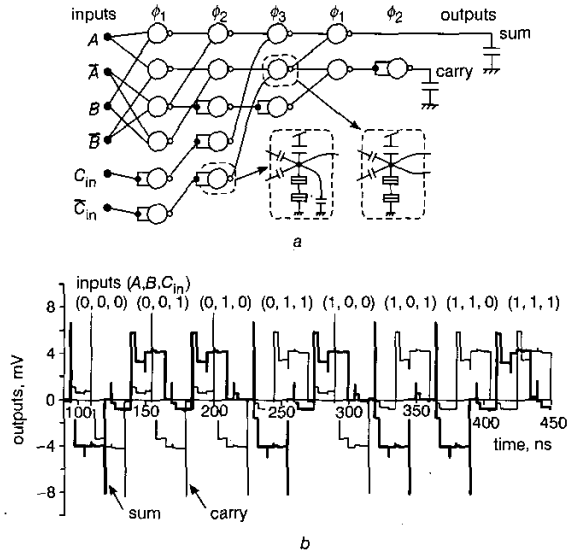

Fig. 3 *Full adder using NOR gates: circuit configuration and simulated add operation with same parameter settings as used in Fig. 2*

a Circuit configuration
b Simulated add operation

Subsystem design: Any logic function can be implemented by combining identical gates into a cascade configuration, with the output capacitor of one gate acting as the input capacitor of the following gate. Fig. 3*a* shows an example subsystem, a full adder, consisting of NOR gates. The gate device we proposed is bilateral, so we control the signal-flow direction by gating with a three-phase clock. We divide the gate circuits into three groups and excite each group in turn by one phase of the three clock signals, ϕ_1 to ϕ_3. The adder accepts three inputs, augend A, addend B, and carry input Cin (and their complements, $\bar{A}$, $\bar{B}$, and $\bar{C}_{in}$); it then produces the corresponding sum and carry outputs. The gates transfer the signal from the preceding stage to the following stage with appropriate clock timing. The inputs are taken in while clock ϕ_3 is high. The sum output is produced when ϕ_1 goes high again and is kept while ϕ_1 is in the holding period. The carry output is produced when ϕ_2 goes high again. The delay between the inputs and the sum output is four-thirds of a clock period, and the delay between the inputs and the carry output is five-thirds of a clock period. We demonstrated the add operation and confirmed correct operation for all input combinations, as shown in Fig. 3*b*. Multibit adders can be constructed by combining full adders in a cascade configuration. Based on these results, we can develop other subsystems and proceed towards the goal of single-electron LSIs.

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Principles and demonstration of multi-functional adaptive electromagnetic screen

F.C. Smith and R. Gupta

A bidirectional electromagnetic screen is proposed and demonstrated with properties that can be switched between high reflection, absorption and transmission over ~10 ns. The screen comprises frequency selective surfaces loaded with *pin* diodes, which under partial biasing conditions provide the loss mechanism for the absorption state of the screen.

Introduction: A multifunctional adaptive screen is a structure capable of exhibiting different electromagnetic (EM) screening properties, depending on the excitation state of the adaptive elements. There are potentially various useful screen characteristics; however, three exist with important engineering applications, namely high absorption, high reflection, and high transparency. The development of multifunctional screens with these characteristics at radio frequency (RF) and microwave frequencies can be based around the impedance properties of adaptive frequency selective surfaces (FSSs). In this Letter, we demonstrate, for the first time to our knowledge, the feasibility of creating a bidirectional EM screen that can be repeatedly switched between high reflection, high absorption and high transmission over a time interval of ~1–10 ns.

Theory: Fig. 1 shows a transmission line representation of a bidirectional air-filled composite screen. The term bidirectional refers here to the fact that all properties of the screen can be obtained either from port 1 or port 2. Using Fig. 1 and conventional transmission line theory, the EM properties of the screen which result in either high reflection, high absorption or high transmission can be determined as a function of the two impedances Z_1 and Z_2. These properties are listed in Table 1.

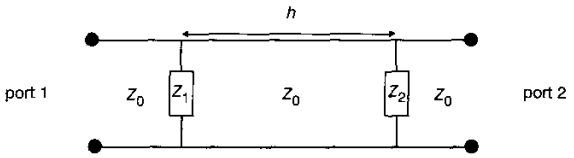

Fig. 1 *Transmission line analogue of bidirectional multifunctional screen*
Characteristic impedance $Z_0 = 377\ \Omega$ ($\simeq \sqrt{(\mu_0/\varepsilon_0)}$)

Table 1: Properties required of Z_1 and Z_2 for screen in Fig. 1 to be either transparent, opaque or absorbing at ports 1 and 2

Screen characteristic	Z_1 [Ω]	Z_2 [Ω]
Absorber (port 1), reflecting (port 2)	377	0
Absorber (port 2), reflecting (port 1)	0	377
Transparent	±∞	±∞
Reflecting (ports 1 and 2)	0	0

Data based on normal incidence and quarter wavelength spacing between Z_1 and Z_2 (for absorbing states)

The screen in Fig. 1 is assumed to be bidirectional: the adaptive impedances Z_1 and Z_2 are therefore realised from two identical FSSs. Inspection of Table 1 reveals that a large change in the complex impedance of the FSS is required to achieve the three characteristics. An array of closely spaced parallel wires exhibits a low inductive impedance [1]; if the wires are chopped to create an array or short dipoles, the impedance is high and capacitive. These two states can be