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Paper

A Highly Sensitive Thermosensing CMOS Circuit Based on Self-Biasing Circuit Technique

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A thermosensing CMOS circuit that changes its internal voltage steeply at a critical temperature was developed. The circuit is based on a self-biasing circuit technique and uses the temperature-sensitive characteristics of MOSFETs operating in the subthreshold region. To develop this sensor device, a method to analyze self-biasing circuits, which is different from a conventional one, was employed. This method is useful for understanding the self-biasing circuit operation. A temperature sensor device makes use of a MOSFET resistor's transition from a strong inversion to a weak-inversion or subthreshold operation. The temperature at which the transition occurs can be set to a desired value by adjusting the parameters of MOSFETs in the circuit. The sensor LSI can be made using a standard CMOS process and can be used as over-temperature and over-current protectors for LSI circuits. © 2009 Institute of Electrical Engineers of Japan. Published by John Wiley & Sons, Inc.

Keywords: MOSFET, subthreshold operation, self-biasing circuit, temperature switch sensor

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1. Introduction

A promising area of research and development in solid-state microelectronics is exploring ultralow-power analog LSIs that can be used for new applications. To further advance such LSIs, we have developed sensor LSIs that consist of subthreshold MOSFETs, or MOSFETs operating in a weak-inversion region [1–4]. We herein propose a temperature switch sensor LSI based on a self-biasing circuit technique. A self-biasing circuit can be used as a temperature sensor by making use of the temperature characteristics of its current and voltage.

Safe and stable operation of electrical products is one of the most important requirements that must be addressed during the design phases. To ensure the stable operation of electrical products, thermally sensitive resistor sensors, or thermistors, are widely used to monitor the temperature of various products and detect any undesirable, or dangerous increases in temperature [5]. A critical temperature resistor (CTR) thermistor is widely used for this purpose because it exhibits a sharp change in resistance at a threshold temperature and is suitable for sensing overheating [6]. Therefore, CTR thermistors are often used in overheating detectors, over-current protectors, and temperature-compensation devices. The sharp change in their resistance is caused by a phase transition of its conductive ceramics. However, because a CTR thermistor is made of ceramics, they are incompatible with silicon LSIs. In addition, it is difficult to set a threshold temperature over a wide range. These problems, however, can be solved by developing a temperature detection system consisting of monolithic LSI circuits. Although such a system can be constructed by combining a conventional temperature sensor (e.g. diode, or bipolar devices) with an AD converter and a microprocessor, the system requires several integrated circuits and is, therefore, impractical due to its high-cost and high-power consumption.

A temperature sensor LSI consisting of only MOSFETs was proposed in the literature [7,8]. The circuit is a highly sensitive thermosensing CMOS circuit by using the temperature characteristics of MOSFETs operating in a subthreshold region. This circuit -which we call a critical temperature switch (CTS) circuit- is based on a self-biasing circuit technique and shows a sharp transition of its internal voltage, similar to that of CTR thermistors. However, operation principle of the circuit was not clear in the literature, and the critical temperature for switching could not be estimated theoretically. In this paper, a method to analyze a self-biasing circuit, which is different from a conventional one, is employed to solve these problems. The analysis method is useful to understand the mechanisms of the temperature switching function of the CTS circuit. Theoretical critical temperature for switching is also established in this paper. This device is free from the limitations inevitable in CTR thermistors. The paper is organized as follows: the method to analyze

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self-biasing circuits is described in Section 2, a CTS core circuit and entire circuit configuration are presented in Sections 3 and 4, respectively, experimental results are shown in Section 5, and we conclude the paper in Section 6.

2. Self-Biasing Circuit

Self-biasing circuits are widely used to generate a reference voltage and current in LSIs because of their simple and stable operation [6,7]. Because the reference current and voltage of the circuit are determined by device parameters, these references are temperature sensitive and, therefore, can be used as a temperature sensor signal.

In this section, we outline the method to analyze a self-biasing circuit and highlight the differences from a conventional one. The method we employed enables better understanding of the physical operation principle of a self-biasing circuit. First, a conventional analysis method is described, and then the method employed in this work is presented, focusing on a beta multiplier reference (BMR) circuit as a typical example of self-biasing circuit [6].

Figure 1(a) shows a BMR circuit. The circuit consists of NMOS transistors (M_1–M_2), a resistor (R), and a PMOS current mirror (M_3–M_4). We set the aspect ratios of the transistors such that $K_2/K_1 = K > 1$ and $K_3 = K_4$, where K_i $(i = 1 - 4)$ is the aspect ratio of transistors M_i.

2.1. Conventional analysis method

The circuit in a conventional analysis method is divided into two subcircuits as follows:

(1) NMOS transistors and resistor subcircuit; and
(2) PMOS current mirror subcircuit.

An operating point of the circuit can be determined graphically by using current transfer characteristics of the two subcircuits. This analysis is illustrated in Fig. 1(b). The transfer characteristics of (1) the NMOS transistors and resistor subcircuit and (2) the PMOS current mirror subcircuit can be as $I_2 = f(I_1)$, where f is an arbitrary function, and $I_2 = I_1$, respectively. The operating point of the circuit must satisfy both equations and hence is determined from the point at which the two lines intersect. Therefore, the operating point can be given by $I_1 = f(I_1)$.

This analysis method provides the circuit with two possible operating points, A and zero, at the intersections of the transfer characteristics, as shown in Fig. 1(b). Point A is a desired operating point, and zero is an undesired operating point. To prevent the circuit from remaining at zero, a separate start-up circuit is usually required [6].

In this way, the method can be used for determining the operating point. However, the method is suitable for static operating analysis but is unsuitable to understand the dynamic behavior of the circuit before settling into the operating point and the temperature characteristics of the circuit. Next, we described a method to analyze the self-biasing circuit that is useful for understanding its dynamic operation and the temperature characteristics of the self-biasing circuit.

2.2. Analysis method

The BMR circuit in the analysis method we employed is divided into three subcircuits. Figure 2(a) shows these subcircuits as follows:

(1) diode-connected transistor subcircuit (M_1);
(2) source-degenerated transistor subcircuit (M_2–R); and
(3) PMOS current mirror (CM) subcircuit (M_3–M_4).

These subcircuits operate as a current-to-voltage ($I_1 - V_1$) conversion subcircuit, a voltage-to-current ($V_1 - I_2$) conversion subcircuit, and a current-to-current ($I_2 = I_1$) conversion subcircuit, respectively. The BMR circuit can be considered as a feedback connection of these subcircuits, as shown in Fig. 2(b). The $I_1 - V_1$ subcircuit generates a voltage, V_1, from current I_1 and applies the voltage to the $V_1 - I_2$ subcircuit. The $V_1 - I_2$ subcircuit generates current I_2. The CM subcircuit is used to make the current of I_2 equal the current of I_1.

The operating point of the BMR circuit can be determined from the transfer characteristics of these subcircuits. Figure 3(a)

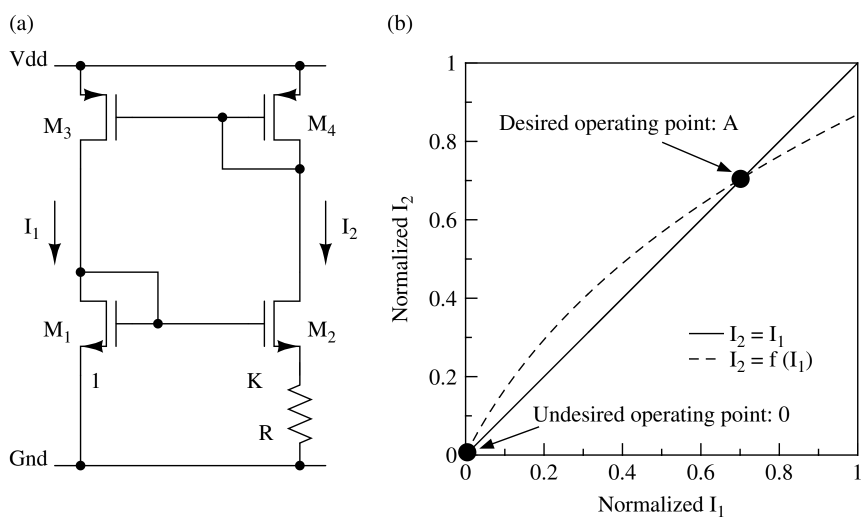

Fig. 1 (a) Beta multiplier reference (BMR) circuit, and (b) its conventional analysis method

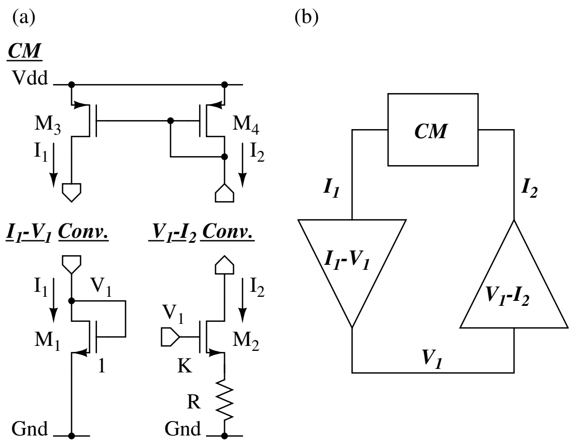

Fig. 2 (a) Three subcircuits for BMR circuit analysis, and (b) circuit's feedback connection

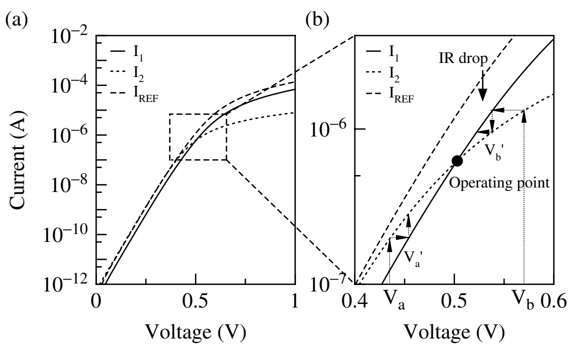

Fig. 3 (a) Transfer curves of BMR circuit, and (b) its partial enlarged view

and (b) shows the transfer characteristics of these subcircuits and a partial enlarged view. Current I_{REF} that is generated by a transistor, which is the same transistor size as transistor M_2 without resistor, is also plotted in the figure for comparison. In the lower current level region, because the voltage drop (IR drop) in resistor R can be ignored, current I_2 is larger than current I_1 by a current gain factor of K. Therefore, current I_2 is almost the same level as that of current I_{REF}. Whereas, in a larger current level region, current I_2 begins to decrease as compared to current I_{REF} because the voltage drop in resistor cannot be ignored, and the effective gate-source voltage of M_2 then starts to decrease. A further increase in current makes current I_2 smaller than current I_1. This decrease in current I_2 creates an intersection point with current I_1. Because the CM subcircuit makes the current of I_2 equal the current of I_1, this intersection point becomes an operating point of the circuit.

From the analysis, details of the circuit operation can be understood as follows. If the circuit starts up at a voltage, V_i ($i = a$ or b), as shown in Fig. 3(b), current I_2 is determined from the transfer curve of I_2. The generated current produces a new voltage of $V_i^{'}$ from the transfer curve of I_1. The circuit repeats the above current and voltage generation process, and then finally operates at the operating point.

The analysis also shows that the zero point of the circuit is not the operating point. As shown in Fig. 3(b), current I_2 in the low current level region is larger than current I_1 by a current gain factor of K. The feedback in the circuit in this region is positive, and the circuit will drive itself out of this state. Therefore, the circuit has only one operating point. However, this does not mean that a start-up circuit is unnecessary for the circuit implementation. The circuit could not operate quickly in the low-current level region due to its low driving current. Therefore, it takes time to settle in the operating point. A start-up circuit is required because the circuit is required to operate immediately once the power is turned on.

3. Critical Temperature Switch Circuit

By using temperature characteristics of the self-biasing circuit, a CTS circuit can be constructed. At low temperatures, the circuit has two possible operating points. At temperatures greater than the critical temperature, on the other hand, the circuit loses one of its operating points because each current transfer curve has different temperature characteristics. The CTS circuit utilizes this loss of operating point as a switching operation.

3.1. Circuit configuration and its operation

Figure 4(a) shows a proposed CTS circuit. This circuit is based on a BMR circuit and uses a MOSFET resistor M_1 instead of an ordinary resistor R. To generate higher gate voltages for M_1, we adapted a cascode configuration of nMOSFETs. The aspect ratios of transistors were set such that $K_3 > K_2$, $K_2 = K_4 = K_5$, and $K_6 = K_7$. All MOSFETs in the circuit were operated in a subthreshold region, except for M_1. The current mirror circuit, consisting of M_6 and M_7, makes the current of I_1 equal the current I_2. The circuit shows a switching operation such that node voltage V_b changes drastically from a higher value to a lower one at a critical temperature (T_{C}). The detailed operation is discussed below.

The circuit operation can be analyzed using the transfer curves for the left (M_2–M_4) and right (M_1–M_3–M_5) branches, as shown in Fig. 4(b). Current I_1, in the left branch, flows through transistors M_2 and M_4 and generates voltage V_b, and current I_2, in the right branch, is controlled by voltage V_b. Because, I_1 and I_2 equal each other because of the PMOS current mirror, we can find the operating point of the circuit by observing the point at which the two transfer curves, $I_1 - V_b$ and $V_b - I_2$ curves, of the circuit intersect. The results are

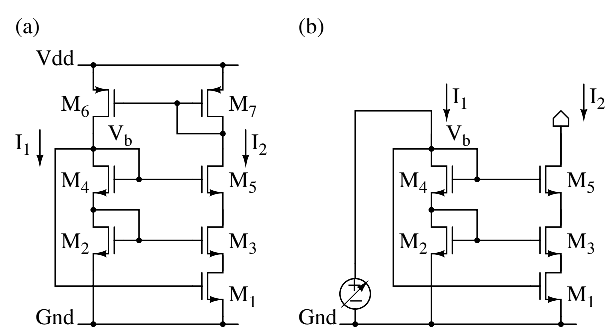

Fig. 4 Critical temperature switch circuit with self-biasing circuit technique

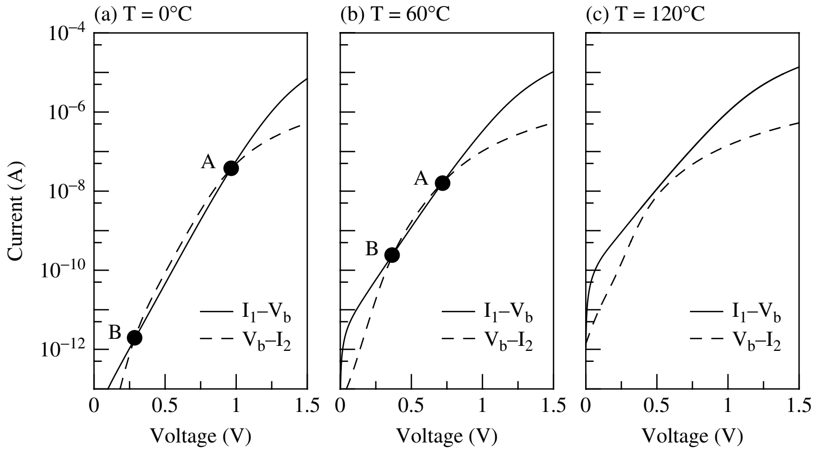

Fig. 5 Transfer characteristics of CTS circuit at three different temperatures. (a) $T = 0^\circ$C, (b) $T = 60^\circ$C, and (c) $T = 120^\circ$C

illustrated in Fig. 5(a)–and (c) in which I_1 and I_2 are plotted as a function of voltage V_b at different temperatures. At low temperatures, the two curves intersect at points A and B, as shown in Fig. 5(a). Point A is a stable operating point, while point B is an unstable point. Point B can be an operating point of the circuit in this analysis. However, if there will be a small noise or a disturbance, the circuit operating at point B will change the internal voltage and current to higher or lower values than that of point B. After losing the operating point from point B, the circuit cannot operate at the same operating point of B. This is because the generation process of internal current and voltage in the circuit changes at the boundary point of B, due to the two curves of $I_1 - V_b$ and $V_b - I_2$ in Fig. 5. This phenomenon can be described as follows: Once the voltage of V_b in the circuit becomes higher than the voltage of point B, the voltage generates a larger current than that of point B from the transfer curve of $V_b - I_2$. The generated current also generates a larger voltage than that of point B from the curve of $I_1 - V_b$. The circuit repeats the above process, and settles into the stable point A. In contrast, once the voltage of V_b is lower than B, the voltage generates a smaller current than point B from the curve of $V_b - I_2$. The generated current also generates a smaller voltage than point B from the curve of $I_1 - V_b$. The circuit repeats the above process, and then settles into the zero. Therefore, the circuit changes its settling points at the boundary point of B. The circuit has two possible operating points −one is point A, and the other is zero (therefore, $I_1 = I_2 = 0$, and $V_b = 0$) −based on its initial condition.

As the temperature increases, the intersection points of A and B approach each other because the temperature characteristics of the two transfer curves are different from each other (Fig. 5(b)). At the critical (or threshold) temperature, the intersections of A and B overlap each other. At temperatures that exceed critical temperature T_C, the two curves do not intersect as shown in Fig. 5(c). Therefore, the circuit operates at a zero point ($I_1 = I_2 = 0$, and $V_b = 0$). The CTS circuit shows a switching operation at a critical temperature because the operating point of the circuit transits from A to zero.

3.2. Critical temperature The critical temperature can be calculated theoretically. The CTS circuit we developed uses the characteristic of a MOSFET operating in a subthreshold region. The subthreshold drain current, I_D, through a MOSFET is an exponential function of gate-source voltage V_{GS} and is given by

$$I_D = I_0 \exp\left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right) \tag{1}$$

where I_0 is a process-dependent parameter, V_T $(= k_B T/q)$ is the thermal voltage, k_B is the Boltzmann constant, T is the absolute temperature, q is the elementary charge, η is the subthreshold slope factor, and V_{TH} is the threshold voltage of the MOSFET [8–10].

In the CTS circuit shown in Fig. 4(a), gate-source voltage V_{GS2} in transistor M_2 must equal the sum of gate-source voltage V_{GS3} in M_3 and drain-source voltage V_D in M_1,

$$V_{GS2} = V_{GS3} + V_D. \tag{2}$$

Because the current through transistor M_2 and current through transistor M_3 are equal, (2) can be rewritten as

$$V_D = \eta V_T \ln(K), \tag{3}$$

where K is the ratio between aspect ratios K_2 and K_3 in M_2 and M_3: that is, $K = K_3/K_2$. Because transistors M_2 and M_4 are connected in a cascode configuration, gate voltage V_b of M_1 can be made higher than the threshold voltage of M_1. At this condition, transistor M_1 operates in a strong inversion and triode region. Current I in transistor M_1 is expressed as

$$I = \beta_1 \left((V_b - V_{TH}) V_D - \frac{1}{2} V_D^2\right), \tag{4}$$

where β_1 is the current gain factor of M_1. The last term in (4) can be ignored because transistor M_1 operates in deep triode region. Therefore, from (1), (3) and (4), current I and gate voltage V_b are given by

$$I = \beta_1 (V_b - V_{TH}) \eta V_T \ln(K), \tag{5}$$

$$V_b = 2V_{TH} + 2\eta V_T \ln\left(\frac{I}{I_0}\right). \tag{6}$$

From these equations, current I and voltage V_b in the circuit are determined by each other.

The temperature dependence of threshold voltage V_{TH} and mobility μ are expressed as

$$V_{TH} = V_{TH0} - \kappa T \tag{7}$$

$$\mu = \mu_0 \left(\frac{T}{T_0}\right)^{-m} \tag{8}$$

where V_{TH0} is the threshold voltage in an absolute zero temperature, κ is the temperature coefficient of the threshold voltage, μ_0 is the mobility at temperature T_0, and m is the temperature exponent factor of mobility [15]. From (5)–(8), we find that temperature coefficient (TC_I) of the current is given by

$$\begin{aligned} TC_I &= \frac{1}{I}\frac{\mathrm{d}I}{\mathrm{d}T} \\ &= \frac{1}{\beta_1}\frac{\mathrm{d}\beta_1}{\mathrm{d}T} + \frac{1}{V_b - V_{TH}}\frac{\mathrm{d}\,(V_b - V_{TH})}{\mathrm{d}T} + \frac{1}{V_T}\frac{\mathrm{d}V_T}{\mathrm{d}T} \\ &= \frac{1-m}{T} + \frac{1}{V_b - V_{TH}} \\ &\quad \times \left(-\kappa + 2\eta V_T \left\{\frac{1}{T}\ln\left(\frac{I}{I_0}\right) + \frac{1}{I}\frac{\mathrm{d}I}{\mathrm{d}T} - \frac{1}{I_0}\frac{\mathrm{d}I_0}{\mathrm{d}T}\right\}\right) \end{aligned} \tag{9}$$

Equation (9) can be rewritten,

$$\begin{aligned} TC_I &= \frac{\frac{1-m}{T} - \frac{\kappa - \frac{2\eta V_T}{T}\left(\ln\left(\frac{I}{I_0}\right) - (2-m)\right)}{V_b - V_{TH}}}{1 - \frac{2\eta V_T}{V_b - V_{TH}}} \\ &= \frac{V_A}{T\,(V_b - V_{TH} - 2\eta V_T)} \\ V_A &= (1-m)(V_b - V_{TH}) \\ &\quad - \kappa T + 2\eta V_T \left(\ln\left(\frac{I}{I_0}\right) - (2-m)\right) \end{aligned} \tag{10}$$

For a standard CMOS process, the numerator and denominator in (10) are a negative and a positive, respectively. Therefore, current I decreases with temperature. The denominator in (10) also decreases with temperature. At the critical temperature, the denominator becomes zero and the slope of the current with temperature decreases toward negative infinity. This phenomenon produces a sharp change in current I and voltage V_b and a switching operation of the circuit. From (10), the threshold condition of the circuit is given by

$$V_b - V_{TH} - 2\eta V_T = 0 \tag{11}$$

From this condition, the critical temperature for the sharp change can be given by

$$T_C = \frac{V_{TH0}}{2\eta \frac{k_B}{q}\left\{1 - \ln\left(2M\frac{\eta^2}{\eta - 1}\ln(K)\right)\right\}} \tag{12}$$

where M is the ratio of aspect ratio in M_1 and M_2 ($M = K_1/K_2$). The critical temperature can be controlled by changing the circuit parameters.

3.3. Simulation results

Operation of the CTS circuit in Fig. 4(a) was confirmed by using a SPICE simulation with a set of 0.35 μm CMOS parameters and an 1.5 V power supply. Figure 6 shows the change in V_b as a function of increasing and decreasing temperature with three different parameters K. The ratio of the aspect ratios of M_2 and M_3 was set to 1.2–2.0 as a parameter. The aspect ratio of M_1 was set to 0.05. Voltage V_b decreases as the temperature increases, and then drops suddenly at the critical temperature. Changing parameter K can set the critical temperature. When the circuit operates at temperature higher than the critical temperature, voltage V_b drops down to a lower voltage. However, voltage V_b, once dropped, does not return to a high voltage even if the temperature decreases below the critical temperature again because the V_b is smaller than unstable point B. This characteristic of the CTS circuit is also shown in Fig. 6. The unstable operating point creates two possible operating points for voltage V_b below a critical temperature. Figure 7 shows critical temperature as a function of K, with the channel width of M_1 as a parameter. Theoretical critical temperatures calculated from (12) are also plotted. These results show that the critical temperature can be set over a wide range from 20 to 100°C by simply changing the circuit parameters.

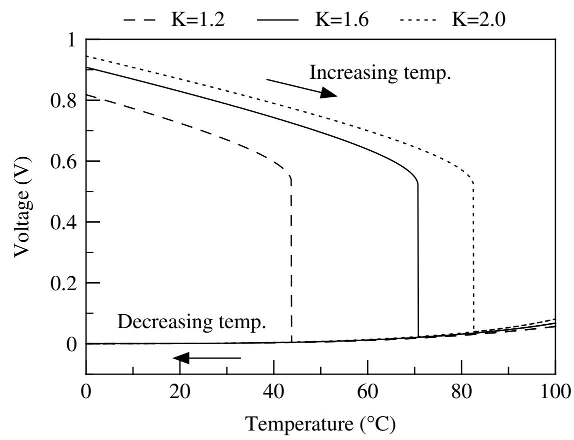

Fig. 6 Simulated results of voltage V_b with K as parameter. Critical temperature T_C can be set by changing K. Different behaviors of V_b with decreasing temperature after increasing temperature are also plotted. CTS circuit has two possible operating points at temperatures below critical temperature

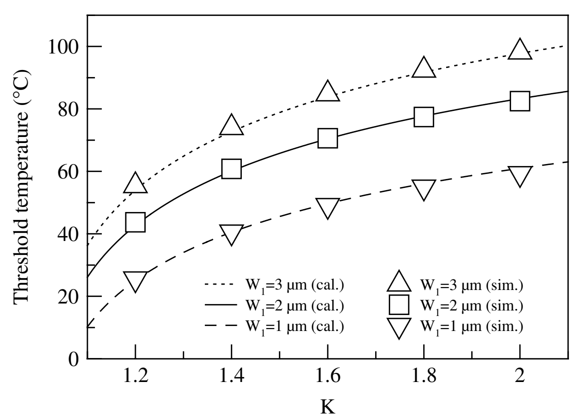

Fig. 7 Theoretical and simulated results of critical temperature as a function of K with the channel width as parameter. Critical temperature can be set over a wide range from 20 to 100°C

Because the temperature characteristics of the circuit are determined by transistors M_1, M_2, M_3 and M_4 as discussed previously, the temperature characteristics of the other transistors have an insignificant effect on the circuit operation. However, the variation of the threshold voltage have significant impact on the circuit operation, especially for critical temperature T_C as shown in (12). Because (12) contains parameter of V_{TH0}, which is related to the threshold voltage of a MOSFET, critical temperature T_C will change directly with the threshold voltage variation. The parameter V_{TH0} in (12) originates from the threshold voltage of transistor M_1. Therefore, if the gate bias voltage is generated so that the voltage monitors the threshold voltage variation, the accuracy in (12) can be improved. We are now developing such system by using the reference voltage circuit which monitors the threshold voltage of a MOSFET in an LSI chip [14].

4. Circuit Configuration

The CTS circuit performs a switching operation by monitoring voltage V_b, which changes from a higher (strong-inversion bias condition for M_1) to a lower voltage (subthreshold bias condition for M_1) with temperature. However, the CTS circuit shows different behaviors when it operates with decreasing temperature after increasing temperature as shown in Fig. 6. This phenomenon is due to the unstable operating point B shown in Fig. 5. When the circuit operates at temperature higher than critical temperature, voltage V_b drops down to a lower voltage. However, voltage V_b, once dropped, does not return to a high voltage even if temperature decreases again below the critical temperature because V_b is smaller than the unstable point B.

To cancel the effect of the unstable operating point B, we used a subcircuit to reset voltage V_b periodically to a higher voltage (higher than the unstable operating point voltage). This resetting enabled transistor M_1 to be returned to a strong-inversion region at temperatures less than the critical temperature. Figure 8 shows the total system including the resetting subcircuit. The subcircuit consists of a ring oscillator, a frequency divider, and a resetting transistor, M_{RST}, connected to the CTS circuit. We used a nanoampere-current source [11], and by this current the ring oscillator is driven and produces a square wave and produces a resetting pulse (RST) and sampling pulse (SMP). Transistor M_{RST} accepts the resetting pulse and periodically sets V_b to a high voltage, and as a result, sets M_1 to a strong-inversion region periodically. Voltage V_b is sampled periodically with an SMP and is retrieved as an output voltage, V_{OUT}, on the capacitance, C_C, and then it is output as a digital signal (D_{OUT}) after through a current-source inverter and a current-limited inverter.

We confirmed the resetting operation by using a SPICE simulation. A CTS circuit with a critical temperature of 77.6°C was used, and temperature was assumed to be 75 and 80°C. At temperatures lower than the critical temperature ($T = 7$°C), the CTS circuit should produce a high voltage output. However, because of the effect of the unstable operating point, the CTS circuit produced a low-voltage output when the initial output was low. This was corrected by the resetting operation. The results are shown in Fig. 9(a). The initial voltage of V_b was set at 0 V; therefore, the initial output was 0, an incorrect output for a temperature (T =75°C) lower than the CTS threshold condition (T_C =77.6°C). After the first resetting pulse was applied to the CTS circuit, voltage V_b was set at a voltage greater than the unstable operating point voltage. As a results, voltage V_b operated at the correct voltage output and, after that, maintained its correct output. At temperatures greater than the critical temperature ($T = 80$°C), the CTS circuit should produce a low-voltage output. The results are shown in Fig. 9(b). The initial voltage of V_b was also set to 0 V. With a resetting pulse, voltage V_b was set to higher voltage but, because the circuit no longer had any operating points at this temperature, decreased to a lower voltage. The sampling pulse correctly retrieved the low voltage of V_b and output in D_{OUT} low digital signal, correctly.

5. Measurement Results

To verify the circuit operation, we performed a measurement of the CTS core circuit shown in Fig. 4(a) by using a discrete MOSFETs: nMOSFET (2SK1398) and pMOSFET (2SJ184) [12]. Figure 10 shows measurement setup including a DC bias generator, thermostatic chamber, and its measurement board. In the measurement, transistor widths for M_2–M_7 were

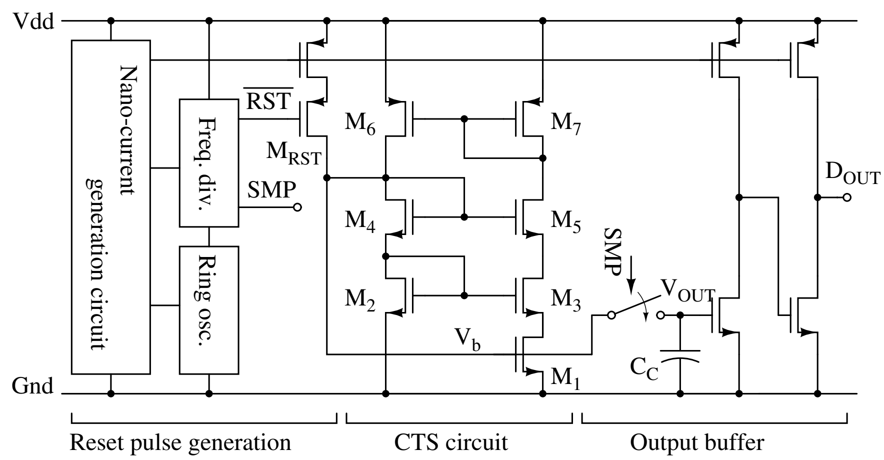

Fig. 8 CTS circuit with resetting subcircuit

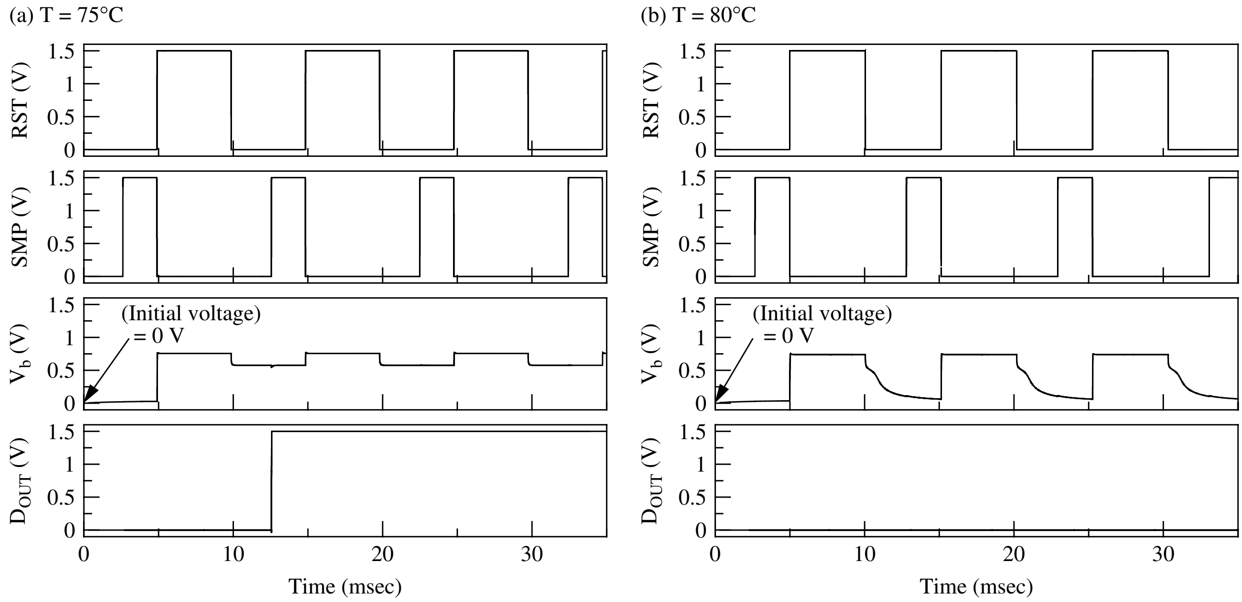

Fig. 9 Reset operation of circuit. Initial voltage of V_b was set to 0 V. Simulated at temperature of (a) 75°C (critical temperature of CTS circuit was 77.6°C), and (b) 80°C

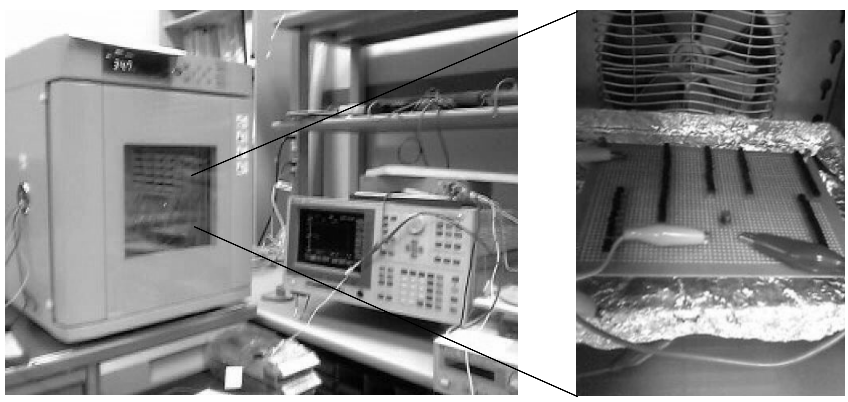

Fig. 10 Left: measurement setup. Right: measurement board

controlled by connecting transistors in parallel and the ratio of $K = (K_3/K_2)$ was set to 2. Power supply voltage was set at 5 V. The temperature was increased with time at the rate of 1.1 (°C/min.). Figure 11 shows the results of the output voltage of V_b in the temperature range of 20–120°C. To avoid the effect of unstable operating point B, the output voltage of V_b was initialized to the higher voltage of supply voltage at the beginning. The output voltage decreased as the temperature increases, and then dropped steeply at the critical temperature about 90°C. The CTS circuit operation was confirmed by experimental results using a discrete MOSFETs.

In this measurement, we showed and confirmed the CTS circuit operation, which was discussed in the previous sections, by using a commercial discrete MOSFETs. However, we are now planning to fabricate a monolithic LSI chip including a CTS core circuit and a resetting circuit by using a standard CMOS technology.

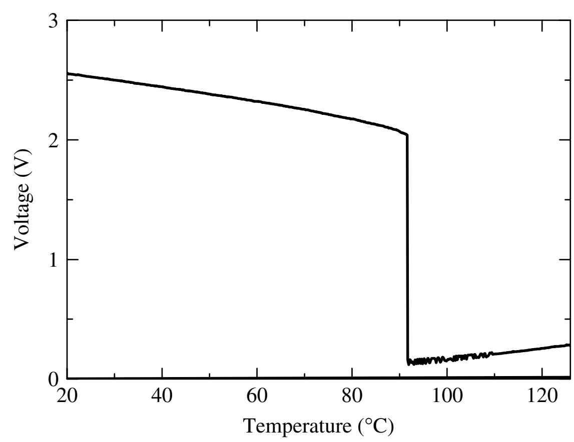

Fig. 11 Measurement results of the output voltage of V_b in the temperature range of 20–120 °C

6. Conclusion

A thermosensing CMOS circuit–CTS circuit–consisting of subthreshold MOSFET circuit was developed capable of changing its internal voltage steeply at a critical temperature. The circuit is based on a self-biasing circuit technique and uses the temperature-sensitive characteristics of MOSFETs operating in the subthreshold region. To develop a sensor LSI, we employed a method to analyze self-biasing circuits that is different from a conventional one. The temperature for the transition can be set to a desired value by adjusting the parameters of MOSFETs in a circuit. The sensor LSI can be made using a standard CMOS process and be used as over-temperature and over-current protectors for LSI circuits.

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References

(1) Hirose T, Yoshimura R, Ido T, Matsuoka T, Taniguchi K. Watch-dog circuit for quality guarantee with subthreshold MOSFET current. *IEICE Transactions on Electronics* 2004; **E87-C(11)**:1910–1914.

(2) Hirose T, Matsuoka T, Taniguchi K, Asai T, Amemiya Y. Ultralow-power current reference circuit with low temperature dependence. *IEICE Transactions on Electronics* 2005; **E88-C(6)**:1142–1147.

(3) Ueno K, Hirose T, Asai T, Amemiya Y. A CMOS watchdog sensor for certifying the quality of various perishables with a wider activation energy. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences* 2006; **E89-A(4)**:902–907.

(4) Hirose T, Asai T, Amemiya Y. Power-supply circuits for ultralow-power subthreshold MOS-LSIs. *IEICE Electron. Express* 2006; **3(22)**:464–468.

(5) Gopel W, Hesse J, Zermel JN. Sensors Volue 4: Thermal Sensors - A Comprehensive Survey-. Wiley-VCH: Weinheim; 1990, 235–239.

(6) Futaki H. A new type semiconductor (critical temperature resistor). *Japan Journal of Applied Physiscs* 1965; **4(1)**:28–41.

(7) Hagiwara A, Hirose T, Asai T, Amemiya Y. Critical temperature switch consisting of subthreshold CMOS circuits. *IEICE Transactions on Electronics* 2006; **J89-C(10)**:654–656.

(8) Hagiwara A, Hirose, T Asai T, Amemiya Y. Critical temperature switch: a highly sensitive thermosensing device consisting of subthreshold MOSFET circuits. *Proceedings of the International Symposium on Intelligent Signal Processing and Communication Systems*, 2006, 111–114.

(9) Baker RJ, Li HW, Boyce DE. *CMOS Circuit Design, Layout, and Simulation*. IEEE Press: New York; 1998.

(10) Gray PR, Meyer RG. *Analysis and Design of Analog integrated circuits*. John Wiley & Sons, Inc.: New York; 1993.

(11) Liu W, Jin X, Chen J, Jeng MC, Liu Z, Cheng Y, Chen K, Chan M, Hui K, Huang J, Tu R, Ko PK, Hu C. *BSIM3v3.2.2 MOSFET Model - User's Mannual*. University of California: Berkeley; 1999.

(12) Cheng Y, Jeng MC, Liu Z, Huang J, Chan M, Chen K, Ko PK, Hu C. A physical and scalable I-V model in BSIM 3v3 for analog/digital circuit simulation. *IEEE Transactions on Electronic Devices* 1997; **44(2)**:277–287.

(13) Cheng Y, Chen K, Imai K, Hu C. A unified MOSFET channel charge model for device modeling in circuit simulation. *IEEE Transactions on Computer-Aided Design* 1998; **17(8)**: 641–644.

(14) Ueno K, Hirose T, Asai T, Amemiya Y. CMOS voltage reference based on the threshold voltage of a MOSFET. Extended Abstract of the 2007. International Conference on Solid State Devices and Materials, 2007, 486–487.

(15) Taur, Y, Ning TH. *Fundamentals of Modern VLSI Devices*. Cambridge University Press: New York; 1998.

(16) Oguey HJ, Aebischer D. CMOS current reference without resistance. *IEEE Journal of Solid-State Circuits* 1997; **32(7)**:1132–1135.

(17) http://www.necel.com/discrete/en/index.html.

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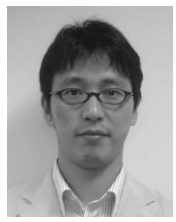

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