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PAPER Special Section on Analog Circuit Techniques and Related Topics

A CMOS IF Variable Gain Amplifier with Exponential Gain Control

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SUMMARY An intermediate frequency (IF) variable gain amplifier (VGA) with exponential gain control for a radio receiver is fabricated in 0.25-μm CMOS technology. The techniques to improve the bandwidth and to reduce temperature dependence of gain are described. The complete VGA is composed of two stages of linearized transconductance VGA and three stages of fixed gain amplifier (FGA). The complete VGA provides a continuous 10 dB to 76.5 dB gain control range, an IIP3 of −11.5 dBm and an NF of 15 dB at 40 MHz.

key words: *variable gain amplifier, VGA, linearized transconductance, linear-in-dB characteristics, exponential gain control, CMOS*

1. Introduction

A variable gain amplifier (VGA) is an indispensable component for intermediate frequency (IF) stage in radio receiver systems. VGA provides a signal whose amplitude is suitable for analog-to-digital converter (ADC) at back-end analog circuits in a receiver.

This paper describes a CMOS linear-in-dB VGA for an IF receiver with bandwidth of 40 MHz. The VGA using linear-in-dB characteristics is effective for wireless communication systems due to its wide gain range and low-power operation. There are two types of CMOS linear-in-dB VGAs. One is a VGA using MOSFETs in square-law as well as exponential-law regions [1], [2]. The other is a VGA using MOSFETs in only square-law region, which approximates an exponential function [3]–[5]. There is difficulty in correctly incorporating the conventional piece-wise modeling of MOSFETs in different two operation regions, required for design of the former [6]. Meanwhile, the techniques described in [3]–[5] apply exponential function of $\exp(x)$, $\exp(2x)$, or $\exp(4x)$ to linear-in-dB characteristics, respectively. The VGA using $\exp(2x)$ [4] is suitable for our target where it has wide gain range and moderate gain variation with control voltage. This type of VGA which linearizes transconductance with DC offset voltage has not been developed for wireless communication. Although it has over 30 dB wide gain range, much wider range of gain is demanded for the application. Multi-stage connection of the VGA is one of the solutions to extend gain range but cascade connection degrades frequency characteristics. In this paper, we explain the method to improve VGA bandwidth without gain range trade-off and to reduce temperature dependence of gain. A fixed gain amplifier (FGA) is also designed to enforce overall gain. The complete VGA consists of two-stage modified linearized transconductance VGA, three-stage FGA, and a buffer.

We first describe the principle of the linearized transconductance VGA, followed by the circuit configurations for bandwidth improvement and small temperature dependence of gain.

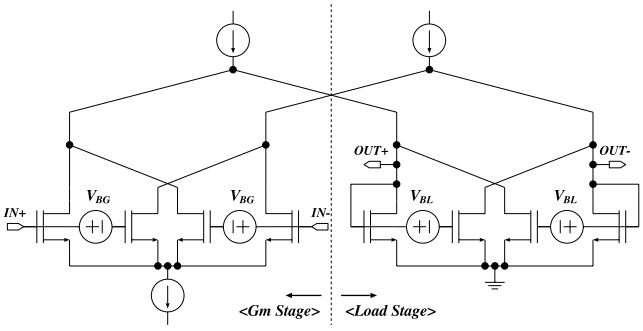

Fig. 1 Basic conceptual schematic of the VGA.

2. Circuit Principle and Design

The linearized transconductance VGA consists of four same size MOSFETs and two DC offset voltage sources in both G_m and load stages, as shown in Fig. 1. Gain of the VGA is the ratio of the transconductance of G_m stage to that of load stage. Each transconductance varies linearly with DC offset voltage, V_{BG} or V_{BL}. Therefore, gain of the VGA, G_{VGA}, is expressed by

$$G_{VGA} = -K\frac{V_{BG}}{V_{BL}}, \tag{1}$$

where K is the size ratio of transistors in G_m stage to that in load stage. By making these DC offset voltages vary linearly in opposite direction, the exponential gain control is achieved [4].

Figure 2 shows the designed VGA, FGA and gain control circuit. In the fully-differential VGA circuit, the input signal is amplified by the G_m stage, and then is further amplified at the diode-connected load stage. Bias voltages V_{GD}

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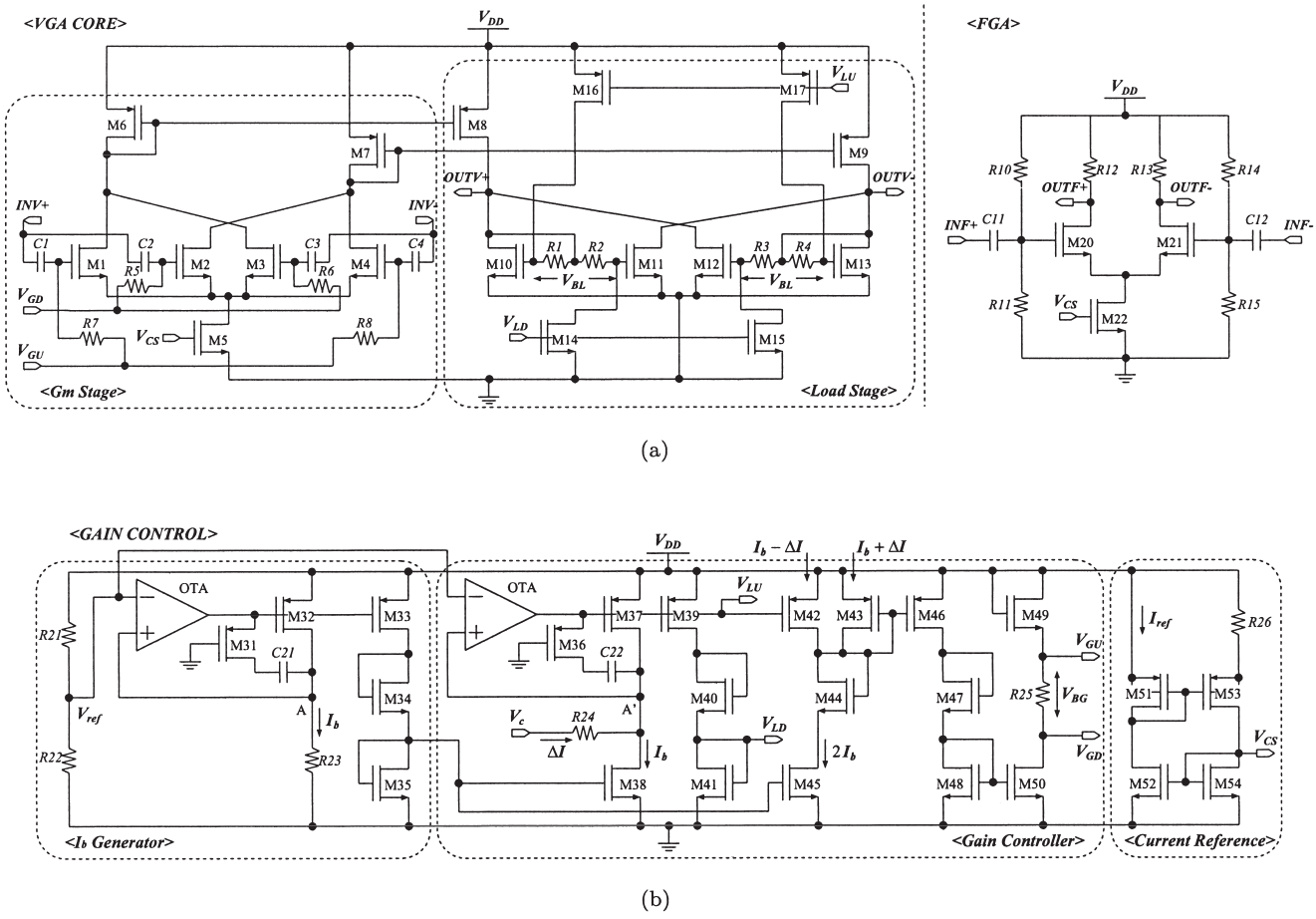

Fig. 2 Schematics of (a) the VGA and the FGA circuits and (b) the gain control circuit.

and V_{GU} generated at the gain controller provides the DC level of capacitively coupled input of VGA. The offset voltage source, $V_{BG}(= V_{GU} - V_{GD})$, is shared in the G_m stage by using $R_5 \sim R_8$ of large resistance, while V_{BL} is generated in the load stage.

The FGA is a differential common source amplifier with resistive load to boost absolute gain of the VGA, which is also capacitively coupled to the inputs. The FGA's are placed at the front and back stage of the VGA because the FGA has low noise figure and wide output dynamic range compared with the VGA.

The DC offset voltage source to control VGA gain consists of a resistor and two MOSFETs, and generates the offset voltage by the current through the resistor. The gain controller generates the voltages, V_{GU}, V_{GD}, V_{LU} and V_{LD} by external control voltage V_c. The offset voltages are given by

$$\begin{aligned} V_{BG} &= V_{GU} - V_{GD} = K_1 R_{25}(I_b + \Delta I), \\ V_{BL} &= K_2(R_1 + R_2)(I_b - \Delta I), \end{aligned} \tag{2}$$

where I_b is drain current of M38, ΔI is current through R_{24} and K_1, K_2 are constants given by size ratio of transistors in the gain controller. $I_b + \Delta I$ flowing through diode-connected M43 is generated using current sink, M45, of $2I_b$ and current source, M42, of $I_b - \Delta I$. From eq.(1), G_{VGA} is determined by V_{BG} and V_{BL} which are oppositely varied with ΔI. The VGA gain control behavior of $(1+x)/(1-x)$, where $x = \Delta I/I_b < 1$, emulates exponential function of $\exp(2x)$.

For the applications of wireless communication, two VGA's have been cascaded to increase gain control range. The cascade connection, however, limits the bandwidth so that a new method to improve the bandwidth has been used as follows. The dominant pole at output node of the VGA is attributed to a resistor and drain capacitance of MOSFETs in the V_{BL} circuit, gate capacitance of diode-connected MOSFET and output capacitance. There is little bandwidth improvement by reducing the resistance due to the inverse relationship between the resistance and drain capacitance under constant V_{BL}. Moreover, this leads to the increase of dissipation current in the V_{BL} circuit. In order to increase 3 dB bandwidth of the VGA, the resistor in the V_{BL} circuit is divided into two equal resistors, R_1 and R_2 (R_3 and R_4), and the output node is connected to the center node between two resistors instead of the gate of M10(M13) (diode-connected load). Similar approach for high speed current mirror, which is a bandwidth improvement technique by introducing a resistor between gate and drain node of diode-connected MOSFET, has been reported [7], while our approach is that by dividing a already existing resistor in DC

offset voltage source. Intuitively, by connecting the output node to the center of DC offset voltage source (center-tapped load), the resistance at output node becomes half compared to the case of diode-connected load. Therefore, it is conceivable that the pole and zero frequencies at the output node are doubled by switching just node connection. From the equivalent circuits of the conventional and proposed load stages shown in Fig. 3, their pole frequency, p, and zero frequency, z, are derived as

$$p = \frac{X_2 \pm \sqrt{X_2^2 - 4X_3\,(g_{m1} - g_{m2})}}{2X_3}, z = \frac{1}{X_1}, \tag{3}$$

where

$$\begin{aligned} X_1 &= 2R_AC_A, \\ X_2 &= 2C_A\,(1 + g_{m1}R_A) + C_{out}, \\ X_3 &= X_1\,(C_A + C_{out}) \end{aligned} \tag{4}$$

in the case of diode-connected load stage, while

$$\begin{aligned} X_1 &= R_AC_A, \\ X_2 &= 2C_A + C_{out}, \\ X_3 &= X_1C_{out} \end{aligned} \tag{5}$$

for center-tapped load stage. Here, C_A is capacitance at the gate node of M10, R_A is resistance of R_1, and g_{m1} and g_{m2} are transconductances of M10 and M11, respectively. Vanished terms from the equation of diode-connected load stage, which are 2 in X_1, $g_{m1}R_A$ in X_2 and C_A in X_3, mean bandwidth improvement with the center-tapped load stage. The ratio of dominant pole frequencies of two load stages is determined by these terms. While there is no bandwidth improvement when $g_{m1}R_A \ll 1$ and $C_A \ll C_{out}$, the ratio

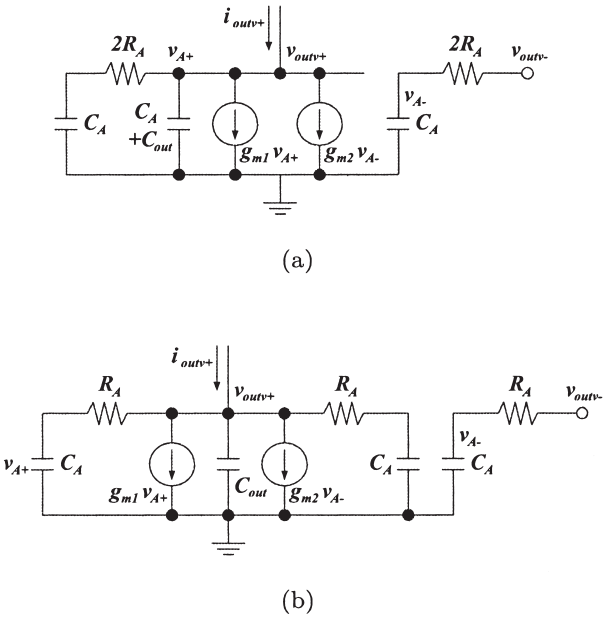

Fig. 3 Equivalent circuits of (a) conventional diode-connected load stage and (b) proposed center-tapped load stage.

can be more than two in the general case of $g_{m1}R_A > 1$ and $C_A \leq C_{out}$. It is assumed that all MOSFETs in the load stage have equal drain capacitances and infinite drain resistances for simplicity. Actually, the dominant pole is determined by the circuit elements of R_1 side from the center tap because PMOS (M16) has larger drain capacitance than NMOS (M14).

The gain of FGA as well as VGA is susceptible to variations in temperature due to temperature dependence of resistors. In order to eliminate the resistance dependence, the I_b generator and the beta multiplier current reference [8] have been added to the gain control circuit. VGA gain is a function of x dependent on R_{24} which determines ΔI. The feedback operational transconductance amplifier (OTA) forces voltage at node A(A') to be equal to V_{ref}. Current I_b generated by V_A across R_{23} in the I_b generator is copied to M38. Then, the resistance term in x is cancelled out. The VGA gain and x are independent of temperature.

$$\begin{aligned} I_b &= \frac{V_{ref}}{R_{23}},\ \Delta I = \frac{V_c - V_{ref}}{R_{24}}, \\ x &= \frac{\Delta I}{I_b} = \frac{R_{23}}{R_{24}} \cdot \frac{V_c - V_{ref}}{V_{ref}}, \end{aligned} \tag{6}$$

where $V_{ref} = V_{DD} \cdot R_{22}/(R_{21} + R_{22})$. The VGA gain is dependent on V_{DD} because V_{ref} is a function of V_{DD}. When $R_{21} = R_{22}$ and $R_{23} = R_{24}$, $G_{VGA} \propto V_c/(V_{DD} - V_c)$. This means that the change of V_{DD} affects the VGA gain. Control of V_c according to V_{DD} variation by auto gain control (AGC) circuit is one solution for this problem.

On the other hand, the gain of FGA is proportional to the load resistance, R_{12} (R_{13}). The current I_{ref} generated by the current reference known as beta multiplier reference is inversely proportional to square of R_{26}. Consequently, FGA gain, G_{FGA}, is also dependent on resistance ratio but independent of temperature [1], [9] as following equations.

$$I_{ref} = \frac{1}{2\beta_{51}R_{26}^2} \quad (W_{53} = 4W_{51}), \tag{7}$$

$$\begin{aligned} G_{FGA} &= -g_{m20} \cdot R_{12} \\ &\propto -\sqrt{2\beta_{20}\frac{I_{ref}}{2}} \cdot R_{12} = -\frac{R_{12}}{R_{26}} \cdot \sqrt{\frac{\beta_{20}}{2\beta_{51}}}. \end{aligned} \tag{8}$$

The temperature stable complete VGA is composed of a pre-FGA, two-stage modified VGA, two-stage post-FGA and a buffer, and its block diagram is shown in Fig. 4. Source follower was used as a buffer amplifier to load a large output capacitor. As mentioned above, by placing the FGA's

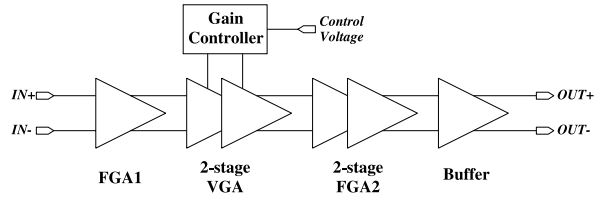

Fig. 4 Block diagram of the complete VGA.

at both sides of the two-stage VGA, improvements of noise and linearity characteristics have been attempted.

3. Simulation and Implementation Results

The circuit has been simulated using HSpice. The VGA with diode-connected load had the 3 dB frequency of 24 MHz at maximum gain which is the worst case of frequency characteristics. The gain range was varied from −18 dB to 11 dB. The bandwidth of the VGA was increased by changing diode-connected load to the center-tapped load, resulting in 83 MHz. Therefore, the bandwidth degradation of the two-stage VGA by cascade connection was relaxed. The 3 dB frequencies of all FGA's and the buffer, wider than 150 MHz, affected rarely the complete VGA bandwidth. As a result, the complete VGA had the 3 dB frequency of 54 MHz and the gain range of 16.5 dB to 74.5 dB at 50 MHz. The temperature dependence of gain has been also simulated at −35°C, 27°C, and 85°C. Differences from the gain at 27°C, were obtained within ± 3 dB overall gain range. A pre-FGA and two stages of post FGAs have been designed as their gains to be about 21.5, 10, and 21 dB, respectively.

The chip has been implemented in 0.25-μm CMOS technology for optional 3.3 V supply voltage with poly and well resistors, and MIM capacitors. For large output swing, the supply voltage was set up to 3.3 V. The chip, shown in Fig. 5, has an active area of less than 0.4 mm^2. The circuit has been carefully laid out to ensure matching of devices in all differential circuits and especially matching of four MOSFETs in each G_m and load stage of the VGA circuit. The channel length of transistors in the gain control circuit requiring large drain resistance was doubled to that in the other circuits. Poly resistors were used as resistors in the DC offset voltage sources and those related to the temperature compensation due to low parasitic capacitance and fluctuation, while well resistors were used in the DC bias circuits requiring large resistance.

Figure 6 shows the measured frequency response of the complete VGA with control voltage from 0.4 V to 2.6 V. The complete VGA consumes 21 mA to 22 mA under 3.3 V supply. The upper 3 dB frequency is 40 MHz at maximum gain, which is slightly smaller than the designed value. This is mainly due to parasitic capacitance of the coupling capacitors, which is added to the load capacitance of each stage. The coupling capacitors in each stage cause the gain reduction for low frequency.

The gain and noise figure (NF) with V_c were measured at a signal frequency of 40 MHz, as shown in Fig. 7. The gain curve shows continuous linear-in-dB characteristics of the complete VGA. The gain varies from 10 dB to 76.5 dB when V_c changes from 0.4 V to 2.9 V. The average gain range sensitivity is around 26 dB/V. Gain out of this V_c range deviates from extension of the gain curve because some transistors does not operate at saturation region. On the other hand, the NF curve shows different characteristics to the gain curve. At 76.5 dB gain, NF of 15 dB was obtained.

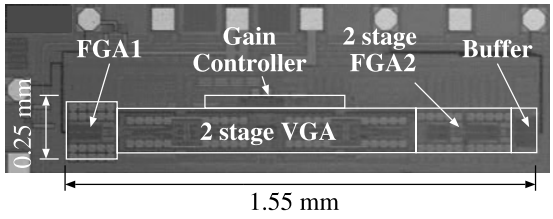

Fig. 5 Photomicrograph of the complete VGA.

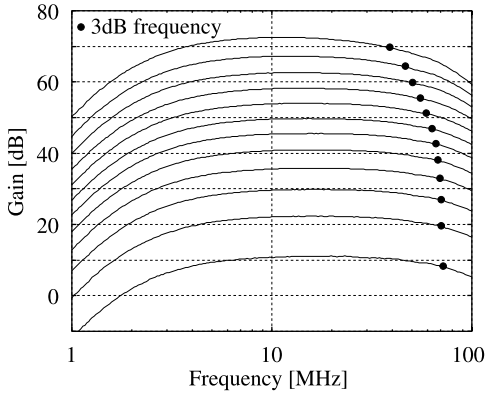

Fig. 6 Frequency responses of the complete VGA increasing control voltage in 0.2 V step from 0.4 V to 2.6 V.

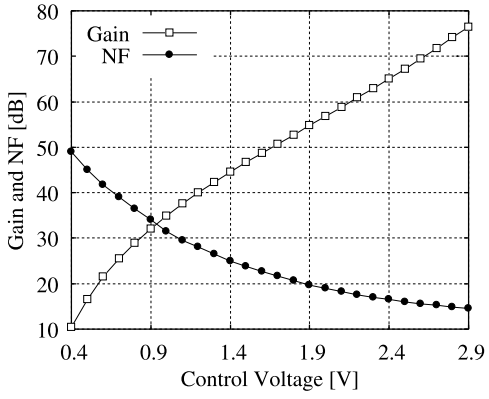

Fig. 7 Gain and NF vs. control voltage at 40 MHz signal frequency.

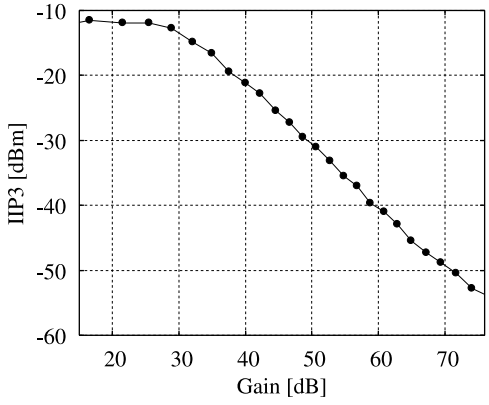

Fig. 8 IIP3 characteristics over the gain control range at 40 MHz signal frequency.

Table 1 Characteristics of the VGA.

Bandwidth (3 dB)	4–40 MHz
Gain range	10–76.5 dB
NF	15 dB
IIP3 @ Gmax	−53 dBm
IIP3 @ Gmin	−11.5 dBm
Supply voltage/current	3.3 V / 21–22 mA

To investigate linearity of the complete VGA, two-tone test at 40 MHz signal frequency with a 1 MHz spacing has been carried out. From the obtained 3rd-order intermodulation distortion (IMD3), the input third intercept point (IIP3) has been calculated [10]. Figure 8 shows the IIP3 characteristics over the gain range. IIP3's of −11.5 dBm at minimum gain and −53 dBm at maximum gain were obtained.

Characteristics of the complete VGA are summarized in Table 1.

4. Conclusions

An IF linear-in-dB VGA for a radio receiver has been presented. The VGA has been fabricated in 0.25-μm CMOS technology. The technique to improve bandwidth of the VGA has been proposed, and the temperature stability of circuit has been also considered. The complete VGA was composed of a pre-FGA, two-stage modified linearized transconductance VGA, two-stage post-FGA and a buffer. The fabricated complete VGA obtained a continuous linear-in-dB gain control range of 10 dB to 76.5 dB, an IIP3 of −11.5 dBm and an NF of 15 dB at 40 MHz signal frequency. The measured results demonstrate that this VGA is suitable for an integrated CMOS radio receiver.

Acknowledgments

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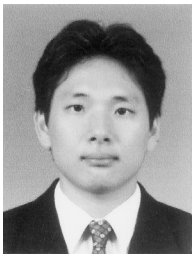

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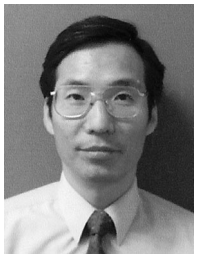

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