PAPER Special Section on Nonlinear Theory and its Applications

# Noise-Induced Synchronization among Sub-RF CMOS Analog Oscillators for Skew-Free Clock Distribution

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**SUMMARY** We present on-chip oscillator arrays synchronized by random noises, aiming at skew-free clock distribution on synchronous digital systems. Nakao et al. recently reported that independent neural oscillators can be synchronized by applying temporal random impulses to the oscillators [1], [2]. We regard neural oscillators as independent clock sources on LSIs; i.e., clock sources are distributed on LSIs, and they are forced to synchronize through the use of random noises. We designed neuron-based clock generators operating at sub-RF region (< 1 GHz) by modifying the original neuron model to a new model that is suitable for CMOS implementation with 0.25-$\mu$m CMOS parameters. Through circuit simulations, we demonstrate that i) the clock generators are certainly synchronized by pseudo-random noises and ii) clock generators exhibited phase-locked oscillations even if they had small device mismatches.

***key words:*** *clock distribution, synchronization, nonlinear oscillators, clock skew*

## 1. Introduction

Synchronous sequential circuits with global clock-distribution systems are the mainstream of implementation in present digital VLSI systems where the clock distribution is the core of synchronous digital operations. Practical clocks given through external pads are distributed to sequential circuits being synchronous to the same clocks via distributed clock networks. System clocks for synchronous digital circuits must arrive at all the registers simultaneously. In practice, time mismatches of clock arrival which are called 'clock skew' occur in LSIs [3]. The major reasons for these mismatches derive from the system clock distribution (wiring defects or asymmetric clock paths), the propagation delay of the clock chip, and the clock traces on the board. The propagation delay is dependent on the fabrication process, voltage, temperature, and loading, which makes the clock skew even more complicated. Small clock skews prevent us from increasing the clock frequency, and large skews may result in severe malfunctions. Indeed clock-skew effects on the circuit performance rise as the integration density (∼miniaturization) or the clock frequency increases.

To resolve these clock-skew issues, various technologies on clock distribution are widely used in present digital systems such as zero-skew clock distribution [4], inserting buffers for skew compensation [5] and controlling the clock-wire length [6]. In regular circuit structures, clock skews are effectively reduced by designing clock paths based on H trees (see [7] for details including statistical analysis). For large-scale complex clock networks, optimizing buffers in the clock distribution tree usually reduces clock skew. One possible way to cancel clock skew is to use asynchronous digital circuits where only local clocks are used instead of global system clocks [8]. However, the functions of these circuits currently cannot satisfy various sophisticated demands. Moreover, major LSI designers have recently started using advanced genetic algorithms in their post-manufacturing processes to calculate the required margin [9].

The present solutions for the skew problems may increase both the total length of clock distribution wires and the power consumption, as well as optimization and post-processing costs. In this paper, we propose another solution for the skew problems. Nakao et al. recently reported that independent neural oscillators can be synchronized by applying appropriate noises to the oscillators [1], [2]. We here regard neural oscillators as independent clock sources on LSIs; i.e., clock sources are distributed on LSIs, and they are forced to synchronize with the addition of artificial (or natural if possible) noises. The authors have proposed an inhibitory neural-network circuit that utilized static and dynamic noises for a "noise-shaping pulse-density modulation" function [10], whereas in this paper we focus on a function of "phase synchronization" among analog oscillators by utilizing dynamic noises. In the following sections, we show a modified neuron-based model that are suitable for hardware implementation, neuron-based clock generators for sub-RF operations (< 1 GHz), and circuit simulation results representing synchronous (or asynchronous) oscillations with (or without) external noises.

## 2. The Model

In the original model [1], the FitzHugh-Nagumo neuron was used to demonstrate the noise-induced synchronization between the time courses of $N$ trials under different initial conditions. Instead we use $N$ conventional Wilson-Cowan oscillators [11] in our model that are suitable for analog CMOS implementation [12]. The dynamics are given by

$$\frac{du_i}{dt} = -u_i + f_\beta(u_i - v_i) + I(t), \tag{1}$$

$$\frac{dv_i}{dt} = -v_i + f_\beta(u_i - \theta), \tag{2}$$

Manuscript received November 27, 2007.
Manuscript revised February 21, 2008.

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DOI: 10.1093/ietfec/e91–a.9.2475

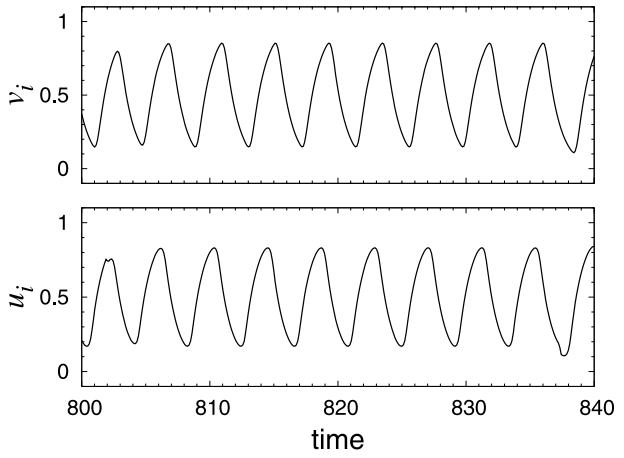



**Fig. 1** Nullclines and trajectories of single Wilson-Cowan type oscillator receiving random impulses.

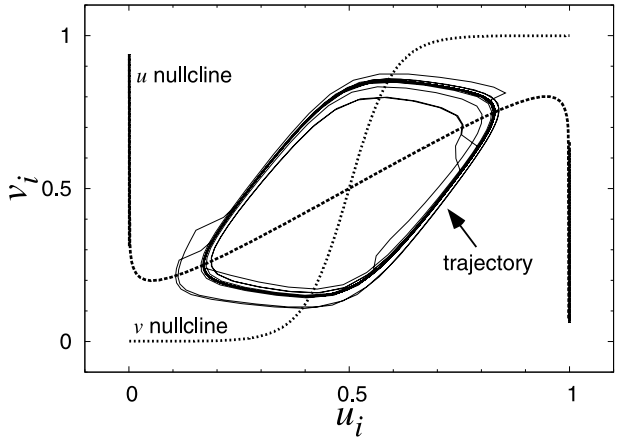



**Fig. 2** Time courses of system variables of single Wilson-Cowan type oscillator receiving random impulses.

where $u_i$ and $v_i$ represent the system variables of the $i$-th oscillator, $\theta$ the threshold, $I(t)$ the common temporal random impulse and $f_\beta(\cdot)$ the sigmoid function with slope $\beta$.

Figures 1 and 2 show numerical simulation results of a single Wilson-Cowan oscillator receiving temporal random impulses given by $I(t) = \alpha \sum_j \delta(t - t_j^{(1)}) - \delta(t - t_j^{(2)})$ where $\delta(t) = \Theta(t) - \Theta(t-w)$ ($\Theta$, $w$ and $t_j$ represent the step function, the pulse width and the positive random number with $t_j^{(1)} \neq t_j^{(2)}$ for all $j$s, respectively). The system parameters were $\theta = 0.5$, $\beta = 10$, $\alpha = 0.5$, $w = 0.1$, and the averaged inter-spike interval of $|I(t)|$ was set at 100. We observed the limit-cycle oscillations (Fig. 1), and confirmed that the trajectory was certainly fluctuated by noisy $I(t)$ (Fig. 2).

When $\beta \to \infty$, the system dynamics can be separated into the following four regions:

$$\text{I } (v < u,\ \ u < \theta) : \begin{cases} \dot{u}_i = -u_i + 1 + I(t) \\ \dot{v}_i = -v_i \end{cases}, \tag{3}$$

$$\text{II } (v < u,\ \ u > \theta) : \begin{cases} \dot{u}_i = -u_i + 1 + I(t) \\ \dot{v}_i = -v_i + 1 \end{cases}, \tag{4}$$

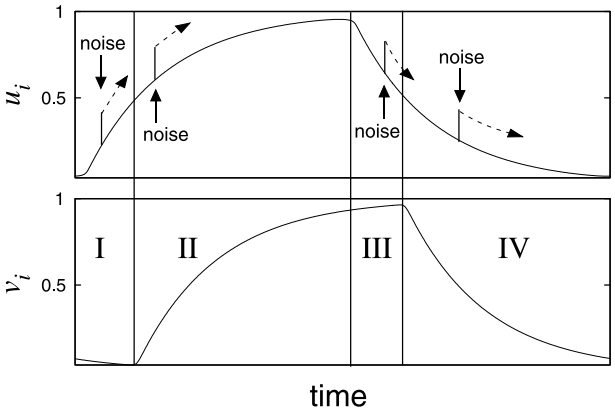



**Fig. 3** Four operational regions (I to IV) of Wilson-Cowan system.

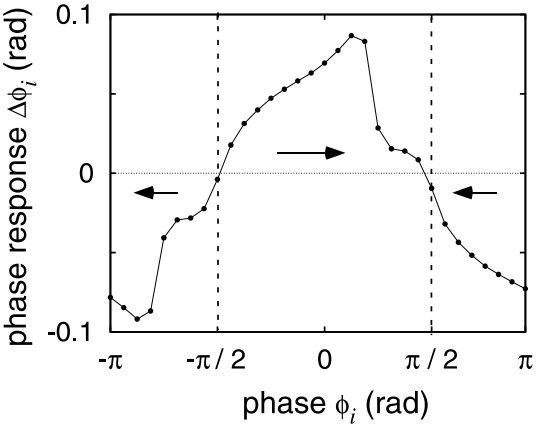



**Fig. 4** Phase response curve of Wilson-Cowan system.

$$\text{III } (v > u,\ \ u > \theta) : \begin{cases} \dot{u}_i = -u_i + I(t) \\ \dot{v}_i = -v_i + 1 \end{cases}, \tag{5}$$

$$\text{IV } (v > u,\ \ u < \theta) : \begin{cases} \dot{u}_i = -u_i + I(t) \\ \dot{v}_i = -v_i \end{cases}, \tag{6}$$

where $\dot{u}_i$ and $\dot{v}_i$ represent $du_i/dt$ and $dv_i/dt$, respectively. Figure 3 shows time courses of $u_i$ and $v_i$ for one period indicating the four regions. In regions I and II, $u_i$ is increasing to 1. Therefore, the oscillation phase $\phi_i$ ($\equiv \tan^{-1}(v_i - 0.5)/(u_i - 0.5)$) is advanced when a positive impulse is given ($I(t) > 0$). On the other hand, in regions III and IV, since $u_i$ is decreasing to 0, the phase is delayed when a positive impulse is given, as shown in Fig. 3.

Figure 4 shows a simulated phase-response curve (PRC) of the Wilson-Cowan system. The PRC represents degrees of the phase advance or phase delay ($\Delta\phi_i$) when an external input is given to the system at $\phi_i$ [13]. In the simulation, we applied a single positive impulse as $I(t)$ at $\phi_i$ ($-\pi \sim \pi$) and measured the resulting phase difference $\Delta\phi_i$. When $-\pi/2 < \phi_i < \pi/2$, $\Delta\phi_i$ was positive, which indicated that the phase was increased when an impulse was given to the system during this term. Otherwise, $\Delta\phi_i$ was negative, and thus the phase was decreased. Here it should be noticed that phase $\phi_i$ diverges around $\phi_i = -\pi/2$, whereas $\phi_i$ converges around $\phi_i = \pi/2$, as shown by left and right arrows in

Fig. 4. Consequently, $\phi_i$ would be locked at $\phi_i \approx \pi/2$ as the time being, when the system accepts random impulses.

We conducted numerical simulations using 10 Wilson-Cowan oscillators ($N = 10$). All the oscillators have the same parameters, and accept (or do not accept) the common random impulse $I(t)$. The initial condition of each oscillator was randomly chosen. Figure 5 shows the raster plots of 10 oscillators (vertical bars were plotted at which $u_i > 0.5$ and $du_i/dt > 0$). When the oscillators did not accept $I(t)$ ($\alpha = 0$), they exhibited independent oscillations as shown in Fig. 5(a), however, all the oscillators were synchronized when $\alpha = 0.5$ as shown in Fig. 5(b). To evaluate the degree of the synchronization, we use the following order parameter:

$$R(t) = \frac{1}{N}\left|\sum_j \exp(i\phi_j)\right|,$$

where $N$ represents the number of oscillators, and $i$ the imaginary unit. When all the oscillator are synchronized, $R(t)$ equals 1 because of the uniform $\phi_j$s, while $R(t)$ is less than 1 if the oscillators are not synchronized. Figure 6 shows the time courses of the order parameter values. When $\alpha = 0$,

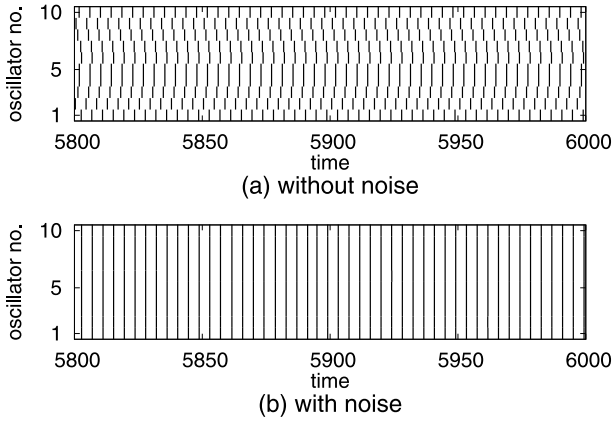



**Fig. 5** Raster plots of 10 oscillators. (a) independent oscillations without random impulses, (b) synchronous oscillations with random impulses.

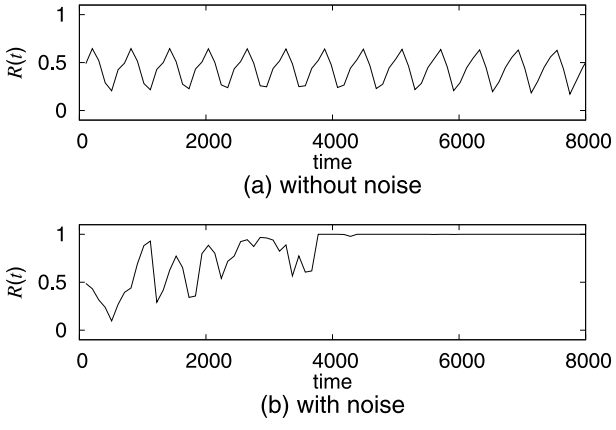



**Fig. 6** Time courses of order parameter values (a) without random impulses and (b) with random impulses.

$R(t)$ was unstable and was always less than 1 [Fig. 6(a)], whereas $R(t)$ remained at 1 after it became stable at $t \approx 5000$ when $\alpha = 0.5$ [Fig. 6(b)]. These results indicate that if we implemented these oscillators as clock generators on CMOS LSIs, applying common random pulses to the oscillators could synchronize them.

## 3. The Circuit and Simulation Results

We designed a Wilson-Cowan oscillator circuit for sub-RF operations (Fig. 7). The circuit consists of a differential pair (M1 to M3) and a buffer circuit composed of two standard inverters. When $I(t) = 0$ and time constants of the Wilson-Cowan system are very small, one can rewrite Eqs. (1) and (2) as

$$u_i \approx f_\beta(u_i - v_i), \tag{7}$$

$$v_i \approx f_\beta(u_i - \theta). \tag{8}$$

The OTA's output voltage ($V_o$) is expressed by $V_{dd} \cdot f(V_1 - V_2)$, while output voltage of the buffer circuit ($V_{o2}$) is given by $V_{dd} \cdot f(V_{in} - V_{dd}/2)$, where $f(\cdot)$ represents a nominal Sigmoid-like function. We thus obtain

$$u_i = V_{dd} \cdot f(u_i - v_i), \tag{9}$$

$$v_i = V_{dd} \cdot f(u_i - V_{dd}/2), \tag{10}$$

by connecting the inputs and outputs to $u_i$ and $v_i$ as shown in Fig. 7 ($V_1 = V_o = u_i, V_2 = v_i, V_{in} = u_i, V_{o2} = v_i$), which corresponds to Eqs. (7) and (8).

In the Wilson-Cowan system, the noise term, $I(t)$, was added to $u_i$'s dynamics only. The easiest way to give noises to the proposed circuit is to couple digital M-sequence circuits with node $u_i$ via a capacitor. The capacitor currents caused by random transitions (0→1 or 1→0) of the M-sequence circuits may fluctuate $u_i$. However, since the proposed circuit is operating in the voltage mode, current injection and ejection via small capacitance may not fluctuate $u_i$ effectively. Therefore, in the proposed circuit, the noisy term was included in the slope factor of OTA's $f(\cdot)$. The slope factor increases vastly as $V_{ref}$ increases. Therefore, by fluctuating $V_{ref}$ with $V_{mseq}$ via $C$, one can perturb the circuit effectively.

In the following simulations, we used TSMC's 0.25-$\mu$m CMOS parameters with $W/L = 0.36\,\mu$m / $0.24\,\mu$m except for M3's channel length ($L = 2.4\,\mu$m). Pseudo-random

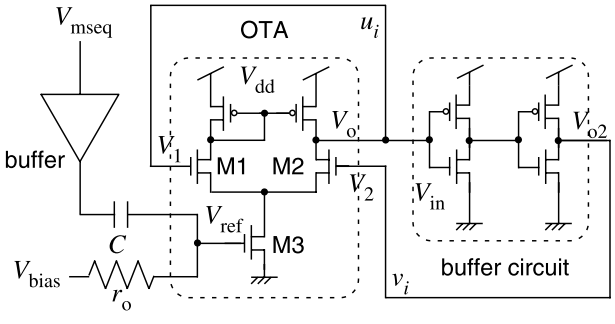



**Fig. 7** Wilson-Cowan circuit for sub-RF operations.

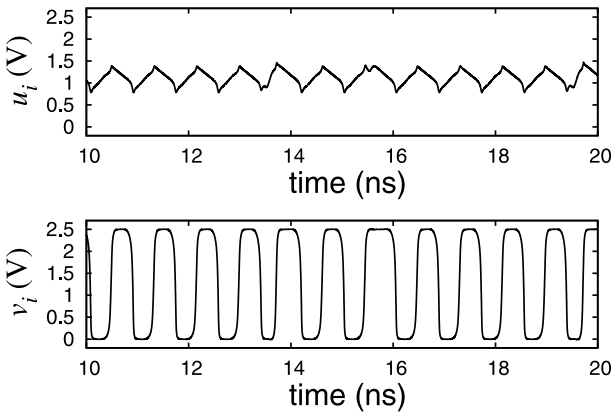



**Fig. 8** Time courses of system variables of oscillator circuit receiving pseudo-random impulses.

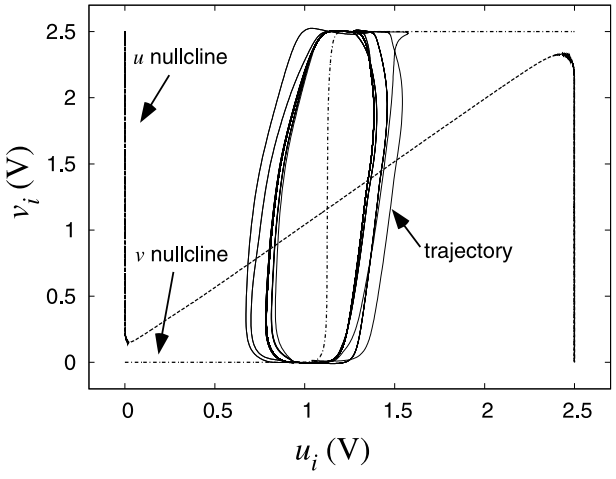



**Fig. 9** Nullclines and trajectories of oscillator circuit receiving pseudo-random impulse.

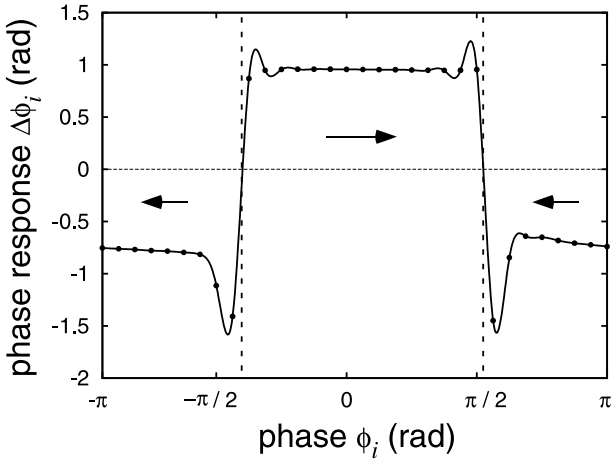



**Fig. 10** Phase response curve of the neuron circuit.

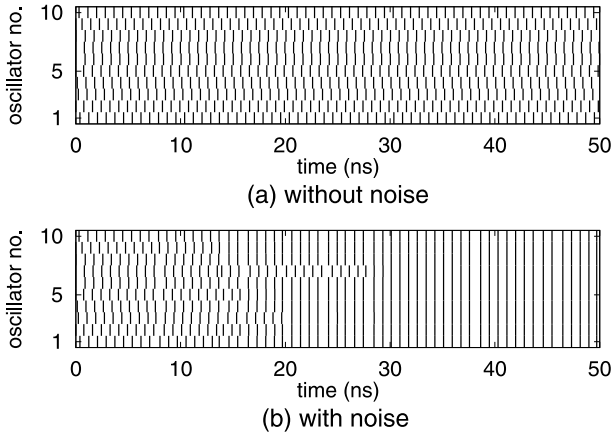



**Fig. 11** Raster plots of 10 oscillator circuits. (a) independent oscillations among proposed circuits without random impulses, (b) synchronous oscillations among proposed circuits receiving random impulses.

sequences ($V_{\mathrm{mseq}}$) were generated using a 4-bit M-sequence circuit.

Figures 8 and 9 show SPICE results of the proposed circuit receiving random impulses ($C = 20\,\mathrm{fF}$ and $R_o = 1\,\mathrm{k\Omega}$; the clock frequency of the M-sequence circuit was 500 MHz, which resulted in a 30-ns pseudo-random sequence). The supply voltage was fixed at 2.5 V. Time courses of $u$ and $v$ are shown in Fig. 8. The simulated nullclines and trajectories are shown in Fig. 9. We observed qualitatively-equivalent nullclines and trajectories to those of the Wilson-Cowan oscillators, and confirmed the limit-cycle oscillations where the trajectory was effectively fluctuated by the M-sequence circuit with the RC filter. The oscillation frequency was 1.17 GHz when the reference voltage $V_{\mathrm{bias}}$ was set at 1 V (M3's DC current was limited up to $60\,\mu$A).

We calculated PRCs of the proposed circuit (Fig. 10). Since the circuit's phase response ($\Delta\phi_i$) had positive and negative parts, the phase converges to around $\pi/2$ as the time being. This implies that if we implement multiple oscillator circuits, their phases are converged to the same values when they receive a common random noise. To confirm this, we employed 10 oscillator circuits. Figure 11 shows the raster plots of the simulated oscillator circuits (vertical bars were plotted at which $v_i > 1.25$ V and $dv_i/dt > 0$). All the circuits exhibited independent oscillations when random sequence $V_{\mathrm{mseq}}$ was not given to them [Fig. 11(a)], whereas after $t \approx 30$ ns they exhibited complete synchronization when $V_{\mathrm{mseq}}$ was given [Fig. 11(b)].

Time courses of the order parameter values were shown in Fig. 12. When random impulse was not given to the circuit, $R(t)$ was always less than 1 [Fig. 12(a)], while $R(t)$ approached to 1 after $t \approx 30$ ns when random impulse was given [Fig. 12(b)]. The reason why $R(t)$ did not converged to 1 is due to stiff oscillations of $v_i$; small phase differences between the oscillators were expanded at the rising and falling times of square-shaped $v_i$.

Our results indicate that if we distributed these circuits as ubiquitous clock sources on digital CMOS LSIs, they could be synchronized when common random impulses were given to the circuits. Although this may cancel out the present clock skew problems, device mismatches between

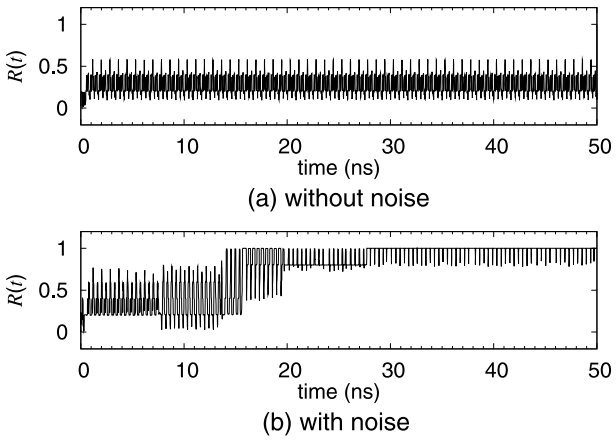



**Fig. 12** Time courses of order parameter values (a) without random impulses and (b) with random impulses.

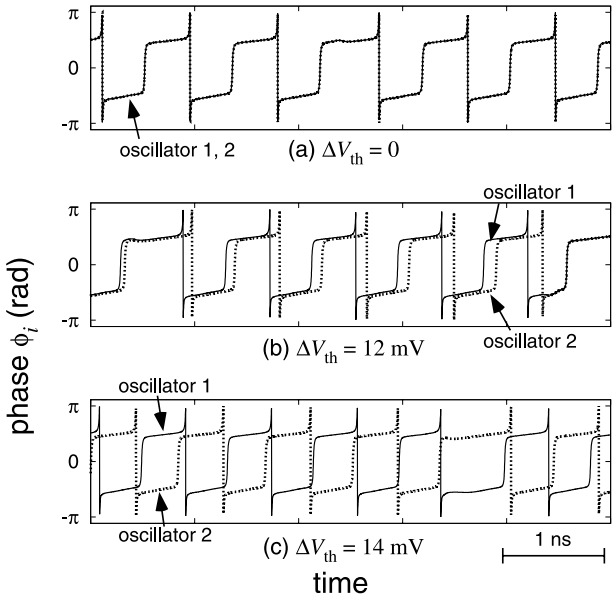



**Fig. 13** Time courses of phases of two oscillator circuits. (a) two identical oscillators ($\Delta V_{th} = 0$), (b) $\Delta V_{th} = 12$ mV and (c) $\Delta V_{th} = 14$ mV.

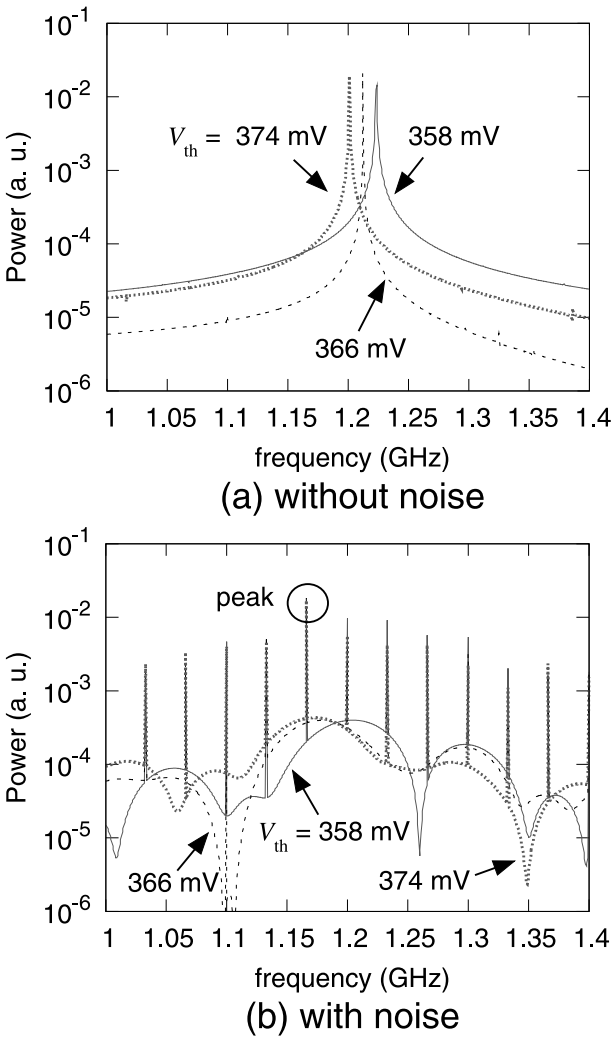



**Fig. 14** Power spectrum density of three oscillator circuits having different threshold voltages ($V_{th} - 8$ mV, $V_{th}$ and $V_{th} + 8$ mV where $V_{th} = 366$ mV) (a) without noises and (b) with common noises.

the clock sources may prevent the sources from complete synchronization. Therefore, we investigated the device-mismatch dependence of the proposed circuits. For our distributing purposes, local mismatches in a single oscillator circuit would be negligible; i.e., mismatches in a differential pair (M1 and M2) and a current mirror. Mismatches in inverters corresponding to threshold $\theta$ in Wilson-Cowan model would also be negligible because they only shift the fixed point, and do not vastly change the oscillation frequency. However, mismatches of M3 between the oscillators may drastically change each oscillator's intrinsic frequency. Therefore, we investigated effects of threshold voltages of M3s on synchronizing properties. Figure 13 shows time courses of phases of two oscillator circuits. As differences of threshold voltages of M3s ($\Delta V_{th}$) increased, the phase difference expanded. Interestingly, the phase difference of two oscillators having different intrinsic frequencies ($\Delta V_{th} \neq 0$ ) was almost locked when random noises were given. This is caused by simultaneous noise injection to the oscillators, and this phase-locked structure is broken when clock frequencies of the M-Sequence circuit is decreased.

The threshold mismatch ($\Delta V_{th}$) does not affect the amplitude because the peak-to-peak amplitude is always limited up to the supply voltage and the ground (thus mismatches of the supply voltage may affect the amplitude), whereas the mismatch does affect the oscillator's operation frequency. Figure 14(a) shows the power spectrum density of three noiseless oscillator circuits having different threshold voltages ($V_{th} - 8$ mV, $V_{th}$ and $V_{th} + 8$ mV where $V_{th} = 366$ mV). As the threshold voltage decreased, the peak frequency was increased because the M3's current (∼operation frequency) is increased by the decrease of the threshold voltage. Figure 14(b) shows the power density when the common noises were applied to the three oscillators. We found that all the oscillators had the same peak frequencies (≈

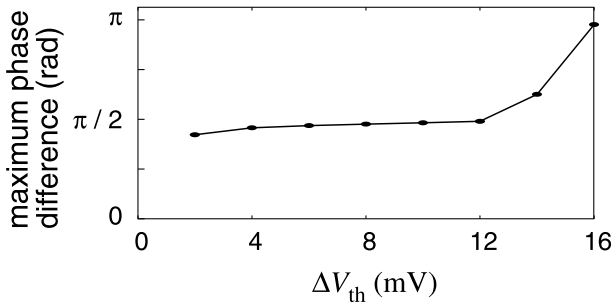



**Fig. 15** Synchrony dependence on parameter mismatch.

1.17 GHz) although they had different threshold voltages.

Figure 15 shows dependence of maximum phase differences among two oscillators on $\Delta V_{\rm th}$. The absolute phase differences were measured between 50 ns and 150 ns for every $\Delta V_{\rm th}$, and we plotted the maximum difference. Surprisingly, when $\Delta V_{\rm th} < 12$ mV, the maximum phase difference was fixed around $\pi/2$, which indicates that the circuit has small tolerance on device mismatches, although the phase difference exists. Using distributed oscillators as clock sources in sequential circuits with the phase difference over $\pi$ ($\Delta V_{\rm th} \geq 16$ mV in our simulations) are definitely not safe, whereas if the phase difference is smaller than $\pi$, one can deal with this difference somehow. Still we do not have exact solutions, but our 'ubiquitous' clock sources with small device mismatches would be synchronized by optimizing our parameter sets.

These results imply that instead of our oscillator circuit, one can employ radio-frequency (RF) oscillators, e.g., voltage-controlled oscillators in phase-locked loops used in present digital VLSIs, to demonstrate the phase synchronization among the oscillators. The reasons why we limited our circuit's oscillation frequency up to around 1 GHz (sub-RF region) are: i) CMOS RF oscillators require on-chip spiral inductors where extensive optimization of inductor layout including electromagnetic analysis are necessary and ii) evaluations of the fabricated chips implementing the RF oscillators would be difficult with our present measurement equipments. Since clock skews can be observed even in digital circuits operating at sub-RF clock frequencies, our possible target would be low-power and low-end micro processors for, e.g., mobile IT products.

For practical implementation, we have to consider how we apply the common noises to all the oscillators. One possible solution is to use power supply noises in large-scale digital circuits. Recent power-supply noise modeling and on-chip measurement results [14] showed that noises on power-supply voltages are quasi periodic, and are not negligible now. Power-supply noises on wide wires could be distributed to the clock sources without local deviation. Another idea is to use external (off-chip) electromagnetic noise sources. In this case, each clock source should implement antennas at the topmost metal layer to catch the electromagnetic noises, and other circuit block must be shielded. Our present circuit employed M-sequence circuits for the demonstration aim, they must be replaced with more practical noises that can reach at each oscillators simultaneously.

## 4. Conclusion

We designed CMOS sub-RF oscillators that could be synchronized using common random impulses, based on a theory in [1], [2]. We proposed a modified Wilson-Cowan model for implementing FitzHugh-Nagumo oscillators. We confirmed that the synchronization properties of the modified model were qualitatively equivalent to those of the original model. We then designed sub-RF oscillator circuits based on the modified model. Through circuit simulations, we demonstrated that the circuits exhibited the same synchronization properties as in the original and modified models. For our clock-distributing purposes, we investigated the synchrony dependence on device mismatches between two oscillator circuits. The result showed that i) the oscillators exhibited phase-locked oscillation and ii) the circuit had small tolerance on device mismatches, although small phase difference ($\pi/2$) exists.

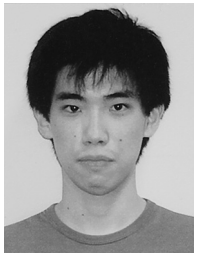
## Acknowledgments

The authors wish to thank Dr. Kensuke Arai of the Kyoto University for most valuable discussions and suggestions during the research. This study was partly supported by Industrial Technology Research Grant Program in '04 from New Energy and Industrial Technology Development Organization (NEDO) of Japan, and a Grant-in-Aid for Young Scientists [(B)17760269] from the Ministry of Education, Culture Sports, Science and Technology (MEXT) of Japan.

### References

[1] H. Nakao, K. Arai, and K. Nagai, "Synchrony of limit-cycle oscillators induced by random external impulses," Phys. Rev. E, vol.72, 026220, 2005.
[2] H. Nakao, K. Arai, and Y. Kawamura, "Noise-induced synchronization and clustering in ensembles of uncoupled limit-cycle oscillators," Phys. Rev. Lett., vol.98, 184101, 2007.
[3] D.E. Brueske and S.H.K. Embabi, "A dynamic clock synchronization technique for large systems," IEEE Trans. Compon. Packag. Manuf. Technol. B, vol.17, pp.350–361, 1994.
[4] R.S. Tsay, "An exact zero-skew clock routing algorithm," IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst., vol.12, no.2, pp.242–249, 1993.
[5] R.B. Watson, Jr. and R.B. Iknaian, "Clock buffer chip with multiple target automatic skew compensation," IEEE J. Solid-State Circuits, vol.30, no.11, pp.1267–1276, 1995.
[6] T.-H. Chao, Y.-C. Hsu, J.-M. Ho, and A.B. Kahng, "Zero skew clock routing with minimum wirelength," IEEE Trans. Circuits Syst. II, vol.39, no.11, pp.799–814, 1992.
[7] M. Hashimoto, T. Yamamoto, and H. Onodera, "Statistical analysis of clock skew variation in H-tree structure," IEICE Trans. Fundamentals, vol.E88-A, no.12, pp.3375–3381, Dec. 2005.
[8] C.J. Myers, Asynchronous Circuit Design, Wiley-Interscience, 2001.
[9] E. Takahashi, Y. Kasai, M. Murakawa, and T. Higuchi, "Post-fabrication clock-timing adjustment using genetic algorithms," IEEE J. Solid-State Circuits, vol.39, no.4, pp.643–649, 2004.

[10] A. Utagawa, T. Asai, T. Hirose, and Y. Amemiya, "An inhibitory neural-network circuit exhibiting noise shaping with subthreshold MOS neuron circuits," IEICE Trans. Fundamentals, vol.E90-A, no.10, pp.2108–2115, Oct. 2007.
[11] H.R. Wilson and J.D. Cowan, "Excitatory and inhibitory interactions in localized populations of model neurons," Biophys. J., vol.12, pp.1–24, 1972.
[12] T. Asai, Y. Kanazawa, T. Hirose, and Y. Amemiya, "Analog reaction-diffusion chip imitating the Belousov-Zhabotinsky reaction with hardware oregonator model," International Journal of Unconventional Computing, vol.1, no.2, pp.123–147, 2005.
[13] A.T. Winfree, The geometry of biological time, 2nd ed., Springer-Verlag, 2001.
[14] K. Ichikawa, Y. Takahashi, and M. Nagata, "Experimental verification of power supply noise modeling for EMI analysis through on-board and on-chip noise measurements," IEICE Trans. Electron., vol.E90-C, no.6, pp.1282–1290, June 2006.



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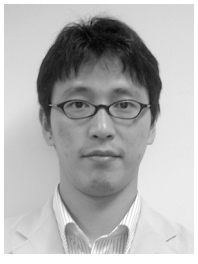

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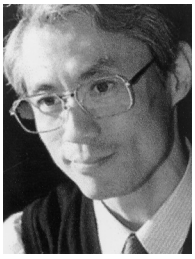

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