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A NOVEL CMOS CIRCUIT FOR DEPRESSING SYNAPSE AND ITS APPLICATION TO CONTRAST-INVARIANT PATTERN CLASSIFICATION AND SYNCHRONY DETECTION

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Abstract

A compact complementary metal-oxide semiconductor (CMOS) circuit for depressing synapses is designed for demonstrating applications of spiking neural networks for contrast-invariant pattern classification and synchrony detection. Although the unit circuit consists of only five minimum-sized transistors, they emulate fundamental properties of depressing synapses. The results of the operations are evaluated by both experiments and the simulation program with integrated circuit emphasis (SPICE).

Key Words

Dynamic synapse, depressing synapse, spiking neuron, analog circuit, neuromorphic VLSI

1. Introduction

Silicon circuits that mimic the nervous systems of insects and animals represent the future of neurocomputing. These circuits can perform various neural functions because the microstructures of a nervous system are replicated in their silicon chips. A number of neural chips have been developed, such as silicon neurons that emulate cortical pyramidal neurons [1], FitzHugh-Nagumo neurons with negative resistive circuits [2], and artificial neuron circuits based on byproducts of conventional digital circuits [3–5]. As recent functional models of spiking neural networks tend to use integrated-and-fire neurons (IFNs) rather than the Hodgkin-Huxley-type neurons [6], neuromorphic engineers have developed hardware neural systems with several types of IFN circuits to investigate the effect of spike timing and synchrony on the network's computational properties, such as competitive neural circuits with IFNs for processing sensory signals [7, 8] and learning circuits with spike-driven synaptic plasticity [9, 10].

In addition to the IFNs, dynamic synapses have also attracted the attention of neuromorphic engineers who focus mainly on the dynamic implications of the neurons. Senn showed an easy way to extract coherence information among cortical neurons by projecting spike trains through depressing synapses onto a postsynaptic neuron [11]. Moreover, a recent model of the layer IV circuitry, which accounts for several contrast-dependent nonlinearities in cortical responses, suggests that synaptic depression contributes to solving the problem of contrast-invariant orientation tuning [12]. Based on this suggestion, Bugmann showed that the strength of a time-averaged current injected into the soma by using a spike train is independent of its frequency, which implies that the response strength of a target neuron depends only on the number of active inputs [13].

Several CMOS circuits that emulate dynamic synapses have been developed [14, 15]. These circuits used capacitors to obtain temporal properties of the dynamic synapse, which prevents us from large-scale implementation of synaptic circuits for practical applications. In this article we propose a compact CMOS circuit that emulates the depressing properties of dynamic synapses. The circuit consists of five transistors without capacitors. We also exhibit network circuits implementing the Bugmann's model for contrast-invariant pattern classification [13] and Senn's model for synchrony detection [11], to demonstrate the properties of our synaptic circuit.

2. Analog CMOS Circuit for Depressing Synapse

A synapse whose conductivity changes based on the firing rate or spike timing of presynaptic neurons is called a dynamic synapse [16, 17]. The change in weight of dynamic synapses is caused by short-term changes in the transmitter discharge and regeneration cycle at the terminal of

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presynapses rather than by learning at the network level. These synapses produce excitatory postsynaptic potential (EPSP) or inhibitory postsynaptic potential (IPSP) by integrating the output of the presynaptic neurons. A signal is conducted to a postsynaptic neuron through EPSP and IPSP. When the firing rate of the presynaptic neurons increases so that the sequential changes in EPSP and IPSP can no longer keep up with the input, the efficiency of signal conduction to the postsynaptic neurons drops. Because presynaptic neuron output is depressed and conducted to the postsynaptic neurons, such a synapse is called a "depressing synapse" and a synapse acting inversely is called a "facilitating synapse."

Fig. 1 shows our MOS circuit for such a depressing synapse constructed by a current mirror (M_3 and M_5) and pMOS common-source amplifier (M_2 and M_4). When there is no input ($I_{\rm in} = 0$), voltage $V_{\rm e}$ at junction A is zero because of leak transistor M_2. Therefore, transistor M_1 is on. When there is input ($I_{\rm in} > 0$) that increases $V_{\rm e}$, M_1 is turned off. Therefore, the current is mirrored to output $I_{\rm out}$ through transistor M_1.

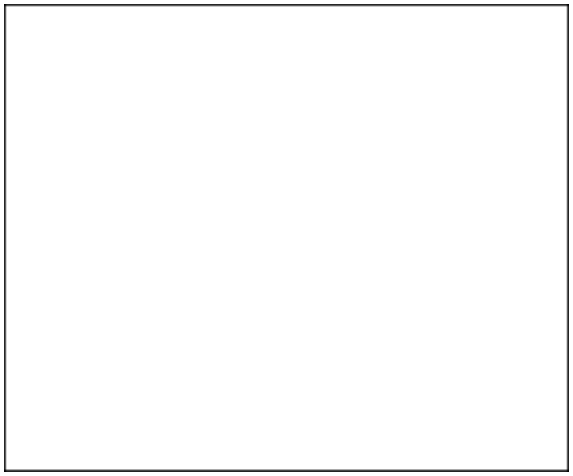

Figure 1. Depressing synapse circuit with five minimum-sized transistors and parasitic capacitance.

Because there is parasitic capacitance $C_{\rm e}$ at junction A, the increase in $V_{\rm e}$ has a short-time delay. Therefore, M_1 enters an on state for a short time, and the circuit outputs spike current $I_{\rm out}$. When the input current becomes zero again, M_2 discharges the capacitance $C_{\rm e}$, and $V_{\rm e}$ returns to zero. Remarkably, the mirror effect of the pMOS common-source amplifier, which amplifies the value of additional parasitic capacitance between the drain and gate terminal of M_4, increases this discharging time.

Now assume that the spike current is given at a short interval, and that subsequent spikes enter before $V_{\rm e}$ returns to zero. In this case, the amplitude of the output spikes decreases when $V_{\rm e}$ increases. Because the current of transistor M_2 increases monotonically when $V_{\rm bias}$ increases, the time until $V_{\rm e}$ returns to zero decreases. By adjusting voltage $V_{\rm bias}$, it is thus possible to change the duration of the depression. Notice that when $V_{\rm bias}$ is set at VDD, the circuit behaved as a nondepressed synapse because $V_{\rm e}$ is zero and M_1 is always on.

It should be noted that our circuit implements only the weight dynamics of the depressing synapse. However, conventional analog memory devices, such as floating-gate MOS (FGMOS) FETs with Fowler-Nordheim tunneling electrodes [18], can easily be incorporated into our circuit. Namely, if M_5 is replaced with a FGMOS FET, the synaptic weight can be changed (through some learning) independent of the weight dynamics. On the other hand, if M_2 or M_4 is replaced with a FGMOS FET, the weight dynamics can be changed and thus learned.

3. Experimental and Simulation Results

We fabricated a prototype circuit using a 1.5-μm scalable CMOS rule (MOSIS, vendor: AMIS, n-well single-poly double-metal CMOS process). Fig. 2 shows the layout of a depressing-synapse circuit. The circuit took up a total area of $35\,\mu{\rm m} \times 36\,\mu{\rm m}$.

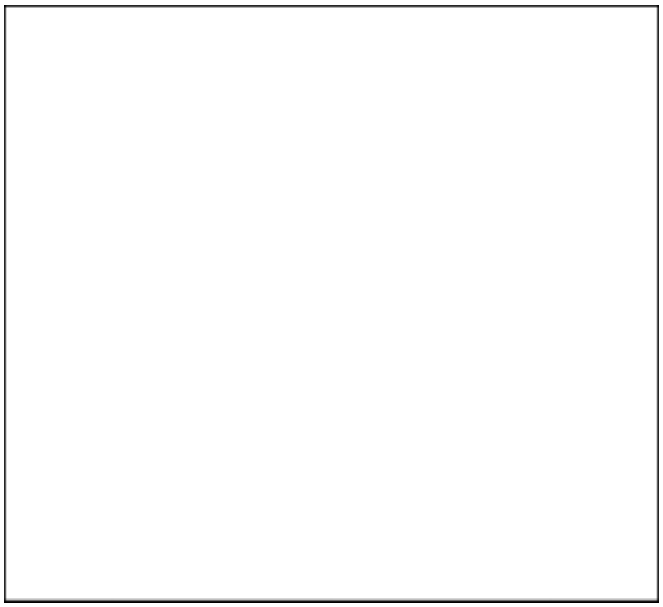

Figure 2. IC layout of depressing synapse circuit (total area of $35\,\mu{\rm m} \times 36\,\mu{\rm m}$ with a 1.5-μm scalable CMOS rule).

Fig. 3 shows time courses of the output of the synapse circuit for increasing input-spike intervals. The experimental conditions were ${\rm VDD} = 5\,{\rm V}$, $V_{\rm bias} = 0.1\,{\rm V}$, input spike width $= 0.1\,{\rm ms}$, and spike amplitude $= 1\,\mu{\rm A}$. A load resistance of $100\,{\rm M}\Omega$ was connected between the output terminal of the circuit and ground to obtain the output current $I_{\rm out}$ as the voltage $V_{\rm out}$. Fig. 3(a) shows input voltage $V_{\rm in}$ of transistors $M_3 \sim M_5$ that decreases from 5 V to 3.7 V when the spike current is given. The first spike was given at $t = 0$. Subsequent spikes were given at $t = 10$, 30, 60, and 120 ms. When the inputs were given successively in a short time (around 0 to 30 ms in Fig. 3(a)), the amplitude of the output pulse was depressed (Fig. 3(c)). As the interval widened, $V_{\rm e}$ approached zero (Fig. 3(b)) and the amplitude of the output pulse returned to the initial value.

Figure 3. Experimental results of depressing synapse circuit; (a) successive spike inputs, (b) degree of synaptic depression, and (c) its outputs.

Fig. 4 shows the change in amplitude of the output spike against the input firing rate. The leak voltage V_{bias} was set at 0.1, 0.2, and 0.3 V. As the spike frequency increased, the amplitude of the output pulse decreased. By increasing V_{bias}, the cutoff frequency was successfully shifted towards the higher frequency.

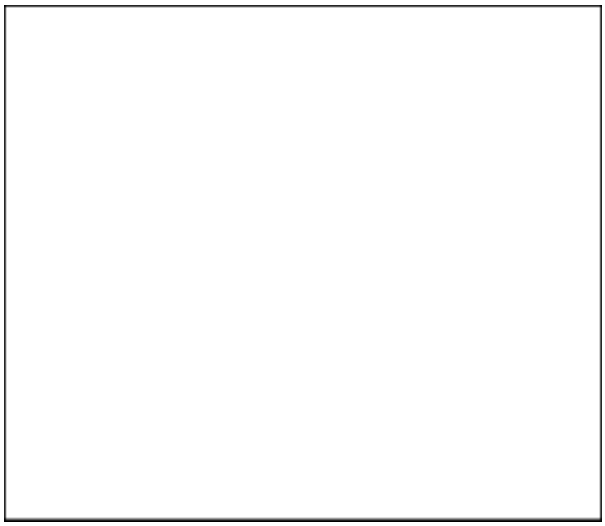

Figure 4. Changes in amplitude of output of depressing synapse circuit against firing rate of presynaptic neuron.

In the following subsections, we show applications of the proposed circuit to spiking neural networks for contrast-invariant pattern classification and synchrony detection. Although these networks are designed to be useful when a large number of depressing synapses are employed, we constructed small-scale circuits to demonstrate only the fundamental properties of the hardware neural networks. As our circuit occupies an area of $35\,\mu\mathrm{m} \times 36\,\mu\mathrm{m}$ even if we use a 1.5-μm CMOS process, its large-scale implementation is remarkably easy.

3.1 Application to the Bugmann's Neural Network for Contrast-Invariant Pattern Classification

Bugmann showed that the strength of a time-averaged current injected into the soma using a spike train tends to be independent of its frequency, which implies that the response strength of a target neuron depends only on the number of active inputs [13]. We demonstrate it here using our depressing synapse circuits.

Let us assume a simple circuit, as shown in Fig. 5. The circuit is designed based on Bugmann's neural network. The right part represents a leaky IFN and the left part represents its dendrite. The IFN consists of a membrane capacitance (C_1), a diode-connected leak MOS transistor, and a threshold detector (V_{th}). In the Bugmann's model, an IFN is used to determine whether the membrane potential exceeds a given threshold value or not. In this sense, the functional behaviour of the model will not be changed, no matter what types of IFNs are used. So, here we employed one such simple IFN circuit.

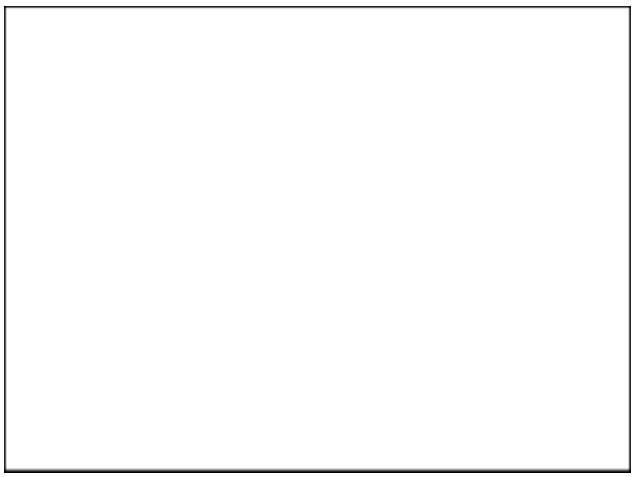

Figure 5. Experimental setups for pattern classification and synchrony detection.

The IFN accepts spike inputs from excitatory neurons through depressing synapses. The IFN outputs a spike when its EPSP $> V_{\mathrm{th}}$, and resets the EPSP after the firing. In this setup, average values of the EPSP increase in proportion to the number of presynaptic active neurons. Therefore, it can detect the number of presynaptic active neurons by setting appropriate threshold V_{th} corresponding to the number of active neurons. On the other hand, the EPSP also increases in proportion to the firing rate of spiking neurons. Therefore, ability to discriminate the number of presynaptic active neurons largely deteriorates if the firing rate is not at a constant value.

It has been shown that this discrimination performance is improved by using the depressing synapse [13]. If input spikes are given to the depressing synapse successively in a short period, the efficiency to increase the EPSP per spike drops. Even if the number of input spikes increases with an increase in the firing rate, the value of EPSP does not dramatically change because the efficiency per spike is lowered by the synaptic depression. Namely, the discrimination performance of the network tends to be independent

of firing frequency. To demonstrate this, we construct a network in which four synapse circuits are connected to the IFN circuit. We compared the operation of the neuron circuit with nondepressed and depressed circuits as the number of active presynaptic neurons increases (Fig. 6). In Fig. 6, N represents the number of active inputs. In the case of the nondepressed synapse ($V_{\mathrm{bias}} = 5\,\mathrm{V}$, and it is labelled as NDS in the figure), the average value of the EPSP increased monotonically as the firing rate of postsynaptic neurons increased. The value also increased as N increased. On the other hand, in the case of the depressed synapse ($V_{\mathrm{bias}} = 0.2\,\mathrm{V}$, labelled as DS in the same figure), the EPSP increased nonmonotonically as the firing rate of postsynaptic neurons increased. Now, we define the firing threshold of the IFN as $V_{\mathrm{th}} = 1.8\,\mathrm{V}$. The firing rates when the EPSP exceeded the threshold to the number of active neurons were plotted in Fig. 7 for both depressed (DS) and nondepressed (NDS) synapse circuits. The result indicates that the dependence of the postsynaptic neuron with depressed synapses on presynaptic firing rates is smaller than that of nondepressed synapses.

This difference becomes more apparent when N increases. To confirm it in a large-scale network, SPICE simulation was conducted for the network having 100 synapses. As input, a pulse with pulse amplitude of 1 nA and pulse width of $10\,\mu$s was given. The time constant of postsynaptic neuron was set around 2 ms. The threshold was set at the value of the EPSP produced by 70 active neurons with a firing frequency of 5 kHz. The values of threshold V_{th} were 0.2 V when the depressing synapse was used and 2.0 V when conventional synapse was used. The result is shown in Fig. 8. The firing rate when the EPSP exceeded the threshold to the active neuron for the first time was plotted.

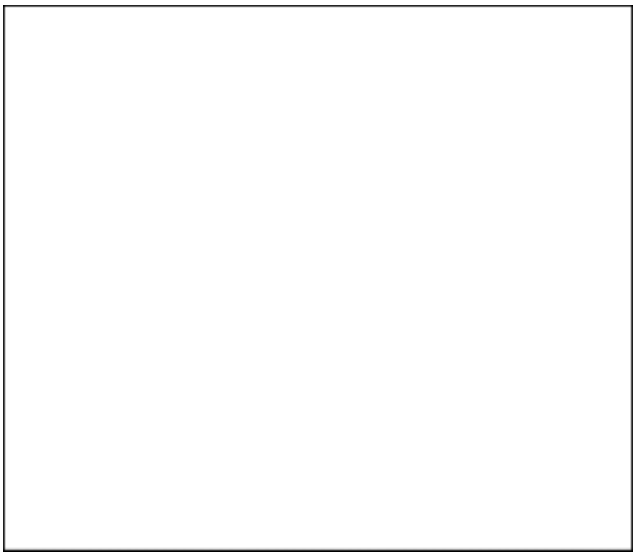

Figure 6. Changes in EPSP of IFN against the number of active presynaptic neurons and their firing rates.

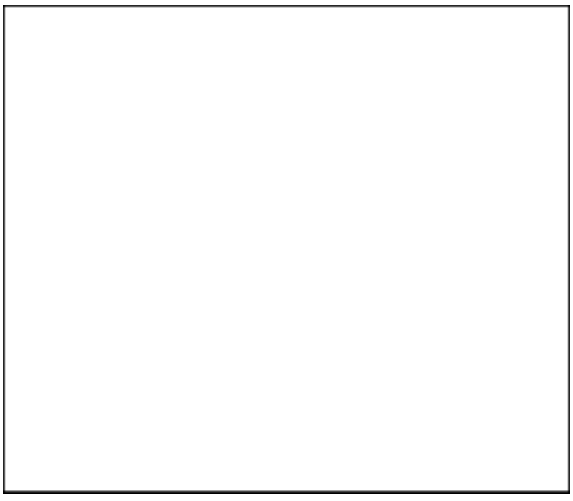

Figure 7. Results for dependence of IFN on the firing rate of presynaptic neurons (4 neurons).

Figure 8. Large-scale simulation results (100 neurons) for same experiments shown in Fig. 7.

3.2 Application to Senn's Neural Network for Synchrony Detection

Senn demonstrated an easy way to extract coherence information among cortical neurons by projecting spike trains through depressing synapses onto a postsynaptic neuron [11]. We demonstrate the extraction of coherent information using our depressing synapse circuits.

Let us consider the same IFN as shown in Fig. 5. We use burst neurons as inputs to the IFN, as in Senn's original work. During a burst input, the output current of the depressing synapse circuit rapidly decreases for successive spikes due to the increase of V_{e} and its slow recovery. But during a nonbursting period, V_{e} has time to be 0, and this results in a strong EPSP at the onset of the next burst. If we compare this dynamic response with that for a nondepressed synapse evoking on average the same EPSP, the depressed synapse will have a larger response at the burst onset and a smaller response toward the end of the bursts.

Fig. 9 shows the response of the EPEP with bursting inputs (a) for a nondepressed synapse (b) and depressed synapse circuit (c). Amplitudes of bursting spike inputs were set at $1\,\mu$A for depressing synapses and 600 pA for nondepressed synapses, which evoked on average the same EPSP (50 mV). This result ensures that the EPSP caused by the depressed synapse circuit has a larger response at the burst onset, as compared with the nondepressed synapse circuit.

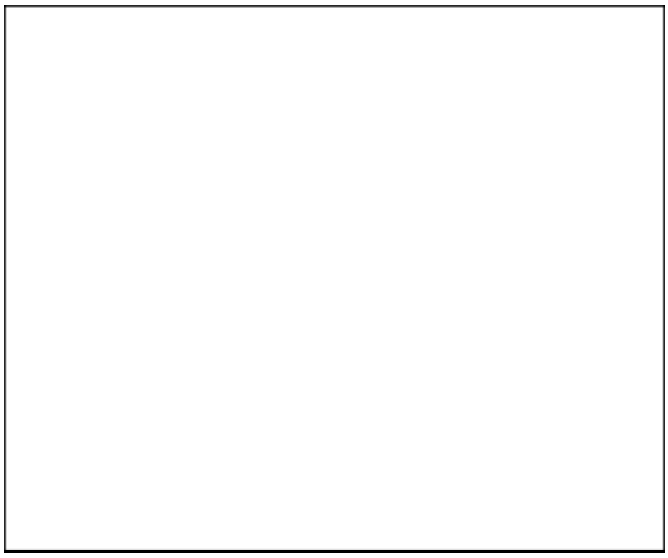

Figure 9. Responses of EPSP for single burst input (a) via nondepressed (b) and depressed synapse circuits (c).

Now we demonstrate that the depressing synapse circuit is able to detect the synchrony during the burst times. We use two bursting neurons as the input of the IFN that receives the burst inputs through depressed or nondepressed synapses. Figs. 10 and 11 show the results. When the input bursts are not synchronized (Figs. 10(a) and (b)), the peak EPSPs evoked by nondepressed (Fig. 10(c)) and depressed synapses (Fig. 10(d)) were both around 0.1 V. But when the input bursts are synchronized (Figs. 11(a) and (b)), the peak EPSP evoked by depressed synapses (Fig. 11(d)) was significantly larger than that of the nondepressed synapses (Fig. 11(c)). Therefore, defining an appropriate threshold $V_{\rm th}$ of the IFN—for example, $V_{\rm th} = 130$ mV in the experiments—the IFN with the depressing synapse circuit can fire when the burst inputs are synchronized.

4. Conclusion

We have designed and fabricated an electronically implemented depressing synapse. The circuit was designed using only five minimum-sized transistors and did not require a capacitor to enable its temporal property. As a result, the circuit took up a total area of $35\,\mu\text{m} \times 36\,\mu\text{m}$ with a 1.5-μm scalable CMOS rule (MOSIS, vendor: AMIS, n-well single-poly double-metal CMOS process). The experimental results indicated that the depressing synapse circuit worked well in an actual environment with realistic configurations, and suggested further potential applications to large-scale spiking neural networks with depressed and nondepressed synapses. With the synapse circuit, we demonstrated two functional neural networks performing contrast-invariant pattern classification and synchrony

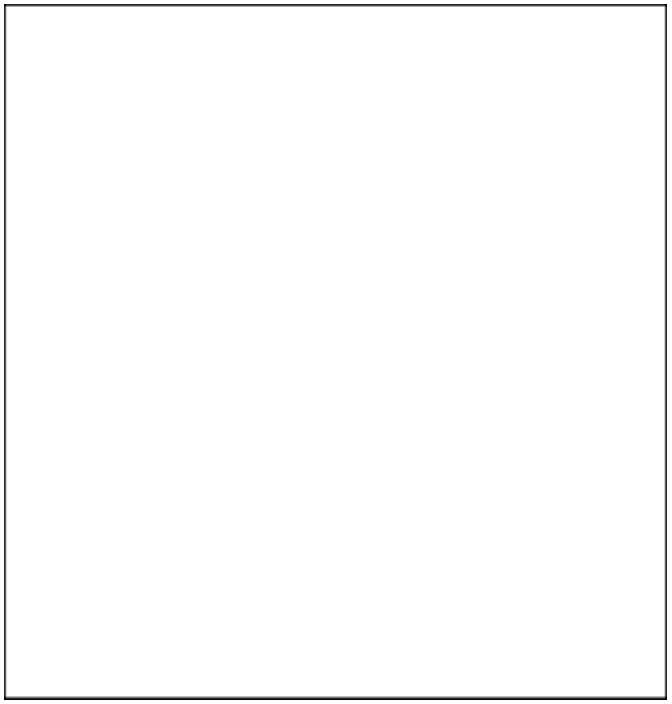

Figure 10. Responses of EPSP for asynchronous burst inputs [(a) and (b)] via nondepressed (c) and depressed synapse circuit (d).

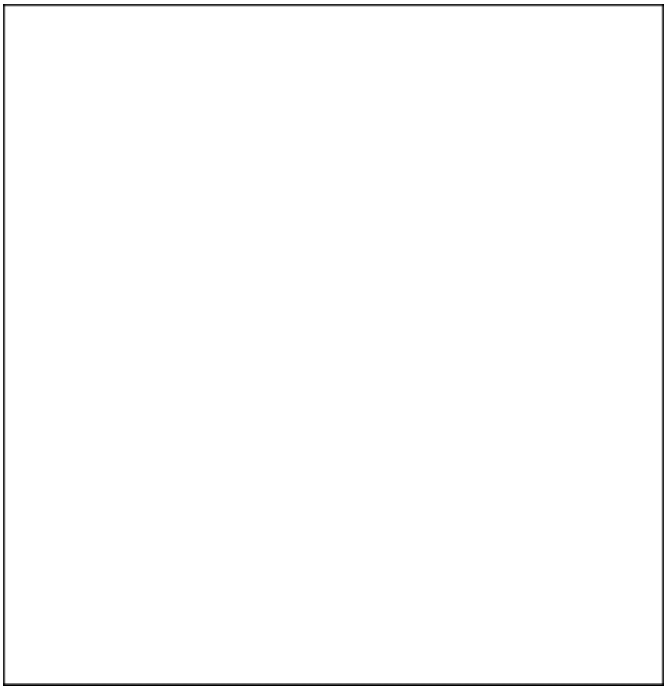

Figure 11. Responses of EPSP for synchronous burst inputs [(a) and (b)] via nondepressed (c) and depressed synapse circuit (d). EPSP evoked by depressing synapse detects synchrony when EPSP $> V_{\rm th}$.

detection using the simulation program with integrated circuit emphasis (SPICE).

Before integrating large-scale spiking neural networks with synapse circuits, we have to consider device mismatches of silicon devices on VLSIs. Namely, if multiple depressing-synapse circuits were implemented on the same wafer, the values of parasitic capacitances might differ from each other. This prevents us from developing applications that require precise matching among CMOS devices. For instance, the two network-level applications (contrast-invariant pattern classification and synchrony detection) are not very tolerant to the variability among CMOS devices. These applications were introduced to "demonstrate" our circuit where the computational function of the circuit was qualitatively equivalent to that of neural models for pattern classification and synchrony detection. However, actual neural systems work very well without such precise matching among neural devices (neurons, synapses, etc.). When this mechanism becomes clear, our subthreshold CMOS circuits certainly will have the advantage of its compactness and low-power dissipation, as compared with conventional neural circuits.

At present, it seems to be too early to use neuromorphic devices for "real" applications (and of course to create its specs) because we do not have "true" neural models that overcome the problem of mismatches between neural tissues for reliable information processing. But attempts to incorporate computational neural models with integrated-circuit engineering may give us possible (but important) cues for designing novel neural circuits and devices, and are thus necessary for developing future neuromorphic VLSIs.

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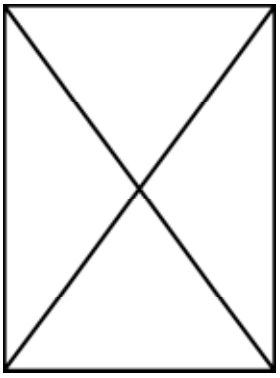
Biographies



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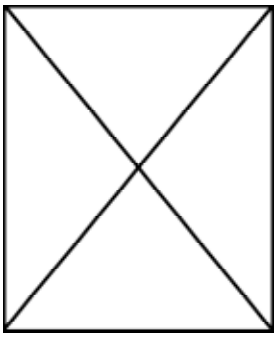

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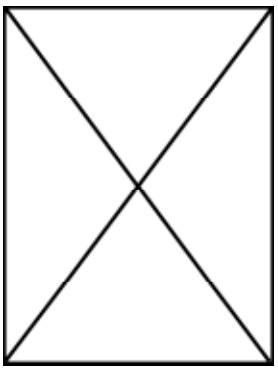

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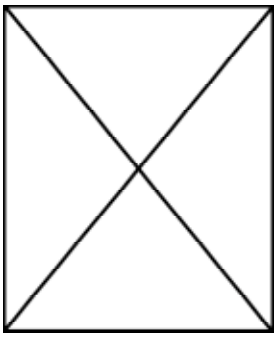
and chaotic systems as well as design and applications of image sensors.



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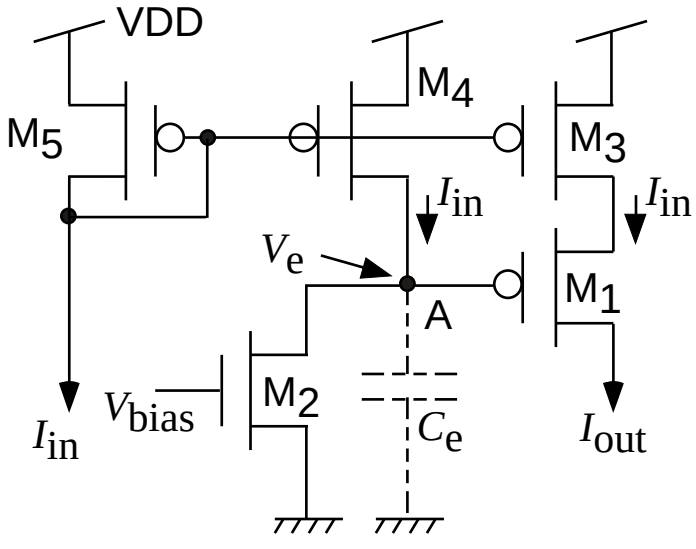

Fig. 1 Depressing synapse circuit that consists of five minimum-sized transistors and a parasitic capacitance.

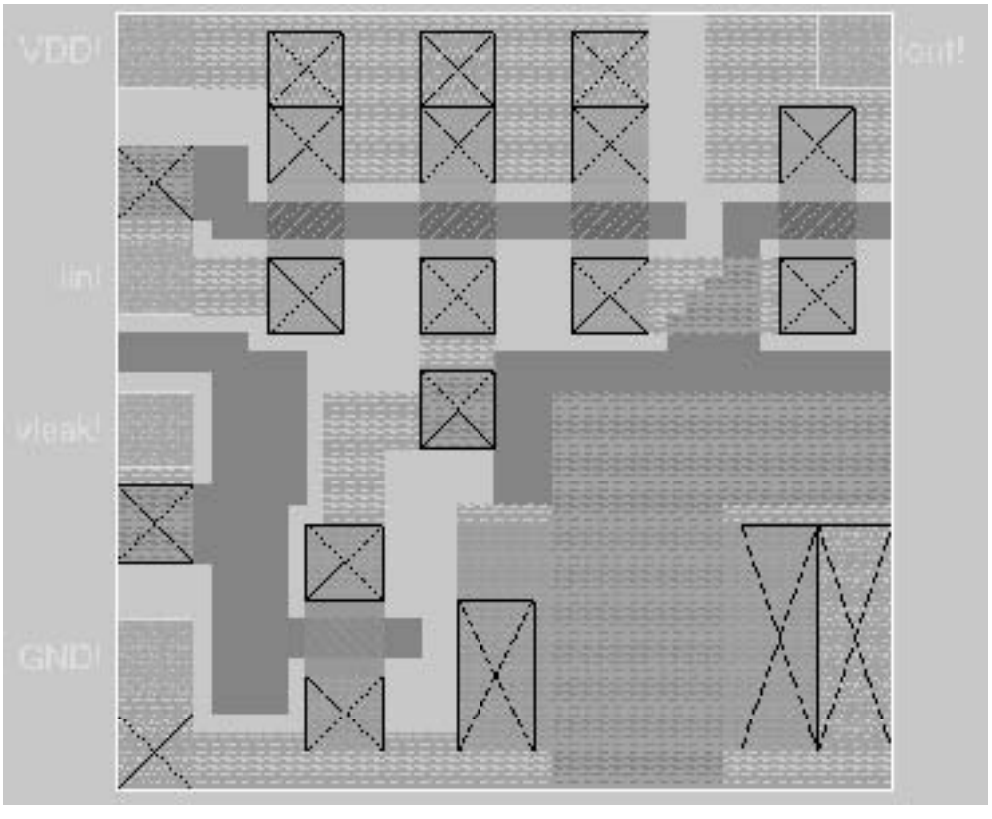

Fig. 2 IC layout of the depressing synapse circuit (a total area of 35 μm x 36 μm with a 1.5-μm scalable CMOS rule).

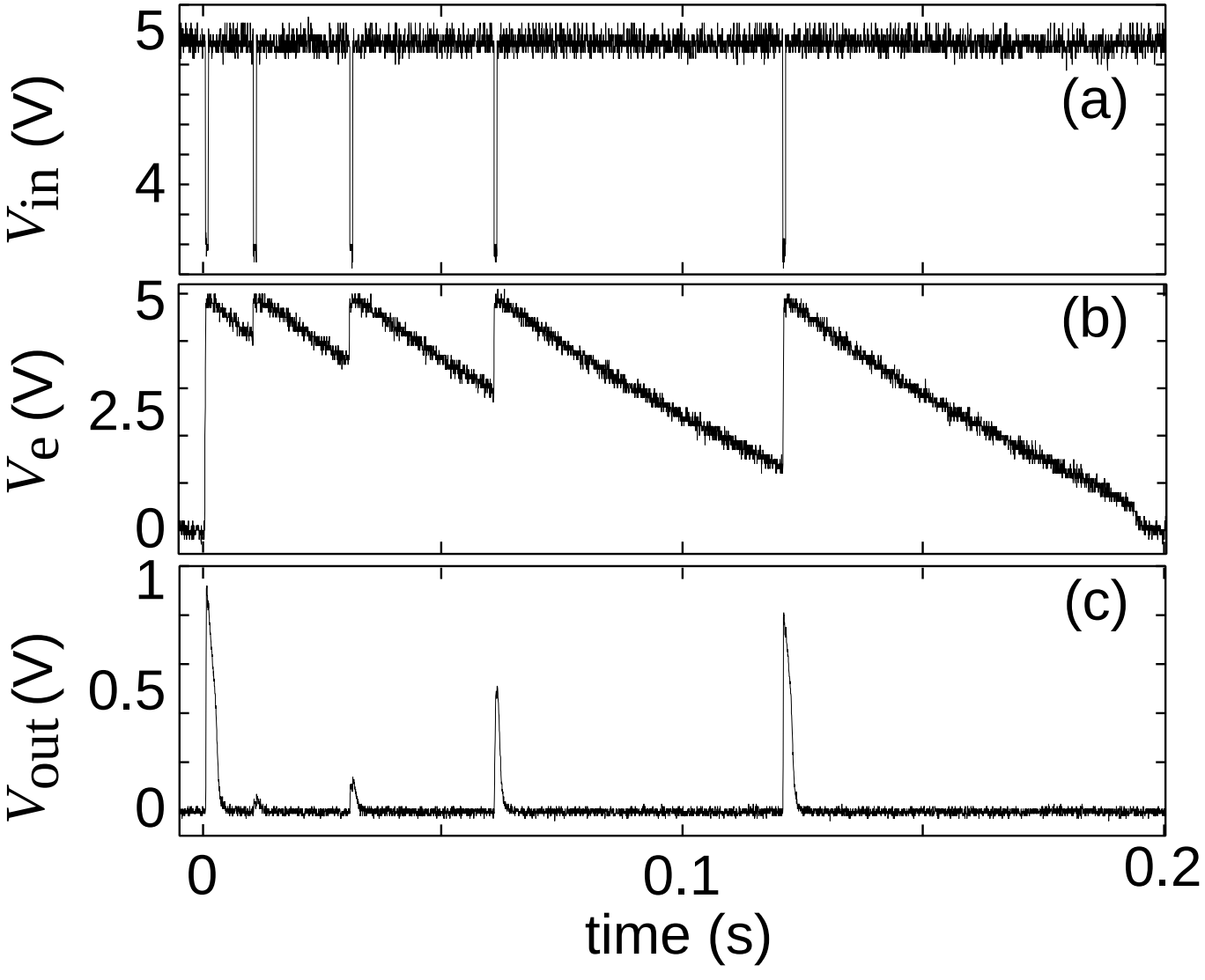

Fig. 3 Experimental results of depressing synapse circuit; (a) successive spike inputs, (b) the degree of synaptic depression, and (c) its outputs.

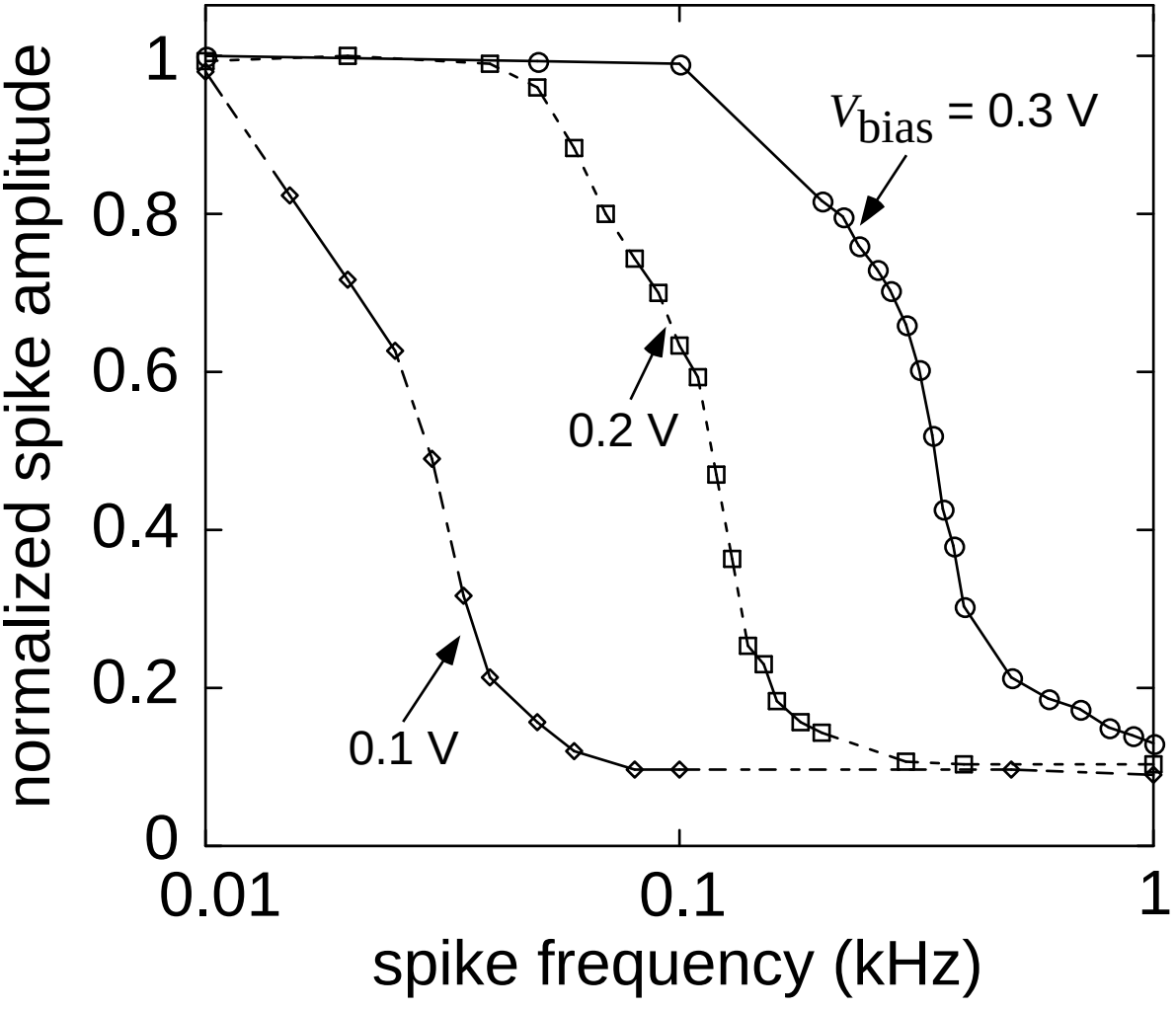

Fig. 4 Changes in amplitude of the output of depressing synapse circuit against the firing rate of presynaptic neuron.

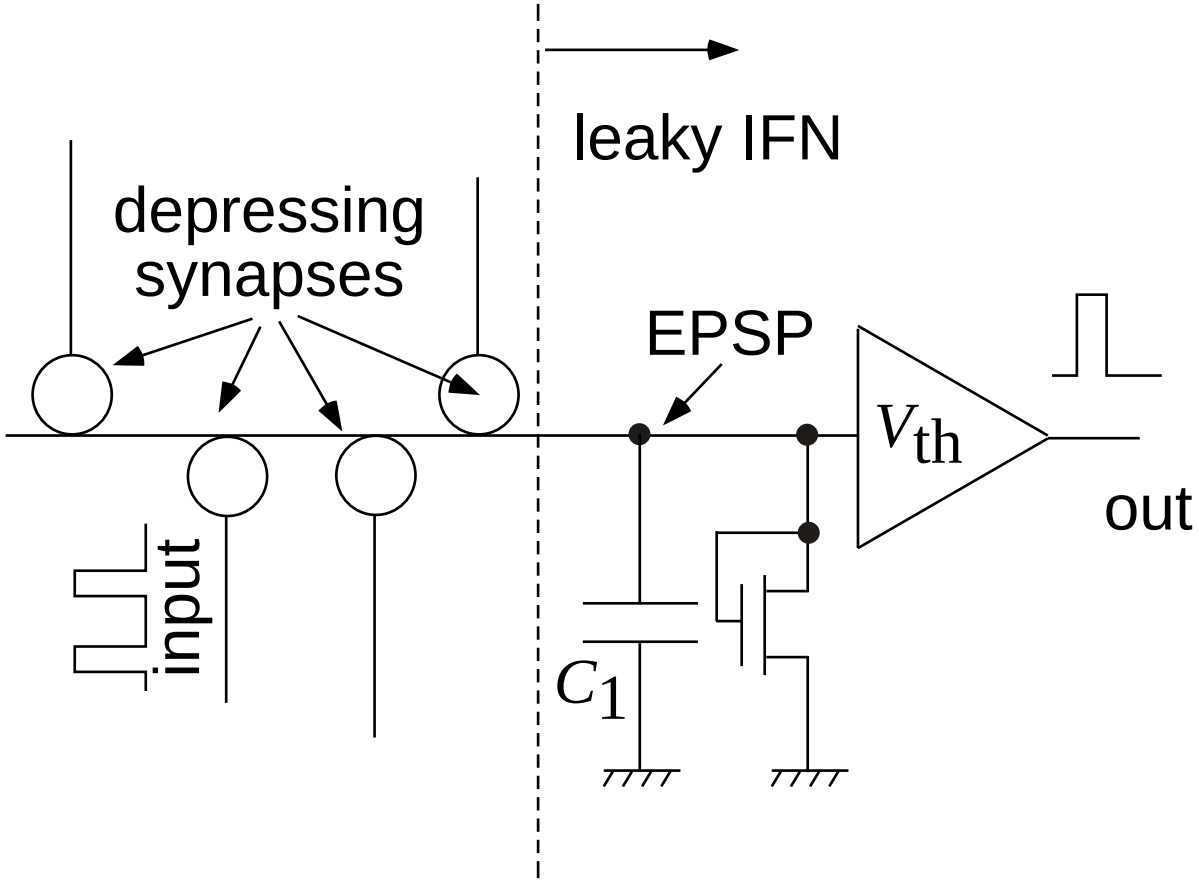

Fig. 5 Experimental setups for pattern classification and synchrony detection.

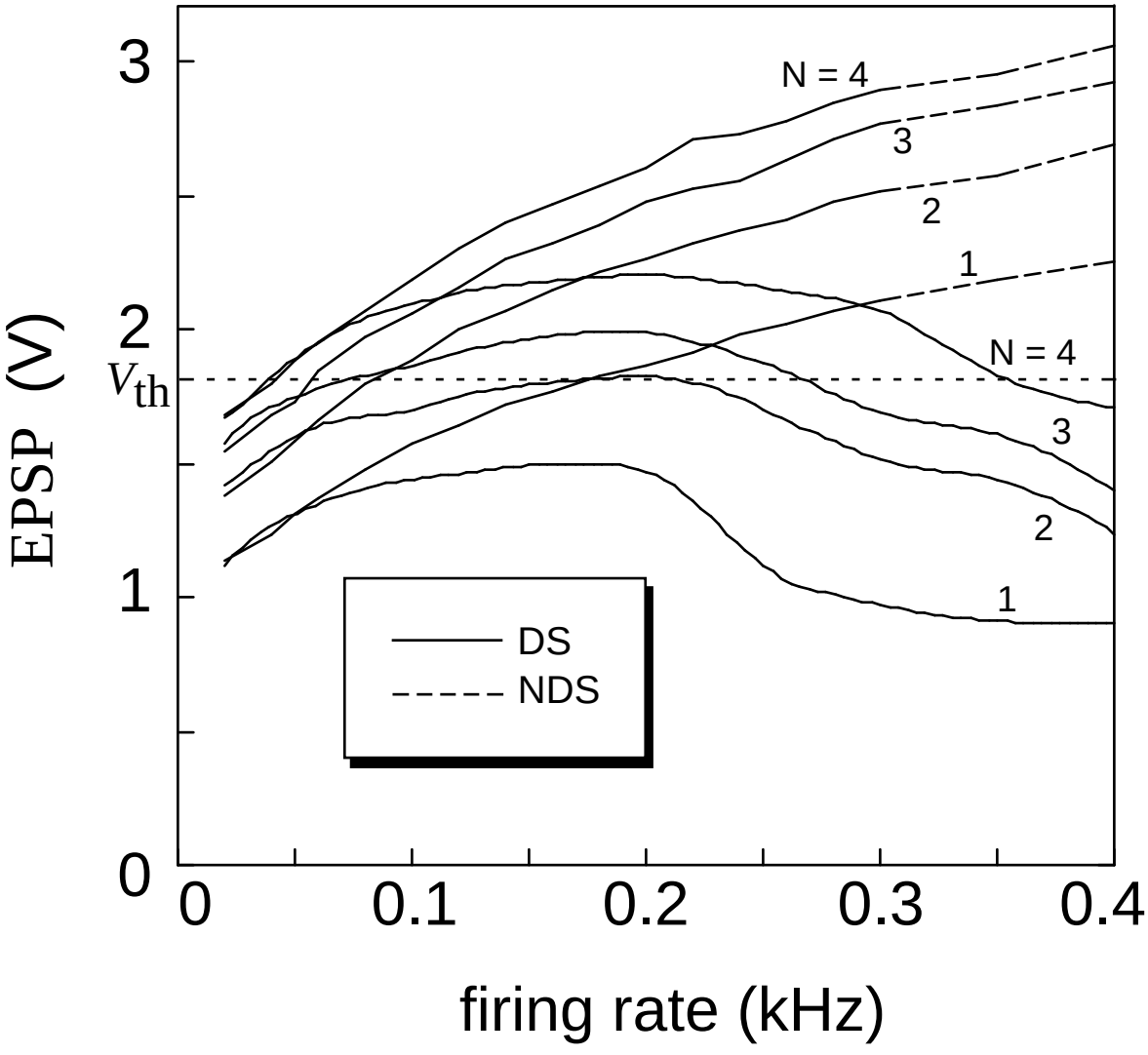

Fig. 6 Changes in EPSP of IFN against the number of active presynaptic neuron and their firing rates.

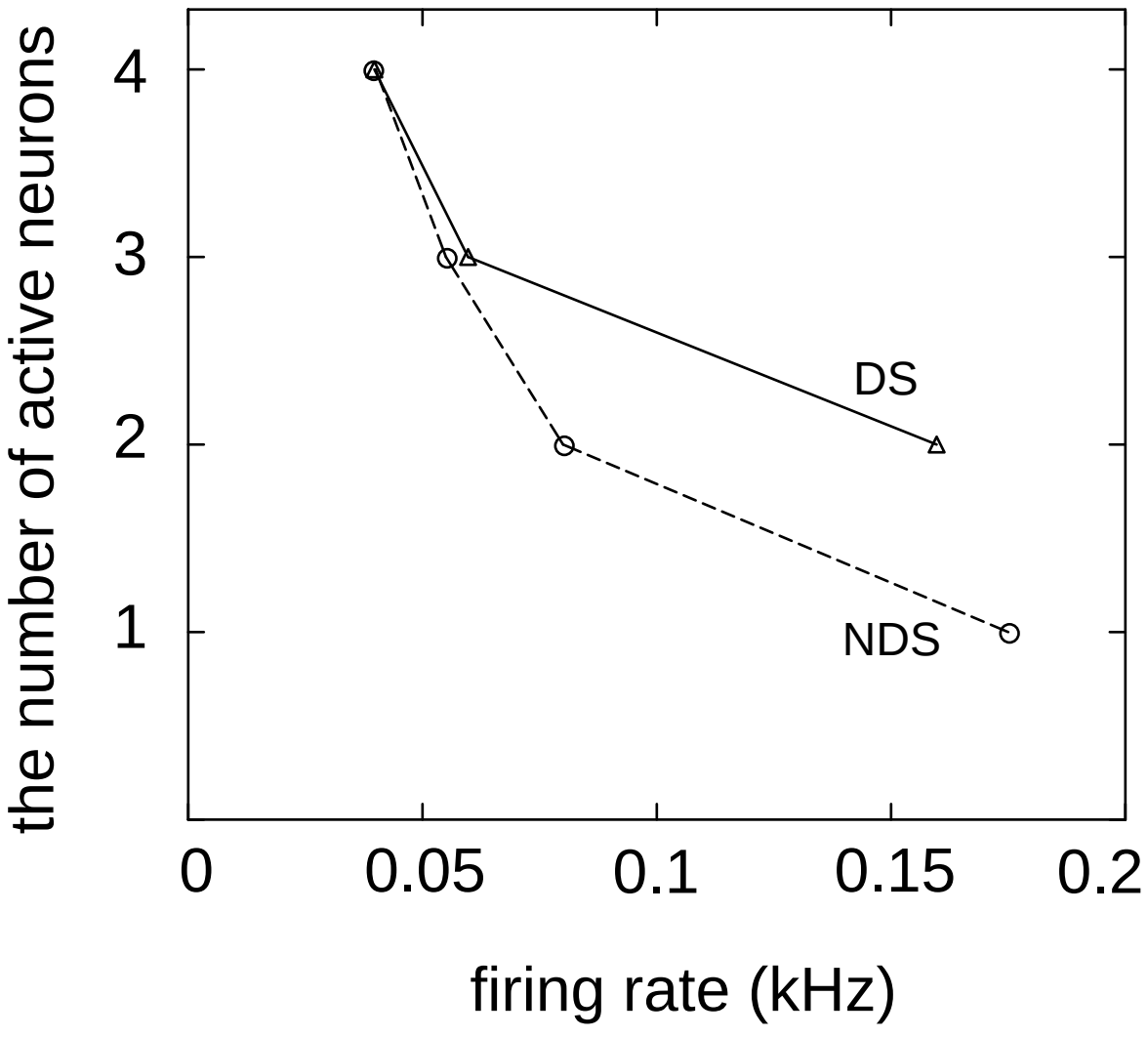

Fig. 7 Results for dependence of IFN on the firing rate of presynaptic neurons (4 neurons).

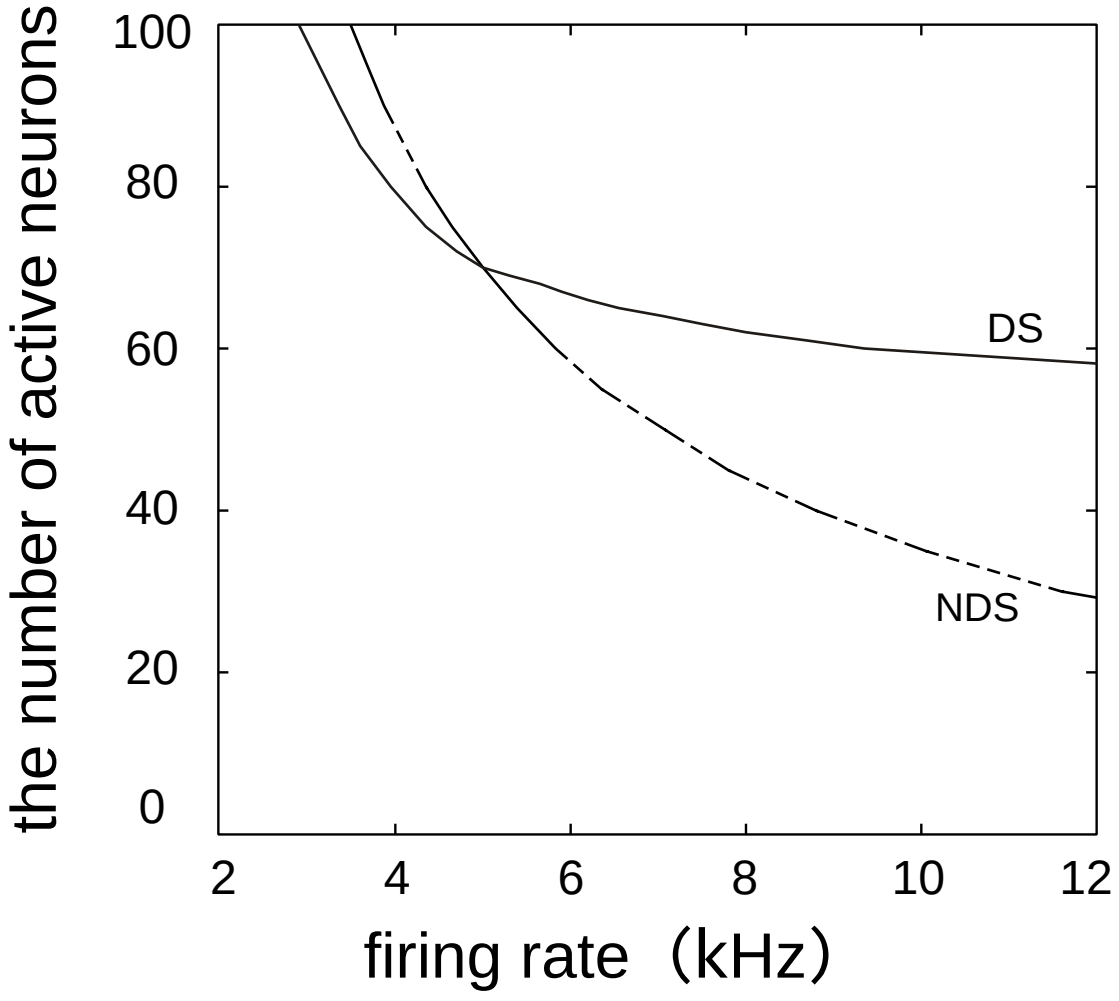

Fig. 8 Large-scale simulation results (100 neurons) for the same experiments shown in Fig. 7.

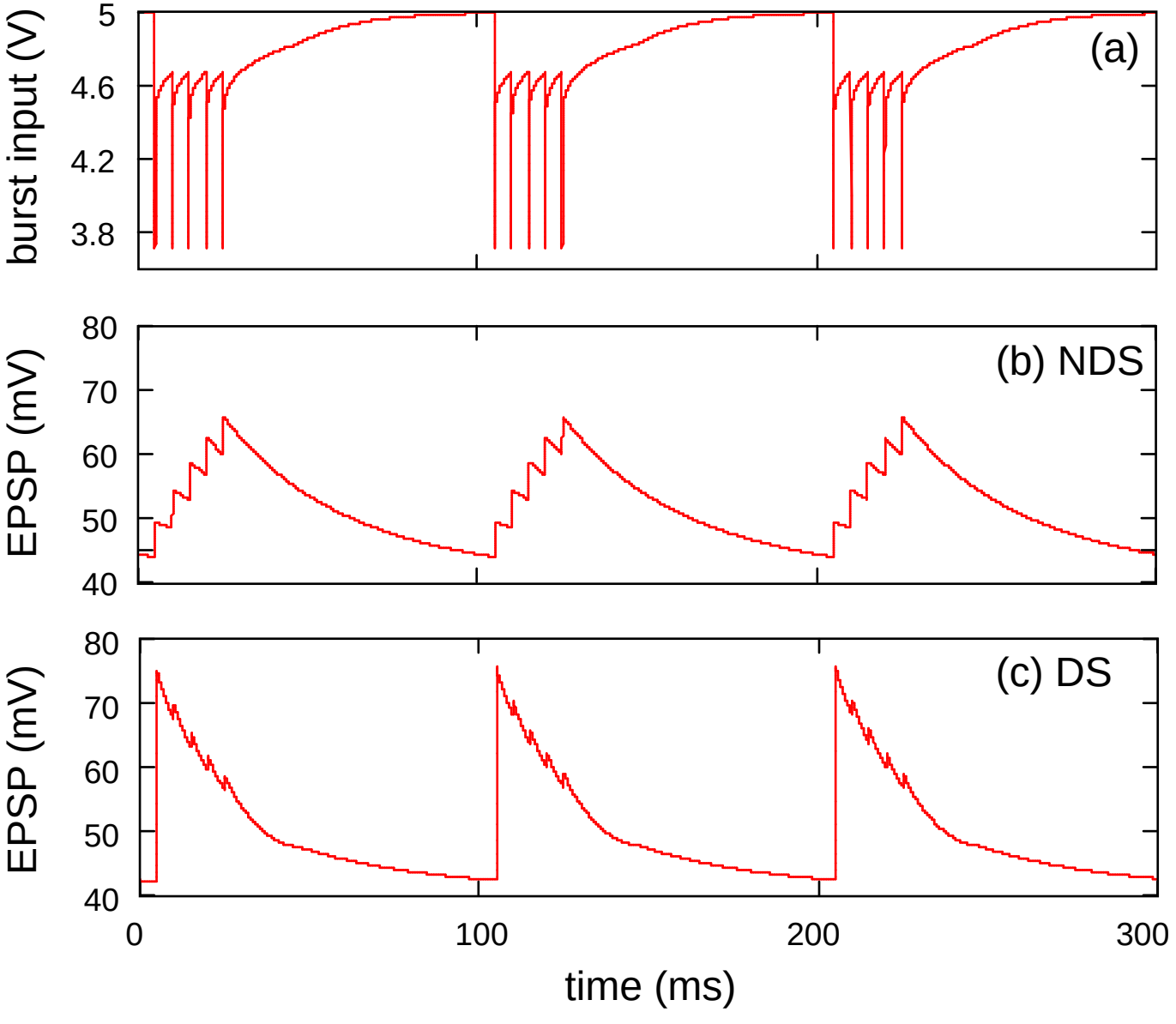

Fig. 9 Responses of EPSP for single burst input (a) via nondepressed (b) and depressed synapse circuit (c).

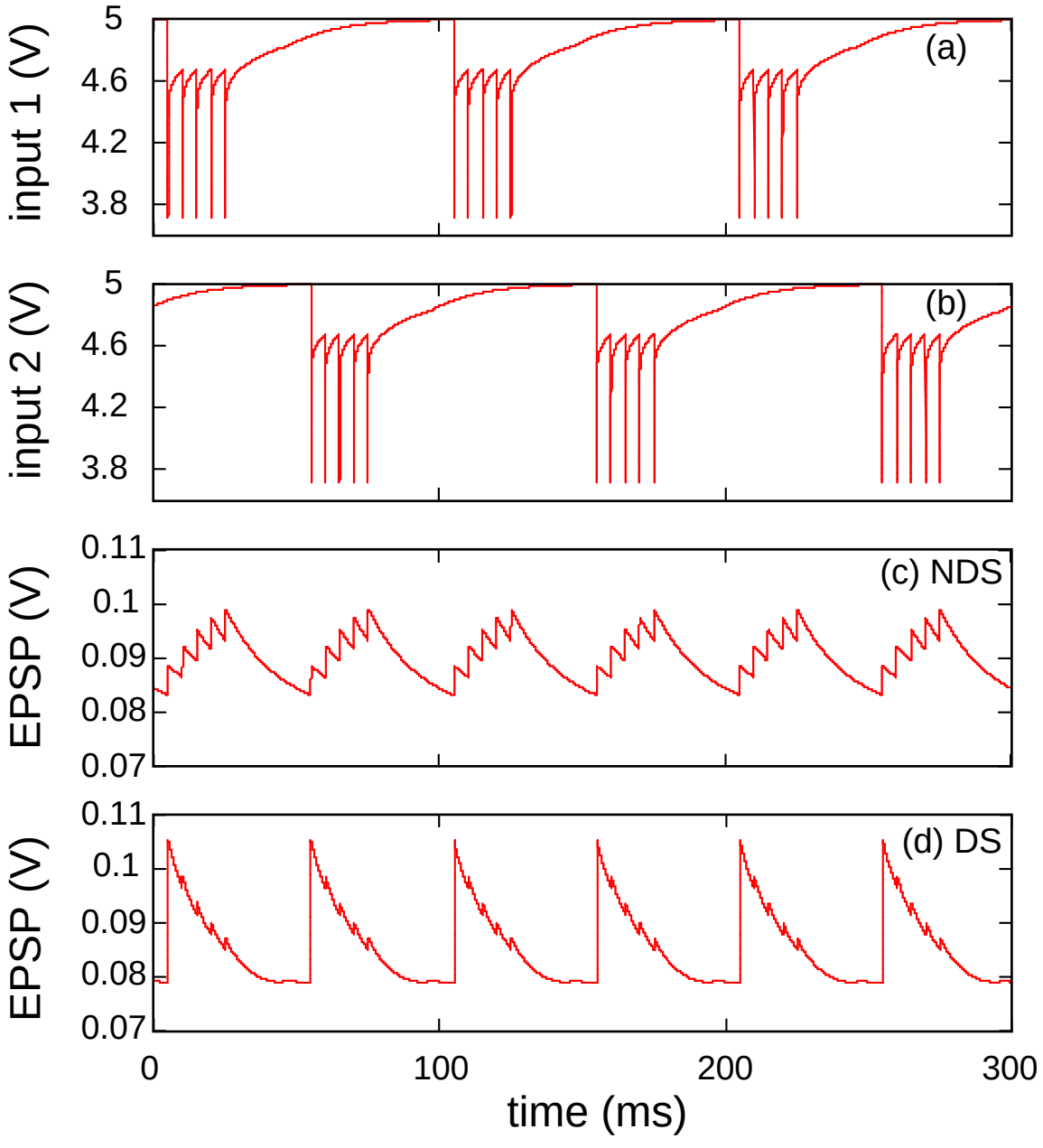

Fig. 10 Responses of EPSP for asynchronous burst inputs [(a) and (b)] via nondepressed (c) and depressed synapse circuit (d).

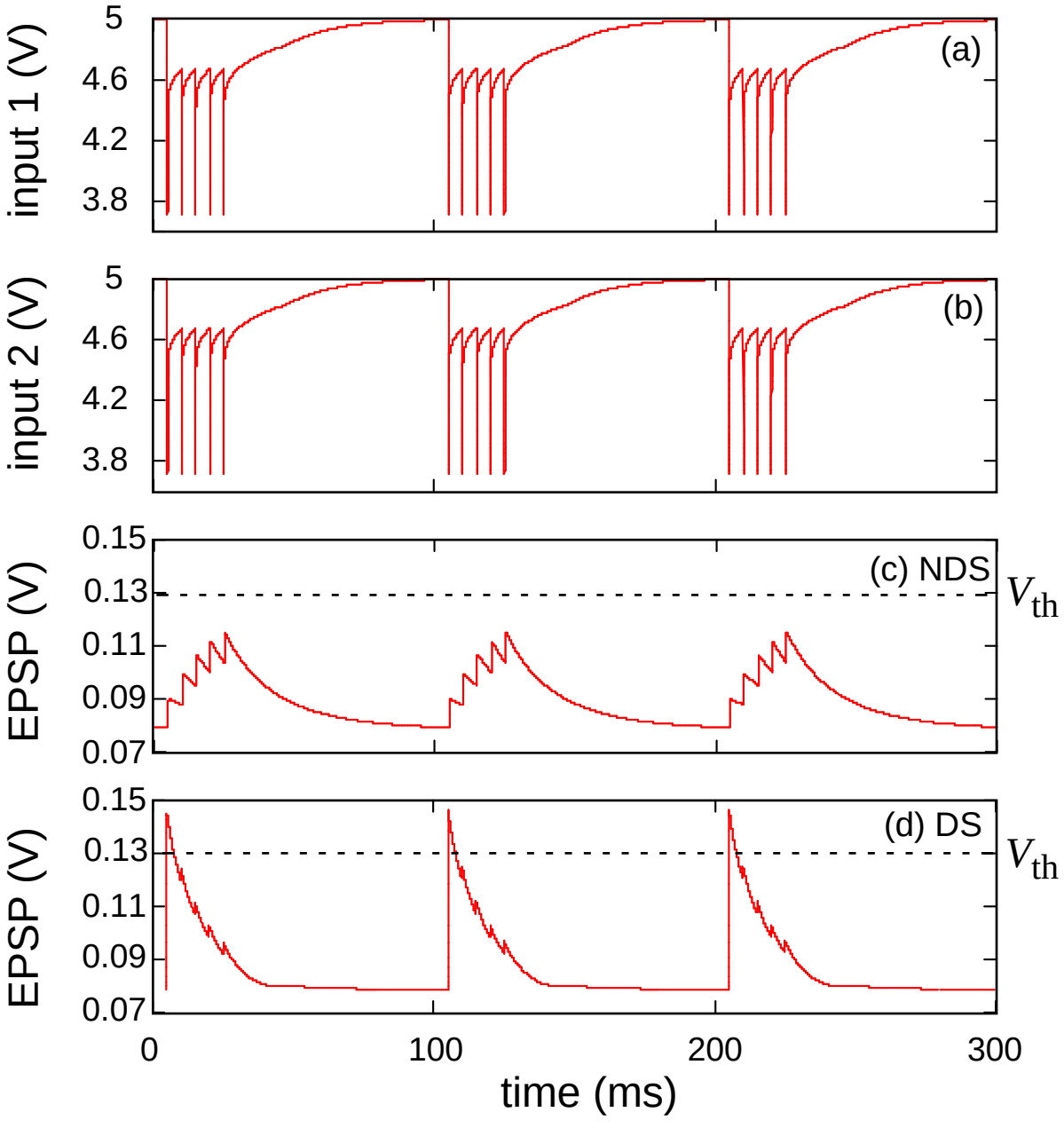

Fig. 11 Responses of EPSP for synchronous burst inputs [(a) and (b)] via nondepressed (c) and depressed synapse circuit (d). The EPSP evoked by the depressing synapse detect the synchrony when EPSP > V_{th}.