

Paper

3D Stacked Imager featuring Inductive Coupling Channels for High Speed/Low-Noise Image Transfer

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Abstract This paper proposes 3D stacked module consisting of image sensor and digital logic dies connected through inductive coupling channels. Evaluation of a prototype module revealed radiation noise from the inductive coils to the image sensor is less than 0.4-LSB range along with ADC code, i.e., negligible. Aiming at high frame rate image sensor/processing module exploiting this attractive off-die interface, we also worked on resolving another throughput-limiter, namely power consuming Time to Digital Converter (TDC) used in column parallel ADCs. Novel intermittent TDC operation scheme presented in this paper can reduce its power dissipation 57% from conventional ones.

Keywords: 3D-stacked imager, Through Chip Interface (TCI), Radiation noise, Single-Slope ADC, Time to Digital Converter (TDC), Intermittent operation.

1. Introduction

Stacking image sensor and digital logic dies are getting wide attractions for 1) reducing image sensor die area, 2) optimizing sensor/logic fabrication process through functional separation, and 3) achieving faster image transfer (more than 1,000 fps) needed for smarter image processing. Thus the development of the 3D stacked imagers with these features is much useful for realizing interesting applications such as computational imaging and intelligent camera modules.

Unlike conventional approaches using Through Silicon Vias (TSV), the paper proposes stacking the dies using parallel inductive coupling channels with vertically aligned coils, called Through Chip Interfaces (TCI), for achieving better cost, manufacturability, and energy consumption[1]. Although there are a lot of researches of 3D stacked chips using TCI for various applications, this study is first trial of applying TCI to 3D stacked imagers. Figure 1 explains our 3D module concept. Since a single TCI can achieve more than

4Gbps throughput[1], top/bottom rows of TCIs operating in parallel can resolve bandwidth bottleneck in achieving 1,000 fps and higher inter-chip image transfer. In this study, we have test-cased single-TCI-domain image sensor/digital logic into one die, and then stacked two of them with half-die-size pitch shifted. Since high-speed data transfer are realized using TCI with inductive coupling. The imager also performs high-speed image capturing. Power consumption increases in fast circuit operation. Thus, the power management becomes much important. Obviously, evaluation of TCI noise is the most important. Because the TCI has the radiation noise.

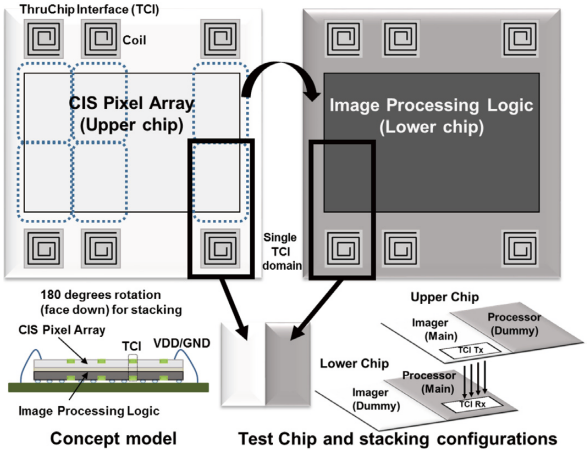

Fig.1 Imager/logic 3D stacked module concept.

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One of major contributions of this paper is to show there is actually no TCI-oriented radiation noise observed on an image sensor, allowing them to be placed near the pixel read circuits. As our goal is to commoditize high speed image transfer by using TCI, we have also developed new column ADCs which can substantially enhance energy-efficient parallel column readability.

This paper organized as follows. Section 2 describes the 3D-Stacked Imager with the TCI. The details and analysis of the Single-slope ADC (SS-ADC) with the intermittent-working TDC for low-power use are presented in Section 3. In section 4 experimental results of TCI-radiation-noise characteristics are demonstrated.

2. Proto-type Chip for 3D-Stacked Imager

Figure 2 shows a micro-photograph of our fabricated chip using 0.18-μm 1P4M CMOS image sensor process. In the test chip, we cut out a part of imager/processing logic and combined them to single die. Using the two dies, we made the prototype 3D stacked module, where the upper die was shifted with half-size pitch and then the imager side of the upper die was stacked on the processor side of the lower one. Other-side circuits were dummies in this stacking.

The left half (Tx side) of the die consists of an image sensor, an asynchronous parallel to serial converter (P2S) that serializes 12-bit parallel pixel data with two-extra bits (start and stop bits), and a TCI-Tx. In the right half (Rx side), the received serial data at TCI-Rx are converted into parallel 12-bit pixel data by an asynchronous Serial to Parallel Converter (S2P). The TCI-Tx includes two sets of coils/drivers (TCI Tx cir) for transferring a pair of data and clock, whereas the TCI-Rx includes a corresponding set of coils/amplifiers (TCI Rx cir). In addition to these pairs of Tx/Rx, 9 coils and drivers/amplifiers were placed just beneath the image sensor (350/280/170 μm coils x 150/120/120 μm distance, see also Fig.9, top right), in order for evaluating potential-radiation-noise interference from TCI circuits to the image sensor.

3. Energy-Efficient Single-Slope ADC

A 3D-stacked imager using TCI realizes high-speed data transfer and corresponds to high-speed image capturing, so, the power management becomes much important. Single-slope ADCs (SS-ADCs) with a Time-to-Digital Converter (TDC) have been proposed for high-speed SS-ADC[2)3)4)].

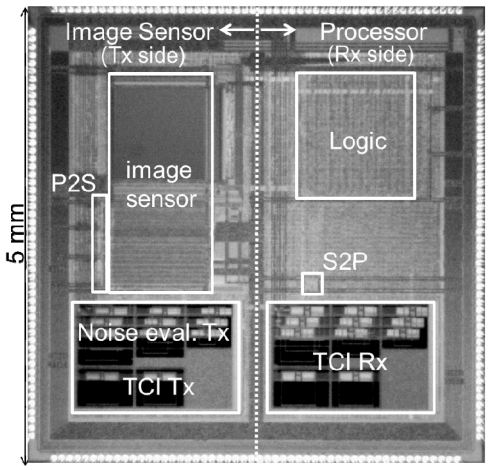

Fig.2 Micro-photograph of proto-type chip for 3D-Stacked imager with TCIs.

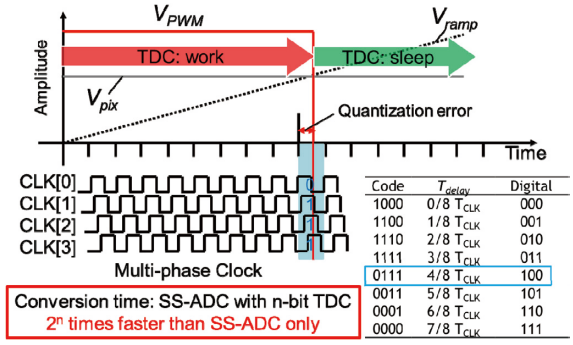

Fig.3 Operation scheme of SS-ADC with TDC.

Figure 3 shows the operation of the ADC with TDC. This circuit operates coarse and fine A/D conversions. When V_{PIX} and V_{RAMP} are given to the comparator, the SS-ADC starts coarse ADC and the counter outputs upper bits. Then, the comparator generates a quantization error between the PWM signal V_{PWM} and clock signal. The quantization error is given to the TDC and digitized as lower bits, so the fine A/D conversion is done. The code shows the time shift of the multi-phase clock (CLK [0:3]). The TDC measures the quantization error of the SS-ADC within one clock period. Applying a TDC with n-bits resolution to the SS-ADC, the conversion time is reduced by a factor of 2^n. Therefore, the SS-ADC with TDC can operate faster without high-speed clock signals.

Conventional TDCs need to run continuously, where numbers of delay cells and D-FFs being driven by a high speed multi-phase clock, in order to keep the consistency between the stages of the ADC operation and to maintain robustness against meta-stability. This results in high power consumption which becomes a limiter when applying TDC to column-parallel pixel read

circuits for achieving higher frame rate. We propose an intermittent TDC operation scheme that can reduce its power dissipation drastically. The TDC runs continuously until the PWM signal of the SS-ADC falls. A "high" period of the PWM signal is defined as T_{PWM}. Here, we focus on the timing of the T_{PWM} falling edge and consider the delay signal, $T_{PWM} + \Delta T_{PWM}$, which is generated from T_{PWM} through normal delay cells. Then, we can make a time window ΔT_{PWM} and restrict the TDC to work only in this period.

3.1 Proposed single-slope ADC with TDC

Figure 4 shows block diagram of our SS-ADC with TDC configuration and the detail circuit compositions of them. It has two stages. The first is a TDC with multi-phase clock signals, a number of D-FFs and an encoder. The second is a SS-ADC with a ripple counter and a comparator using the differential amplifier. The encoder is based on a ripple counter, this circuit counts number of the state "1" or "0" of the TDC code along with the MSB of the code; the TDC receives multi-phase clocks signals CLK [0:3], stores them to the latches in parallel and then outputs the data sequentially by the addressing using TDC_address[0:8]. The NAND gates applied to the phase interpolator which converts the 4-channel multi-phase clock signals to the 8-chnannel for the TDC redundancy. The Schmitt trigger, the inverter chain (ΔT_{PWM}) and also the NAND gates are used for the intermittent-working-TDC scheme.

In the combined usage of the SS-ADC and the TDC, special care should be taken with the consistency between the TDC and the counter. By 'consistency' we mean that the lower bits (TDC output) have to be coupled with the upper bits (counter output). In other words, the settled TDC state completely decides the counter state with synchronization. Generally, the shared clock is given to a TDC and a counter for the consistency. However, when the falling edge of the stop signal (comparator output) is close to the clock signal timing, meta-stability occurs and these circuits work at individual timings, so even using a shared clock, the consistency degrades due to the meta-stability. Delay adjust cannot fundamentally handle the meta-stability, either. Exact consistency is important for robustness against meta-stability.

Figure 5 shows consistency managing of our synchronized TDC. Only a master clock without phase shift is used for the counter operation through the first D-FF of the TDC (signal A). In this configuration, the settled state of the signal A completely holds the counter

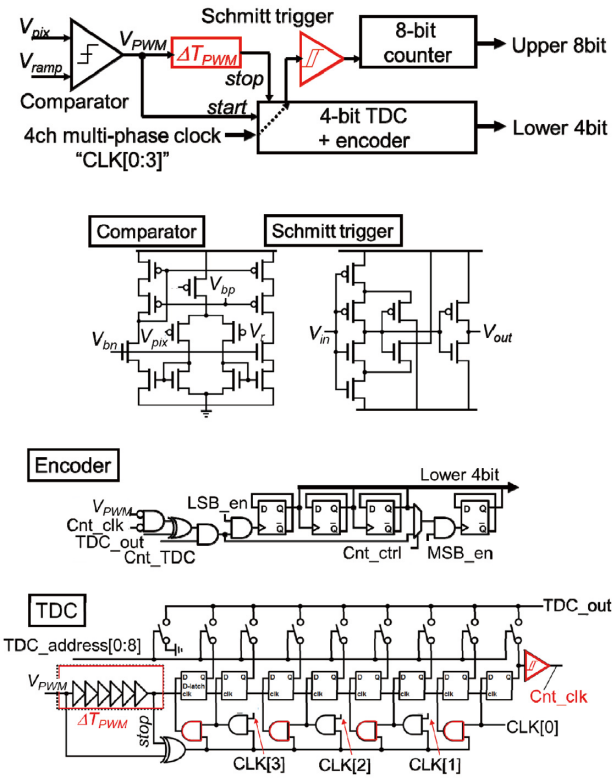

Fig.4 Block diagram and detail circuits composition of proposed column ADC.

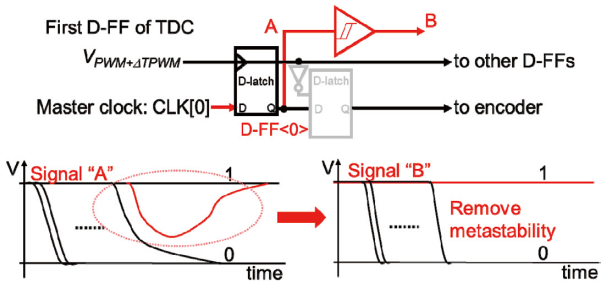

Fig.5 Managing of consistency between SS-ADC and TDC.

state. Consistency between the TDC and the counter can be achieved by using this scheme. However, when the PWM signal is close to the clock signal, meta-stability occurs on the signal A and miscodes may be generated. We therefore applied the Schmitt trigger between the TDC and the counter to remove the meta-stability of the signal A. Using the signal B through the Schmitt trigger, we obtain exact consistency/synchronization between the TDC and the counter. A stand-alone SS-ADC with a delay-line TDC was proposed for low voltage use[5]. An additional circuit was required for avoiding meta-stability. Moreover, since there is no consistency between the ADC and the TDC, digital calibration was also needed.

3.2 Intermittent working TDC

A SS-ADC with multi-phase clock TDC can reduce the number of operation cycles and keep consistency between the ADC and TDC. However, continuous work of the multi-phase clock TDC is required for the consistency between the ADC stages. Multi-phase clock signals are the fastest switching signals in the ADC with TDC, which are input on each inverter-delay cell and each D-FF, and they alternately switch the numbers "high" or "low" continuously. The major factors in power consumption are the supply of switched signals to these circuits and ensuring that these signals operate continuously[5)6)]. Therefore the TDC consumes too much power with the multi-phase clock signal, so it is difficult to allow for flexibility in the resolution of the TDC. To increase the resolution, it is necessary to reduce power consumption. Here, we focus on the delay cells, generating the multi-phase clock signals, and propose an intermittent TDC operation scheme. This technique can reduce power dissipation drastically.

Figure 6 shows the proposed intermittent operation. The previous TDC configuration operates continuously until the PWM signal falls (See also Fig. 3). A "high" period of the PWM signal is defined as T_{PWM}. Here, we focus on the timing of the T_{PWM} falling edge and consider the delay signal, $T_{PWM} + \Delta T_{PWM}$, which is generated from T_{PWM} through a delay signal and an enable generator composed of normal inverter chain. Then, we can make a time window signal ENABLE and restrict the TDC working during ΔT_{PWM}. In other words, we can achieve intermittent TDC operation using the time window ΔT_{PWM}. Also, as shown in figure 4, the enable signal is given to each NAND delay cell. The delay cells operate the same as the inverter only when the enable signal is "high." The delay cells output multi-phase clock signals in the period of ΔT_{PWM} and supply them to the D-FFs. Except in the ΔT_{PWM}, the output signals of the delay cells and D-latch in the D-FFs are not switched. This operation time is much shorter than that of the conventional TDC. In this architecture, the SS-ADC digitizes the period of $T_{PWM} + \Delta T_{PWM}$, so the output code of the ADC has some value that is offset along to ΔT_{PWM}. The offset can be removed by digital CDS. The power dissipation of the TDC works only for a short period, so we can set the resolution of the TDC higher and realize a faster A/D conversion rate in the SS-ADC stage. In this study, we applied the 4-bit resolution to the TDC.

4. Experimental results

4.1 Experimental setup

Figure 7 shows an experimental setup for the 3D stacked module. The test board was controlled by a Xilinx Kintex-7 FPGA board through FMC connectors. Fig. 8 shows measured characteristics of sensor side. The ADC has 11-bit resolution with 1-bit redundancy. The Differential Non-Linearity (DNL) is +0.26/-0.23 LSB, and the Integral Non-Linearity (INL) is +7.5/-14.5 LSB. Degradation of the INL is caused by non-linearity of the ramp-wave generator. We also confirmed image capturing with 3ms exposure (in Fig. 8) and correct TCI

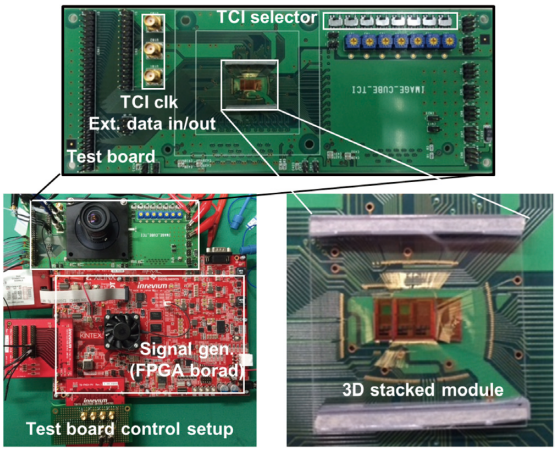

Fig.7 Prototype board of 3D stacked module with TCI.

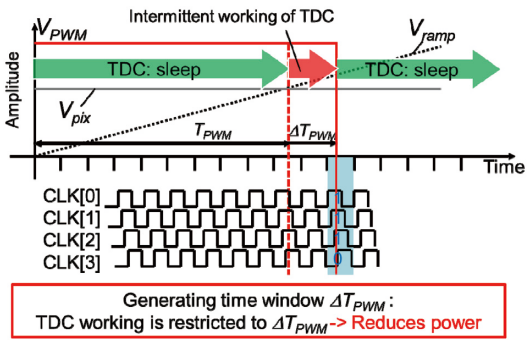

Fig.6 Intermittent operation of TDC.

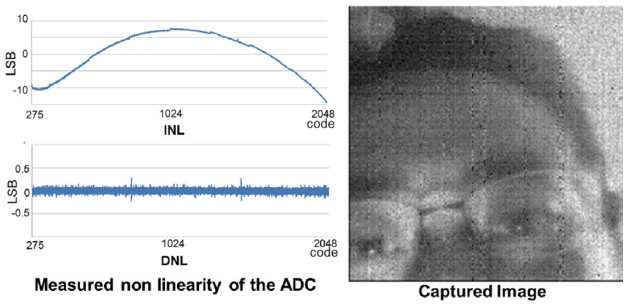

Fig.8 Measured characteristics of sensor side.

Table 1 The details of the upload contents and the input items.

Process	0.18-μm CMOS 1P4M
Pixel pitch, res.	5μm, 200x200
Voltage supply	3.3V(analog) /1.8V to 1.3V(digital)
ADC, TDC res.	11 bits (+ 1 bit), 625ps
Sampling rate	200kS/s@100MHz
ADC power VDDD=1.8V	108 μW/col. (This work) 247 μW/col.(Normal SSADC+TDC)*
ADC power VDDD=1.3V	71 μW/col. (This work) 141μW/col.(Normal SSADC+TDC)*
DNL, INL	+0.26/-0.23, +7.6/-14.5

*Ref. [3][4] do not address power consumption of their column circuits.

Table 2 Comparison with other types of the SS-ADC.

Reference	[6]	[7]	This work
Process	0.25-μm	0.18-μm	0.18-μm
Architecture	Multiple ramp single-slope	Two step single-slope	Single-slope + TDC
Resolution	10-bit	12-bit	11-bit + 1bit
Conversion time	16 μs	36 μs	5 μs
Column power	95 μW	128 μW	108 μW

communication in the 3D stacked module. Measured Bit Error Rate (BER) was less than 10^{-12} at 100 Mbps using 2^7-1 Pseudo-Random Bit Sequence (PRBS) data. Table 1 summarizes the chip characteristics. The ADC parts achieved 57% reduction of power dissipation from the conventional architecture[2)3)4)]. Table 2 lists comparison with other types of the SS-ADC.

For the noise evaluation of the TCI, we designed three sizes of coils and placed 9 coils with 150/120 μm pitch from the top to the bottom. The column ADCs No. 24, 76, 194 are the nearest column ADCs from the large, middle and small-sized coils. And we prepared two types of boards, which were main- and sub board. Figure 9 shows the geometry of the TCI coils and its 3D stacking. The main board, which was normal set up, was used for image transfer to the lower chip through TCI transmitter. So the transmitter works as in-plain noise generator. In the other hand, the sub board, it was artificial setup. The TCI transmitter works only noise generator and it was placed just below the analog amps of the column ADC. The column ADCs No. 66 is the nearest column ADCs from the large-sized coil in this configuration. Using these boards, we evaluated the TCI noise interference. In the noise evaluation, we supplied pseudorandom noise, which was synchronized to A/D-conversion timing, to only one selected TCI and measured LSB shift of the ADC code from the selected column ADC. Since the noise sequence is same in the SS-ADC period, the noise component doesn't disappear

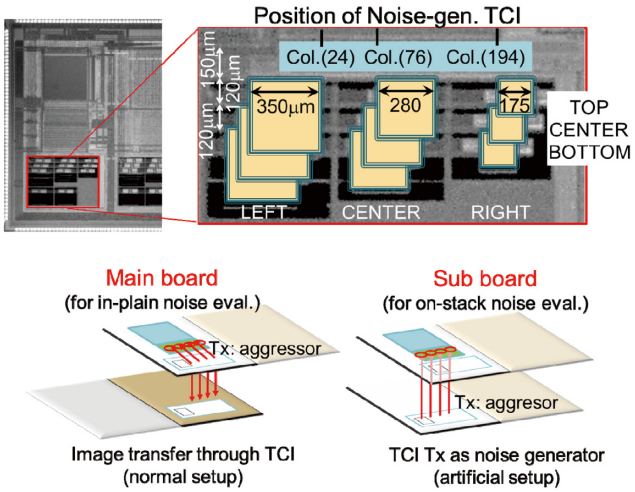

Fig.9 TCI coils geometry and 3D stacking.

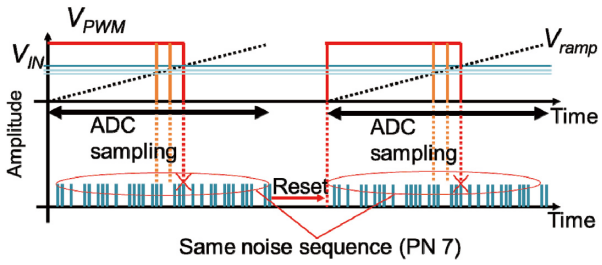

Fig.10 TCI radiation noise evaluation.

through averaging (in Fig. 10). We obtained 16, 384 samples and averaged at each noise-interference measurements. Since radiation noise decreases in proportion to the cube of the distance[8)], the interference component should have dependencies on ADC-code, as well as coil locations (TOP / CENTER / BOTTOM). Figure 11 and 12 show measured TCI-radiation-noise characteristics. Although the 35-LSB-range interference was observed using artificial setup, less than the in-plain noise evaluation. Also, measured results show no such dependencies, meaning no radiation noise interference detected. In the normal setup, receiving sensitivity of TCI-Rx is important. Communication of TCI with coil-diameter D tolerates stacking shift from D/2 to D/3[8)9)]. Thus, managing the coil pitch, the stacking precision can be relaxed with considering radiation noise from the neighboring TCI channel. Approximately -3 LSB offsets was observed, however, compared with the TCI noise-free condition. We consider this offset is caused by minute IR drops which should have been solved by better power line design.

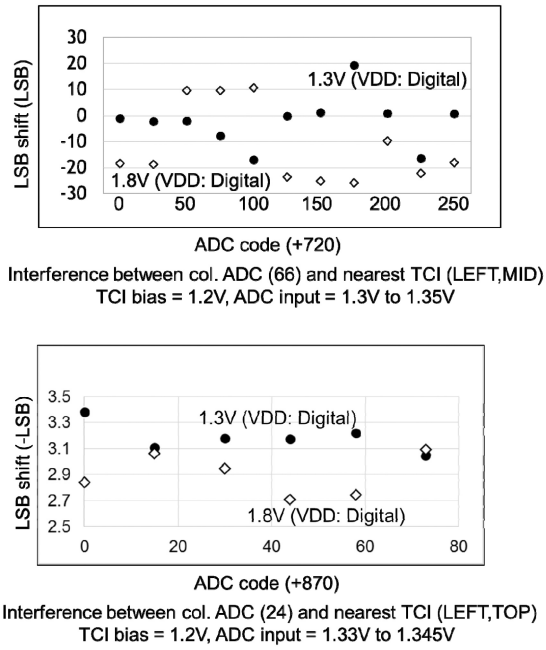

Fig.11 TCI radiation noise evaluation (dependencies on ADC-code).

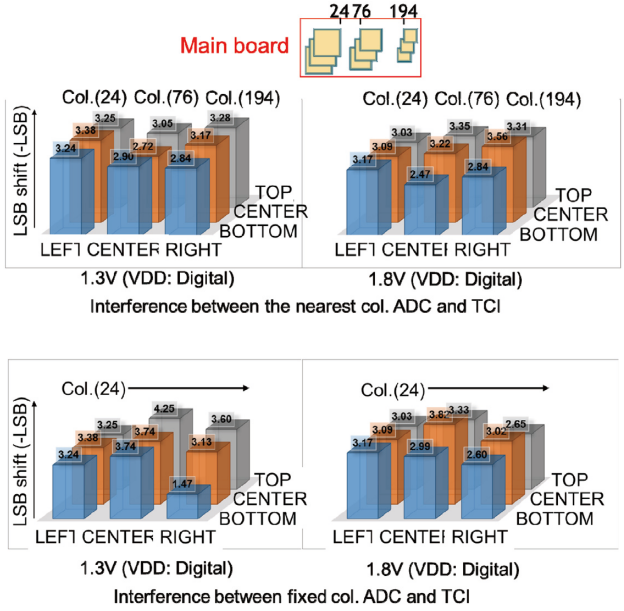

Fig.12 TCI radiation noise evaluation (dependencies on coil locations).

5. Conclusion

In the 3D stacked imager module featuring TCI, radiation-noise dependencies were not observed using in-plain noise evaluation. It indicated that the presented geometry was one of the possible configuration for low-noise image transfer by using TCIs, and will be valuable for subsequent design of 3D-stacked imager/logic modules featuring TCIs. Combining the intermittent TDC architecture gathers high-speed readout and low power consumption for pixel data transfer. Design techniques of TCI coils and timing controls of data transfer have possibilities for reducing even the on-stack noise, so we are developing them and they are underway.

Acknowledgment

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Tadahiro Kuroda received the Ph.D. degree in electrical engineering from the University of Tokyo, Tokyo, Japan, in 1999. In 1982, he joined Toshiba Corporation, where he designed CMOS SRAMs, gate arrays and standard cells. From 1988 to 1990, he was a Visiting Scholar with the University of California, Berkeley, where he conducted research in the field of VLSI CAD. In 1990, he was back to Toshiba, and engaged in the research and development of BiCMOS ASICs, ECL gate arrays, high-speed CMOS LSIs for telecommunications, and low-power CMOS LSIs for multimedia and mobile applications. In 2000, he moved to Keio University, Yokohama, Japan, where he has been a Professor since 2002. He has been a Visiting Professor at Hiroshima University, Japan, and the University of California, Berkeley. His research interests include low-power, high-speed CMOS design for wireless and wireline communications, human-computer interactions, and ubiquitous electronics. He has published more than 200 technical publications, including 50 invited papers, and 18 books/chapters, and has filed more than 100 patents. Dr. Kuroda has served as the General Chairman for the Symposium on VLSI Circuits, the Vice Chairman for ASP-DAC, sub-committee chairs for ICCAD, A-SSCC, and SSDM, and program committee member for the Symposium on VLSI Circuits, CICC, DAC, ASP-DAC, ISLPED, SSDM, ISQED, and other international conferences. He is a recipient of the 2005 IEEE System LSI Award, the 2005 P&I Patent of the Year Award, and the 2006 LSI IP Design Award. He is an IEEE Fellow.

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