Paper:

Basic Circuit Design of a Neural Processor: Analog CMOS Implementation of Spiking Neurons and Dynamic Synapses

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We discuss the integration architecture of spiking neurons, predicted to be next-generation basic circuits of neural processor and dynamic synapse circuits. A key to development of a brain-like processor is to learn from the brain. Learning from the brain, we try to develop circuits implementing neuron and synapse functions while enabling large-scale integration, so large-scale integrated circuits (LSIs) realize functional behavior of neural networks. With such VLSI, we try to construct a large-scale neural network on a single semiconductor chip. With circuit integration now reaching micron levels, however, problems have arisen in dispersion of device performance in analog IC and in the influence of electromagnetic noise. A genuine brain computer should solve such problems on the network level rather than the element level. To achieve such a target, we must develop an architecture that learns brain functions sufficiently and works correctly even in a noisy environment. As the first step, we propose an analog circuit architecture of spiking neurons and dynamic synapses representing the model of artificial neurons and synapses in a form closer to that of the brain. With the proposed circuit, the model of neurons and synapses can be integrated on a silicon chip with metal-oxide-semiconductor (MOS) devices. In the sections that follow, we discuss the dynamic performance of the proposed circuit by using a circuit simulator, HSPICE. As examples of networks using these circuits, we introduce a competitive neural network and an active pattern recognition network by extracting firing frequency information from input information. We also show simulation results of the operation of networks constructed with the proposed circuits.

Keywords: dynamic synapse, depressing synapse, analog VLSI

1. Introduction

Phase I of R&D on neural network hardware successfully ended around 1990 with the fabrication of analog/digital circuits that emulate conventional neural networks. R&D has since focused on the development of applications and industrialization of the neural networks based on achievement of Phase I, such as improvement of classical implementation of neuron on silicon chips [1-3] and development of vision sensor chips.

Hardware developers currently tend to apply a constructive method for designing neural circuits. Neuromophic analog LSIs are constructed by a method based on the latest achievements in physiological studies. To realize advanced brain functions in neural processors applying the constructive method, we must study modern neural networks that employ dynamic characteristics of actual neurons, i.e., spiking neuron and dynamic synapses.

Studies on neural hardware focusing on spiking properties of neurons fall into two groups: those aiming at reproduction of spiking characteristics and those emphasizing network construction using the spiking neuron [4]. We have focused on neural hardware mimicking spiking characteristics of neurons and also functional properties possible to be produced with networks using the spiking neuron circuit we developed [5]. Since most of hardware developers are not familiar with mathematical models or physiological experiments, we require cooperative R&D with specialists in these fields. We often hear in recent cooperative study that there is a need to develop large-scale neural networks using analog neuron (closer to the Hodgkin-Huxley model) which is far from the simple spiking neuron models, and thereby produced problems in computer load (simulation time). This factor hinders us from understanding the neural system. Our target here is to develop an analog VLSI that integrates large-scale analog neural circuits. The VLSI is expected to operate in parallel real time, that is, to develop neural chips holding many analog neuron models, to solve the load problem. Developed chips are provided as IP (Intellectual Property: in the VLSI field, this term indicates application specific circuits blocks capable of being reused in other devices), so it will become possible to construct a platform that enables electronics engineers and researchers in other field to design their original neural

hardware. Employment of analog parallel architecture for neural circuit permits real time emulation of large scale network (not-simulation) which employs cell models that exhibit stiff responses, for which digital processors are poor to simulate. On the other hand, a neural circuit fabricated with semiconductor device (silicon neuron) is robust physically and electrically as compared with actual neurons, namely, precision and reproductivity of circuit's response are better than that of actual neuron's response. Thanks to such properties of analog neural circuits, a researcher is able to construct a real time neural network regardless its size of network. Such a network is easy to handle electrically and physically, when compared with an actual neuron network. Such neural network permits to construct "new environment for experiment of neural network" more realistic when compared with virtual model constructed on digital computer. Against such advantage, the analog implementation of neural circuits includes the following disadvantage. It is inferior in (1) adjustments of impedances similar to physiological experiments, (2) real-time multichannel measurements, (3) construction of three-dimensional neural structures, such as axons and dendrites in actual biotissues. Due to restrictions of LSI manufacturing, researchers have decided architectures of neural processors taking such trade-offs into consideration.

The ideal neural net for analog implementation has the following characteristics: 1) the neuron expresses the information processing result by equilibrium potential or spiking row; 2) the input is given by the spiking row or the initial value of dynamics of the spiking row or neurons; 3) a neuron is connected to its neighboring neurons (or connected to all of neurons whose synaptic weights are uniform); 4) redundancy is generated on the network level, not the element (neuron) level. Due to 1), multipoint measurement is possible. Due to 2), input can be given to all neurons with smaller numbers of input pins. 3) is difficult, but data transfer with address-event representation [6] (firing information represents the position of the neuron circuit) has solved the problem. However, this system differs considerably from the constructural design concept. The characteristics of 4) are technologically very important, and by successful adoption of the properties, we have attempted to develop analog LSIs that overcome problems of low tolerance for noise and mismatches in analog devices. The dispersion of physical parameters of semiconductor devices is extremely low compared to that of the actual neuron. To emulate vague devices such as neurons, dispersion of the semiconductor device is not a problem; otherwise, the design concept of the chip is wrong.

In developing such analog ICs, we studied functional properties of a "network" of neurons, rather than the properties of a "neuron". We do not create devices that faithfully regenerate the dynamics of neurons and synapses, but construct networks by analog circuits of simplified spiking neurons and synapses having properties

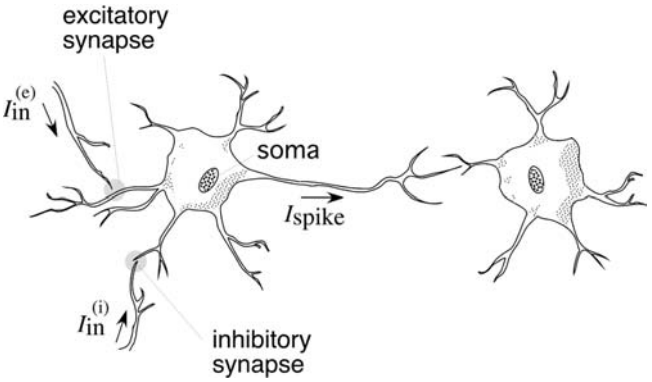

Fig. 1. Schematic image of a neuron model.

considered necessary at the lowest level. We propose LSI architecture of spiking neuron circuit and dynamic synapse circuit capable of large-scale integrationas a basic circuit. We designed the neuron and synapse circuit compactly, aiming at large-scale integration of neural networks on VLSIs. We show an example of construction of neural hardware (network) using them.

2. Model of Spiking Neuron and Its Analog CMOS Circuit

A schematic image of a neuron model is shown in **Fig. 1**. The difference from the conventional McCulloch-Pitts neuron model is that the internal state of single neurons sequentially changes based on the following dynamics:

$$\tau_{\text{e}} \frac{dE}{dt} = -E + I_{\text{in}}^{(\text{e})}, \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (1)$$

$$\tau_{\text{i}} \frac{dI}{dt} = -I + I_{\text{in}}^{(\text{i})}, \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (2)$$

$$\tau_{\text{m}} \frac{dU}{dt} = -(U - V_{\text{rest}}) + E - I, \quad \ldots\ldots\ldots\ldots \quad (3)$$

where

U: membrane potential of soma,
E: excitatory postsynaptic potential (EPSP),
I : inhibitory postsynaptic potential (IPSP),
V_{rest}: resting potential and t: time.
$\tau_{e,\, i,\, m}$: time constants

The neuron receives inputs $I_{in}^{(e)}$ and $I_{in}^{(i)}$ through excitatory and inhibitory synapses. The soma charges and discharges its own membrane capacitance through synapses. When excitatory input increases, membrane potential rises, and when inhibitory input increases, membrane potential falls. The neuron outputs an impulse (spike) when the membrane potential exceeds a preset threshold. The most important point of this model, not shown in the

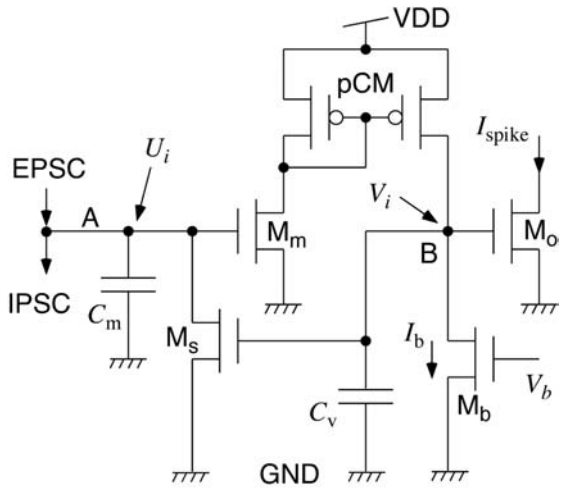

Fig. 2. Electrical neuron circuits.

dynamics above, is to reset the membrane potential to below resting potential after the generation of the spike. During a certain period after the generation, which we call a refractory period, a neuron cannot generate additional spikes even when an excitatory input is given. This neuron is called an integrate-and-fire neuron (IFN) [7].

We propose an analog CMOS circuit that qualitatively exhibits the same behavior as the IFN model of (1)-(3). The circuit was designed based on the current-mode input-output architecture. Because current is summed simply by connecting output, the current-mode neuron circuit is optimum for large-scale network integration in which the sum of output of many neurons is easily calculated. Large- scale integration of neurons is also difficult if the power consumption of each neuron circuit is high. We therefore designed a neuron circuit where MOS transistors operate in their subthreshold region [8].

Figure 2 shows the current mode neuron circuit. When the MOS transistor operates in the subthreshold region, drain-source current is expressed by:

$$I_{ds} = I_0 e^{\kappa V_{gs}/V_T}(1 - e^{-V_{ds}/V_T} + V_{ds}/V_0) \quad \ldots\ldots\ldots (4)$$

Here, potentials of the transistor source and substrate are assumed to be the same. I_{ds} expresses drain-source current, V_{gs} gate-source voltage, V_{ds} drain-source voltage, V_0 early potential, I_0 and κ are process-dependent parameters, and $V_T=kT/q$ (k is Boltzmann's constant, T absolute temperature, q charge of electron; at room temperature V_T is about 26 mV). Typical values of the standard 1.5-μm n-well analog CMOS process are I_0=0.5 $\times 10^{-15}$ A, V_0 = 15 V and κ = 0.6. We define the value of I_{ds} become independent of the magnitude of V_{ds} when V_{ds} exceeds 4 V_T, which we call the saturation region of operation. In this case, (4) is simplified as

$$I_{ds} = I_0 \exp(\kappa V_{gs}/V_T) \ldots\ldots\ldots\ldots\ldots\ldots (5)$$

We call this equation saturation current equation of MOS transistor at the subthreshold region.

When the input current through excitatory and inhibitory synapses is expressed by EPSC (excitatory postsynaptic current) and IPSC (inhibitory postsynaptic current), dynamics at junction A in **Fig. 2** are given by

$$C_m \frac{dU_i}{dt} = -g\,U_i + (\mathrm{EPSC} - \mathrm{IPSC}) - I_0 \exp(\kappa V_i/V_T)$$
$$\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (6)$$

where

C_m : membrane capacitance and
g : leakage conductance between junction A and ground.

Equation (6) is equivalent to (3) with V_{rest} =0 when the last term of the right member is excluded. This term expresses the current of transistor M_s and this transistor shunts junction A to ground. The level of shunting is decided by the magnitude of gate voltage V_i of transistor M_s. Dynamics of V_i at junction B are obtained from (5) as:

$$C_v \frac{dV_i}{dt} = I_0 \exp(\kappa U_i/V_T) - I_b \,,\ldots\ldots\ldots\ldots (7)$$

where

C_v: capacitance and;
I_b : current of transistor M_b

When U_i rises by the increase in excitatory input EPSC, the current of transistor M_m increases. The current charges C_v through a pMOS current mirror (pCM), and V_i also rises. By this increase in V_i, currents of transistors M_s and M_0 increase exponentially as (5). Junction A is thus shunted to ground immediately after the increase. This momentary increase and decrease of U_i represents generation of spikes. Spiking output is taken from transistor M_s. Because transistor M_b discharges the electric charge of C_v, V_i falls below the threshold of transistor M_s after a certain refractory period. During the period, the neuron can not output spikes even when ESPC increases.

3. CMOS Implementation of Dynamic Synapses

A synapse, whose conductivity (weight) changes based on the firing rate or spike timing of presynaptic neurons, is called a dynamic synapse [9,10]. The change of synapse weight in dynamic synapses is caused by short-term changes in the transmitter discharge and regeneration cycle at the terminal of presynapses rather than by learning on a network level.

The simplest operation of the dynamic synapse was described in (1) and (2) in the preceding section. These synapses produce EPSP and IPSP by integrating output ($I_{in}^{(e,\,i)}$) of the presynaptic neuron. A signal is conducted to a postsynaptic neuron through EPSP and IPSP. When

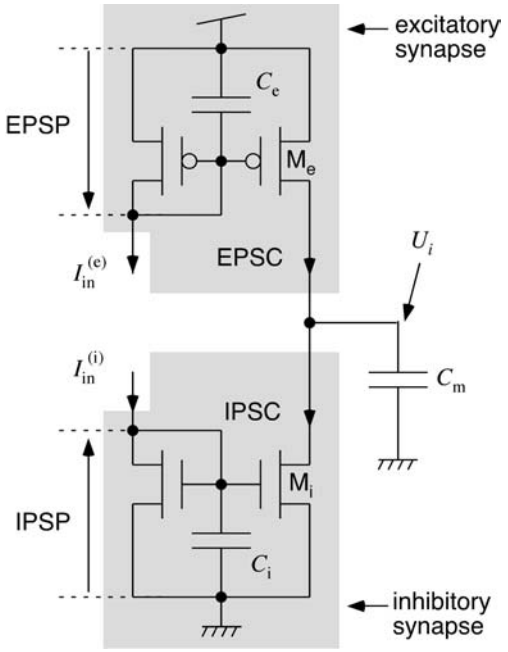

Fig. 3. Excitatory/inhibitorydepressing synapse circuits.

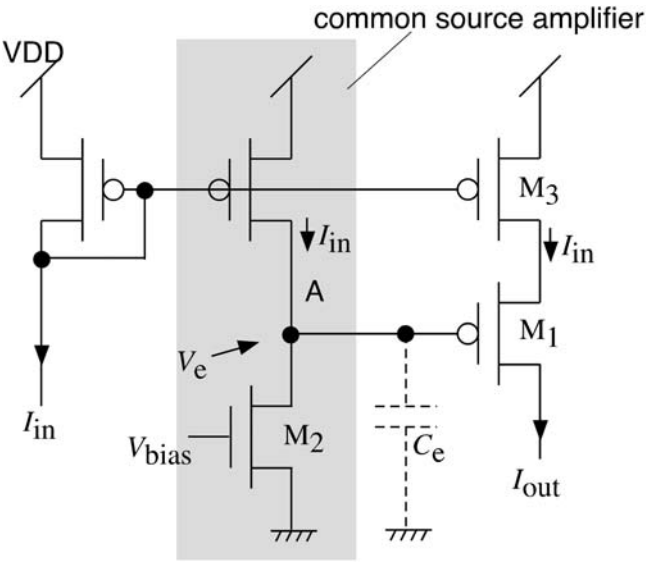

Fig. 4. Depressing synapse circuits corresponding to impulse input.

the firing frequency of the presynaptic neuron increases and sequential change of EPSP and IPSP comes to be unable to follow input, the signal conduction efficiency to postsynaptic neuron drops. Thus, this synapse behaves as a lowpass filter. Because presynaptic neuron output is depressed and conducted to the postsynaptic neuron, such synapse is called depressing synapse and a synapse acting inversely is called facilitating synapse.

Figure 3 shows the depressing synapse circuit. Depending on the connection type with postsynaptic neurons, depressing synapses are classified as excitatory or inhibitory. The excitatory (inhibitory) synapse circuit charges (discharges) the membrane (C_m) of the postsynaptic neuron and the membrane potential rises (falls). Each synapse circuit receives input current $I_{in}^{(e,\,i)}$ and generates EPSP and IPSP. EPSP and IPSP are converted to electric current by MOS transistors M_e and M_i, and charges and discharges the membrane (C_m) of the postsynaptic neuron. EPSC (current of M_e) and IPSC (current of M_i) are obtained from (5) as:

$$\mathrm{EPSC} = I_0 \exp(\kappa \mathrm{EPSP} / V_\mathrm{T}) , \quad \ldots\ldots\ldots\ldots \quad (8)$$

$$\mathrm{IPSC} = I_0 \exp(\kappa \mathrm{IPSP} / V_\mathrm{T}) , \ldots\ldots\ldots\ldots\ldots\ldots \quad (9)$$

The dynamics of the excitatory and inhibitory synapses are

$$C_\mathrm{e} \frac{d\mathrm{EPSP}}{dt} = -I_0 \exp(\kappa \mathrm{EPSP} / V_\mathrm{T}) + I_\mathrm{in}^{(\mathrm{e})} , \ldots . \quad (10)$$

$$C_\mathrm{i} \frac{d\mathrm{IPSP}}{dt} = -I_0 \exp(\kappa \mathrm{IPSP} / V_\mathrm{T}) + I_\mathrm{in}^{(\mathrm{i})} , \ldots . \quad (11)$$

$C_e(C_i)$ expresses the capacitance between the excitatory (inhibitory) synapse and soma. Equations (10) and (11) are qualitatively equivalent to (1) and (2).

The depressing synapse circuit (**Fig.3**) is constructed with a simple circuit, but it is problematic in handling impulse input (pulse width of spiking does not depend on firing frequency). This synapse circuit integrates input pulses by charging and discharging capacitances (C_e and C_i). When the values of capacitances are large (integration for a long period), the maximum amplitude of output pulse becomes low and the pulse width becomes wide. Therefore, the maximum amplitude of output pulse is depressed but the efficiency per spike (here, the quantity of electric charge which one spike has) does not change between presynapse and postsynapse, so we propose a depressing synapse circuit in which the efficiency per synapse is depressed based on increase of firing rate even to the input of constant pulse width and whose construction is easy. **Fig.4** shows a depressing synapse constructed by combining a current mirror and common-source amplifier. When there is no input (I_{in} = 0), voltage V_e of junction A is zero. Therefore, transistor M_1 is in an on state. When input current is given (I_in>0), V_e increases and M_1 becomes off. Therefore, the current mirrored to output I_{out} through transistor M1 and M3 is zero. Because there is parasitic capacitance C_e at junction A, the increase of V_e accompanies a short-time delay. Therefore, transistor M_1 becomes on state for a short time, and the circuit outputs pulsive current. When the input current becomes zero again, transistor M_2 discharges the parasitic capacitance C_e and V_e returns to

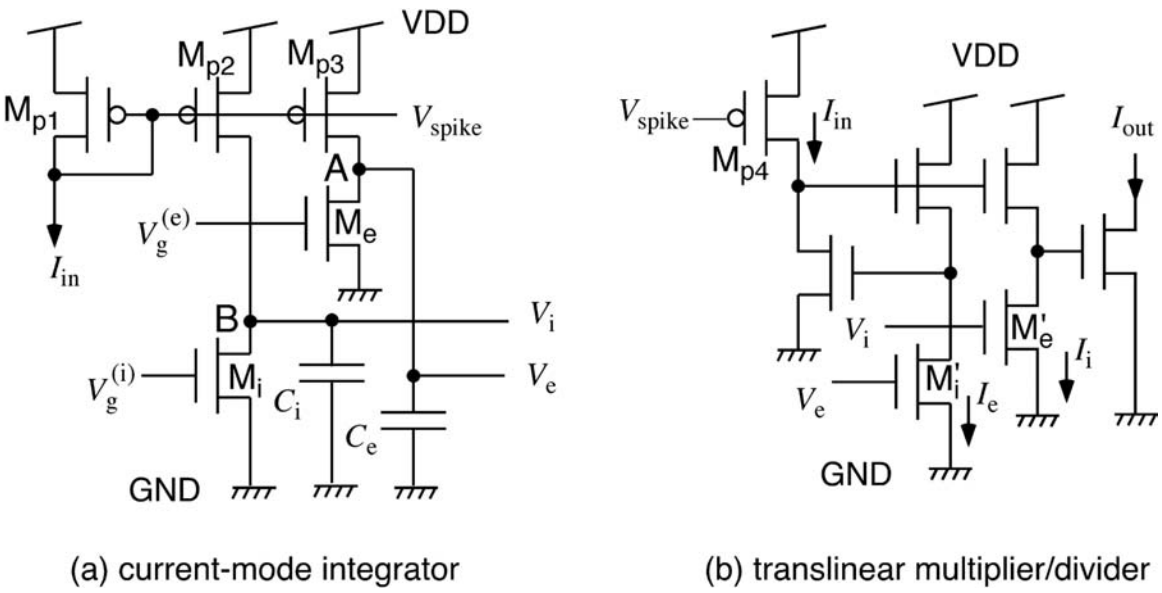

Fig. 5. Dynamic synapse circuits with depressing and facilitating properties.

zero. If the pulsive current (spike) is given at a short interval, subsequent spikes enter before V_e returns to zero. Because M_1 is not perfectly on, the amplitude of output spike becomes small based on the magnitude of V_e (when V_e increases, the amplitude of output spike decreases). Therefore, the efficiency per spike (here, quantity of electrical charge which one spike has) decreases. Because current of transistor M_2 monotonically increases based on increase of gate voltage V_{bias}, when V_{bias} increases, the time until V_e returns to zero decreases. By adjusting voltage V_{bias}, it is therefore possible to change the time constant of depressing.

Here, we propose yet-another dynamic synapse circuit that exhibits both depressing and facilitating properties. First, a current integrator as shown in **Fig.5 (a)** is constructed. Input I_{in} from the presynaptic neuron is transferred to junctions A and B by the current mirror (M_{p1} to M_{p3}) and capacitors C_e and C_i are charged, and transistors M_e and M_i discharge the capacitors C_e and C_i. When the firing cycle of the presynaptic neuron becomes shorter than the charging and discharging time constant of current integrators, the mean values of V_e (or V_i) in time increases.

In this circuit construction, drain voltage V_e and V_i of transistors M_e and M_i take value below 4 V_T (MOS transistor does not operate in saturation). Therefore when current of transistors M_e and M_i is expressed using (4), the dynamics at junctions A and B in **Fig.5(a)** are as follows:

$$C_i \dot{V}_i = I_{in} - I_0 e^{\kappa V_g^{(i)}/V_T}(1 - e^{-V_i/V_T} + V_i/V_0)$$

$$C_e \dot{V}_e = I_{in} - I_0 e^{\kappa V_g^{(e)}/V_T}(1 - e^{-V_e/V_T} + V_e/V_0)$$

Output (V_e, V_i, V_{spike}) of **Fig.5(a)** is given to translinear multiplier-divider [11]. The input-output characteristic of the translinear multiplier-divider, shown in **Fig.5(b)**, is

$$I_{out} = \frac{I_e}{I_i} I_{in}$$

and if transistors M'_e and M'_i operate in saturation, the output current of the circuit is obtained from (5) as:

$$I_{out} = \frac{e^{\kappa V_e/V_T}}{e^{\kappa V_i/V_T}} I_{in}$$

Input current I_{in} from the presynaptic neuron is given to the translinear multiplier-divider through the current mirror (M_{p1} and M_{p4}) where V_{spike}, and V_e and V_i of **Fig.5(a)** are given to gates of transistors M'_e and M'_i in **Fig.5(b)**. When $V_e > V_i$, the translinear multiplier-divider amplifies input from the presynaptic neuron, and when $V_e < V_i$, output is restricted. If the amplitude of input spiking current from the presynaptic neuron is constant and $C_i = C_e$, the relative magnitude of voltages at junctions A and B is decided only by the current of transistors M_e and M_i. The current of these transistors increase monotonically based on the increase of gate voltage $V_g^{(e)}$ and $V_g^{(i)}$ of M_e and M_i, so when gate voltage increases, the time constant of the integration circuit decreases. Therefore, if $V_g^{(e)} > V_g^{(i)}$, the time average of V_i becomes larger than that of V_e. Consequently, the gain of the translinear multiplier-divider decreases. Supposing I_{in} and I_{out} are output of the presynaptic neuron and input of the postsynaptic neuron, this circuit functions as a depressing synapse. If $V_g^{(e)} < V_g^{(i)}$, the mean value of V_e in time becomes larger than that of V_i, the gain of the translinear multiplier-divider increases. This circuit functions as a facilitating synapse.

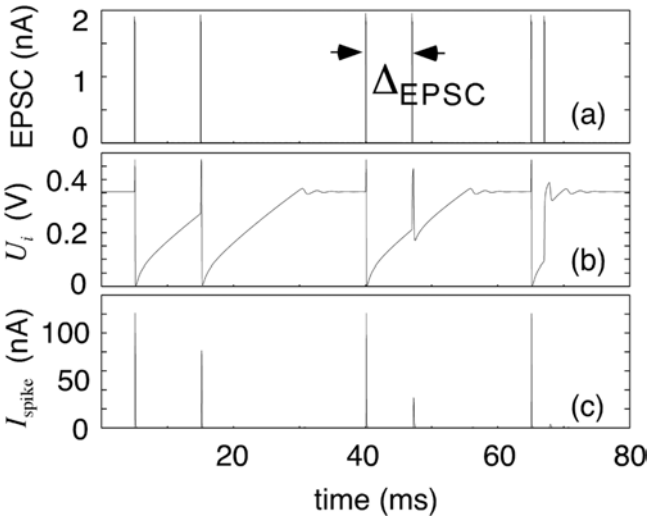

Fig. 6. Results of simulation of spiking neuron circuits.

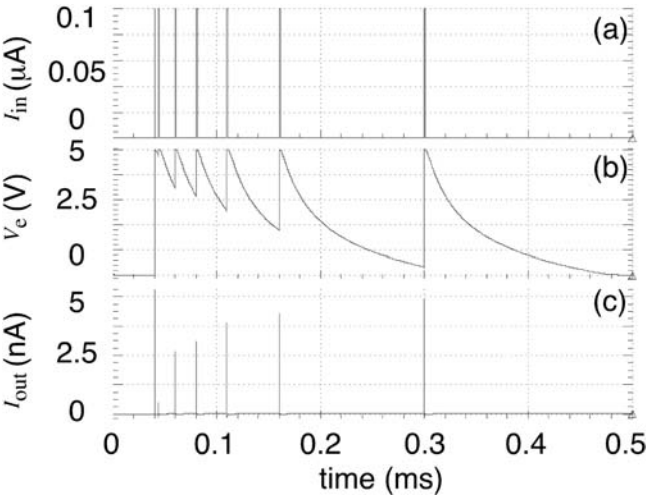

Fig. 7. Results of simulation of depressing synapse circuits**.**

With the proposed circuit, the functions of depression and facilitation are switched by the balance of the magnitudes of $V_g^{(e)}$ and $V_g^{(i)}$.

4. Result of Simulation

We examined operation of the spiking neuron and dynamic synapse circuits by simulation. The following simulation result was obtained by circuit simulator HSPICE with the parameters of AMIS 1.5-μm CMOS transistors of MOSIS. The minimum size transistors (channel width and length are 2.3 μm and 1.5 μm) were used.

Figure 6 shows the simulation result of the spiking neuron circuit (C_m = 300 fF, C_v = 1 pF, I_b = 1 nA). When EPSC is given at the timing in **Fig.6(a)**, the peak of membrane potential U_i (**Fig. 6(b)**) decreases based on the decrease of time interval of EPSC (Δ_{EPSC}) and decrease of spiking output was confirmed (**Fig.6(c)**). Namely, the amplitude of output spikes decreased as Δ_{EPSC} decreased. In this simulation, to make the time constant of the circuit the same level as the actual neuron ($O(10^{-3})$ seconds), capacitances (C_m and C_v) were set at relatively large values. If it is desirable to operate this circuit faster than the actual neuron, small capacitances can be chosen (compact circuits can thus be implemented on a chip). This circuit correctly operated on the order of transistor gate capacitance (10 fF in this process; the time constant under the same bias condition is $O(10^{-6})$ seconds). Even when using a relatively redundant 1.5-μm CMOS process, the size of the neuron circuit on the chip becomes below 10 μm^2. If the input and output of this circuit are assumed to be output of presynaptic neuron and input of the postsynaptic neuron, it operates in the same way as the depressing synapse in which postsynaptic neuron input decreases based on the spiking interval decrease of the presynaptic neuron. This means the depressing circuit can be constructed without modification of the circuit.

Figure 7 shows an example of operation of the depressing synapse circuit (V_{bias} = 0.3 V, input pulse width: 10 μs, pulse amplitude: 0.1 μA). The input current I_{in} was given to the circuit as spikes by changing the spike interval (**Fig.7(a)**). The first spike was given at t = 40 μs. Subsequent spikes were given at t = 44 μs, 60 μs, 80 μs, 110 μs, 160 μs and 300 μs. When inputs are given successively in a short time (around 4 μs to 50 μs in (**Fig.7(a)**), the amplitude of the output pulse is depressed (**Fig.7(c)**). As the interval is widened, V_e approaches zero (**Fig.7(b)**) and it was confirmed that the amplitude of the output pulse returns to the initial value. **Fig.8** shows the change of amplitude of output pulse to the interval of input spikes. The abscissa shows the interval and the ordinate the amplitude of output pulse. Simulation result and its approximate curve are shown. We confirmed that as the spiking interval becomes short, the amplitude of the output pulse is depressed.

Figure 9 shows an example of operation of depressing and facilitating synapse circuits. (C_e =C_i =10 pF), input pulse cycle: 1 ms, pulse width: 10 μs, pulse amplitude: 1 nA). As designed, when $V_g^{(e)} > V_g^{(i)}$ and spiking input I_{in} (**Fig.9(a)**) was given, the difference between V_e and V_i became big based on increase of number of spiking (V_i<V_e), and I_{out} was depressed based on input of the spiking row (**Fig.9(b)**; set as $V_g^{(e)}$=0.3 V, $V_g^{(i)}$=0.2 V). On the contrary, for $V_g^{(e)} < V_g^{(i)}$, I_{in} increased based on the input of spiking row (**Fig.9(c)**, set as $V_g^{(e)}$ = 0.1 V, $V_g^{(i)}$=0.3 V). We confirmed that when input is cut off, current gain gradually returns to the initial value.

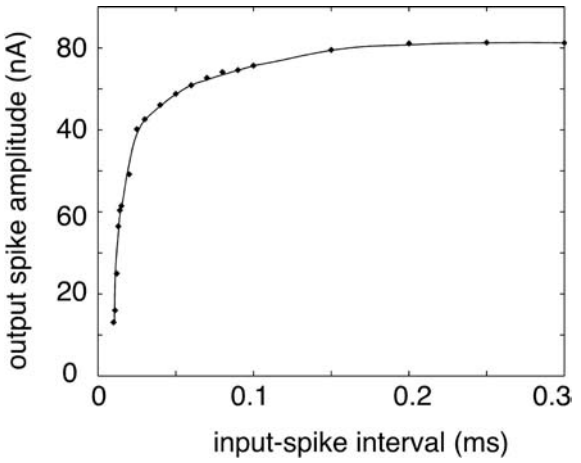

Fig. 8. Attenuation in output spike amplitude against input spike interval.

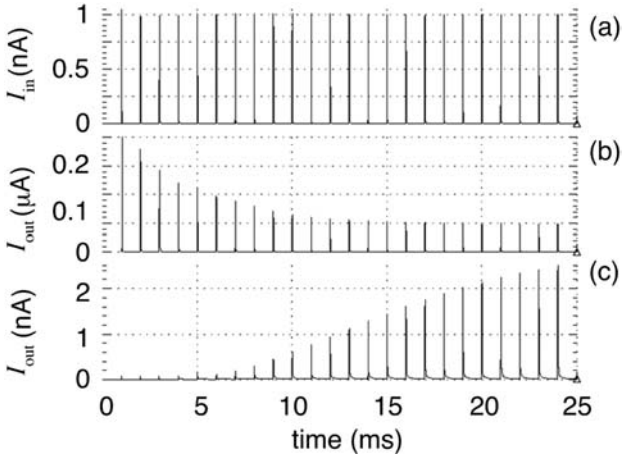

Fig. 9. Operations of depressing and facilitating synapse circuits.

5. Example of Network Construction

We constructed a network using the spiking neuron circuit and the dynamic synapse circuit we propose. We introduce examples of a network construction to make neural competition in a noisy environment and a network to achieve pattern recognition by extracting information on firing frequency from the input information. We clarify the functional properties generated when network is constructed using spiking neuron circuit by simulation.

5.1. Competitive Neural Network

The competitive neural network, which is easily seen in various nervous systems, exhibits selective activation and inactivation among neurons in the network. Each neuron receives external stimuli. A neuron receiving the largest external input is activated, while other neurons are inactivated after neural competition. When the network activates both single and multiple neurons based on the magnitude of the neuron's input, redundancy is produced at the network-level [12]. When the concept of firing time (spike timing), not of firing rate, is introduced in the information code of the neural network, selection efficiency of neurons can be greatly improved [13]. Aiming at a brain type processor to efficiently achieve competition under noise environment, we implemented the analog electronic circuit of the spike-timing-based competitive neural network.

Figure 10 shows the construction of a competitive neural network where the neural information is encoded in terms of spike timing. Plural IFNs excite one global inhibitory neuron (GI) and conversely the GI inhibits all IFNs. The black circle in the figure represents inhibitory synapses, and the white excitatory synapses. Periodic spike inputs were given to these IFNs from outside. The magnitude of input information is expressed by the timing of generation of spikes (not conventional "number of spikes per time"). A neuron that receives an input spike

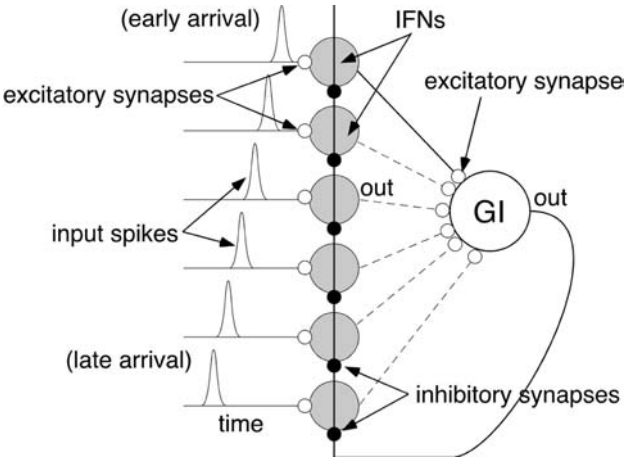

Fig. 10. Construction of competitive neural network with IFNs.

early is assumed to have a large input, while a neuron receives a late spike is assumed to have a small input. IFN at which input spike arrives early (IFN receiving large input) generates output spikes. This is because GI is excited by generation of output spikes and by that, the IFN which has not received input spikes yet (IFN with small input) is inhibited. We call the network, in which neuron receiving large input among the plural inputs is left, the competitive neural network.

The competitive network consists of synapses of neurons having the dynamics shown in (1)-(3)[13], so the network is constructed using the synapse circuit having the performance of (1) and (2) (**Fig.3**) and the neuron circuit having the dynamics of (3) (**Fig.2**). We call the circuit in **Fig.2** an IFN circuit and the circuit in **Fig.3** a synapse circuit.

Figure 11 shows the internal structure of the competitive neural processor. IFN circuit generates spiking current ($I_{in}^{(e)}$) when it accepts input current (I_{spike}). I_{spike} generated by each IFN is added by connection and given to GI (current mirror circuit). The output of GI (the sum total of I_{spike}) is connected to inhibitory input terminal

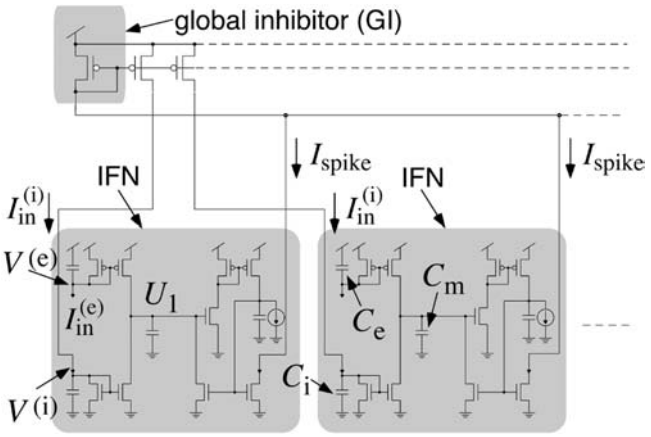

Fig. 11. CMOS cuicuits of competitive neural network.

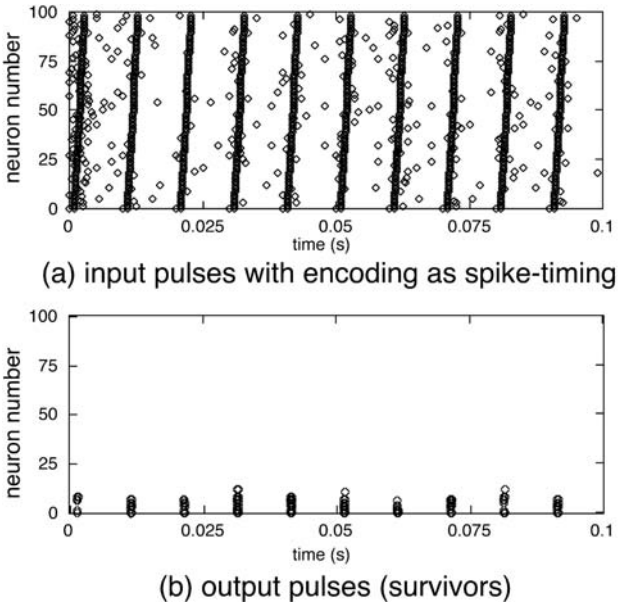

Fig. 12. Simulation results of competitive network using IFNs (number of neurons=100).

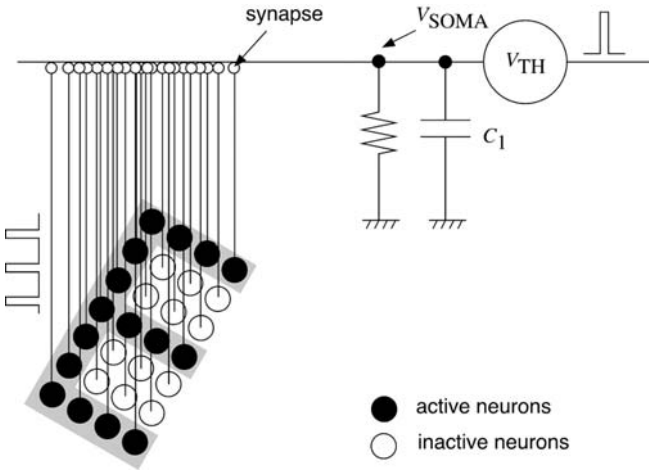

Fig. 13. Active pattern discrimination circuits using depression synapses and spike neurons.

$I_{in}^{(i)}$ of all IFNs and a closed network is constructed. When current is given to the inhibitory input terminal, the membrane potential (U_i) falls, so the IFN circuit does not generate spiking current. Therefore, IFN at which input spikes arrive early excites GI and the excitation lowers the membrane potential at which input spike has not arrived yet. With this construction, IFN at which input spike arrives early (receiving large input) generates output spikes.

We simulated the operation of a network with combination of 100 units of IFN circuits. Each IFN receives input-spike currents. The period and amplitude of input spikes were uniform among all neurons. An index (0 to 99) was given to each neuron. A neuron with a small index number accepts early spikes, while a neuron with a large index number accepts late spikes. Random train of spikes (amplitude of 10% of periodic input spike) is mixed (**Fig.12(a)**). We confirmed that overwhelmingly small number of IFNs generated erronous spikes to the input (compared to frequency of generation of irregular input spikes) and several IFNs with smaller numbers generated correct spikes (**Fig.12(b)**).

5.2. Pattern Recognition Neural Network

We assume a simple network as **Fig.13**. Many spiking neurons are connected to a postsynaptic neuron. Active neuron outputs spikes at a constant period and inactive neuron outputs nothing. The postsynaptic neuron outputs a spike for $V_{SOMA} > V_{TH}$, and resets V_{SOMA} after the firing. V_{SOMA} increases in proportion to the number of presynaptic active neurons. Therefore, this network can discriminate the number of presynaptic active neurons by setting threshold V_{TH} corresponding to the number of active neurons. V_{SOMA} increases in proportion to firing frequency of spiking neurons, too. For example, we assume that the pulse amplitude and pulse width of input spikes, and leak from V_{SOMA} are constant independent of the firing frequency of input spikes. The value of V_{SOMA} produced by 50 active neurons with a firing frequency of 20 Hz is the same as the value of the potential produced by 10 active neurons with that of 100 Hz. Therefore, the performance of the network to discriminate the number of presynaptic active neurons shown in **Fig.13** largely deteriorates due to the change of the firing frequency. It is shown that the discrimination performance become independent of firing frequency (discrimination performance is improved) by using the depressing synapse [14]. If input spikes are given to the depressing synapse successively in a short period, (the case of high firing frequency of each neuron), the efficiency per spikes (here, the quantity of electrical charge that flows into C_i of **Fig.13**) drops. Even if the number of input spikes increases with the increase in firing frequency, the value of V_{SOMA} does not change greatly because the efficiency per spike is low-

Table 1. Difference in performances of discrimination circuits for use/nonuse of depressing synapse.

	E	E	E	L	L	L	-	-	-
conventional synapses	+	+	-	+	+	-	+	-	-
	fail			fail			fail		
depressing synapses	+	+	+	-	-	-	-	-	-
	success			success			success		

+ : $V_{SOMA} > V_{TH}$
- : $V_{SOMA} < V_{TH}$

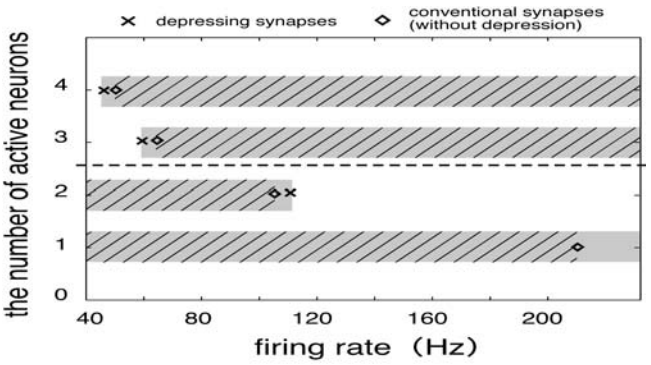

Fig. 14. Measurement results of networks that discriminate between numbers of active neurons (number of synapse=4).

ered. The discrimination performance of the network becomes independent of firing frequency. It is expected that the discrimination result will differ as shown in **Table 1** between using the depressing synapse and not using it. Here, presynaptic neurons are located in two dimensions as **Fig.13**. The active neuron forms patterns such as "E", "L" and "-". The number of neurons is the largest for "E" and the smallest for "-". We assume that threshold is set to the middle between "E" and "L". Firing frequency is expressed by grayscale letters in the table. Closer to black, the firing frequency is high, and closer to white, the firing frequency is low. In the network not using depressing synapse, even in "E" which intrinsically does not fall below threshold, V_{SOMA} does not exceed a threshold at low firing frequency. In "L", and "-" which intrinsically does not exceed threshold, V_{SOMA} is expected to exceed the threshold at high firing frequency. In the network using depressing synapses, because the depressing synapse lowers the efficiency per spike at high firing frequency of input, increase of V_{SOMA} becomes independent of the firing frequency. The network is thus expected to discriminate the number of active neurons independent of firing frequency. We implement this network electronically using the dynamic synapse circuit we designed, and we show that performance approaches the ideal case (**Table 1**).

The basic elements of the network in **Fig.13** are the spiking neuron to output impulse and depressing synapses. Because it is necessary to handle impulse information, the network requires either the depressing synapse circuit in **Fig.4** or the dynamic synapse circuit combining depressing and facilitating performances in **Fig.5**. Because this network does not have facilitating synapses, we adopted the depressing synapse with simple structure in **Fig.4**. We constructed a network in which four synapses are connected to the neurons on a breadboard using *n*-MOS (NEC 2SK1398) and *p*-MOS (NEC 2SJ184). As input, a pulse with pulse amplitude of about 80 μA and pulse width of 0.5 ms was given. Bias voltage V_{bias} was 1 V. Time constant of postsynaptic neuron was 0.1 s. Measurement was done for each case using depressing synapse and the case not using. A threshold was set to the middle of V_{SOMA} for two active neurons and V_{SOMA} for three active neurons at firing frequency of 80 Hz (V_{TH} is 0.24 V when using depressing synapse and 1.99 V when not using). The measurement result of the network is shown in **Fig.14**. The firing frequencies when V_{SOMA} exceeded the threshold to the active neuron for the first time were plotted. The range to be correctly discriminated is shown too. The range shown in gray represents the range where the network using the depressing synapse could correctly discriminate and the range shown in oblique lines represents the range where the network not using the depressing synapse could correctly discriminate. For one active neuron, V_{SOMA} did not exceed the threshold even when the firing frequency was raised. This indicates that for one active neuron, the network discriminates completely independent of the firing frequency by the effect of the depressing synapse. From the experiment, we confirmed that discrimination performance of the network can be improved by using depressing synapse.

To confirm improvement of discrimination performance in a large-scale network, HSPICE simulation was conducted for the network having 100 synapses. As the synapse, the depressing synapse in **Fig.4** is used. We assumed that presynaptic active neuron forms the patterns such as "E", "L" or "-", and "E" is with 90 active neurons, "L" with 50, and "-" with 10. As input, pulse with pulse amplitude of 1 nA and pulse width of 10 μs was given. The time constant of postsynaptic neuron was 2 ms. In experiments, we studied the performance of the network with both conventional and depressing synapses. The threshold was set at the value of V_{SOMA} produced by 70 active neurons with a firing frequency of 5 kHz assuming the middle pattern between "E" and "L". The values of threshold V_{TH} were 0.2 V when the depressing synapse was used and 1.97 V when conventional synapse was used. The simulation result is shown in **Fig.15**. The firing frequencies when V_{SOMA} exceeded the threshold to the active neuron for the first time were plotted. The

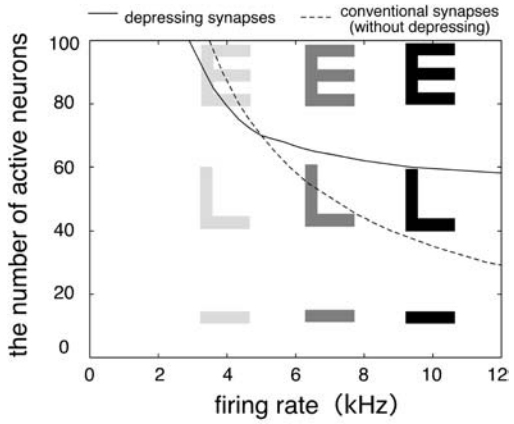

Fig. 15. Simulation results of large-scale active neuron number discrimination network(number of synapses=100).

discrimination result obtained from the simulation was the same as shown in **Table 1** except for the results of the conventional synapse with a small number of active neurons (the letter "-") at the highest frequency. This indicates that the performance of the network with the proposed depressing synapse circuits is the same as the ideal one irrespective of the use of analog CMOS devices. A letter closest to black expresses firing of each active neuron at 10 kHz, a letter closest to white at 4 kHz, and letter of the intermediate color at 7 kHz. When not using depressing synapses, correct discrimination cannot be achieved as for "E" and "L". We confirmed that in using depressing synapse, correct discrimination can be achieved for all patterns. From the simulation result, we confirm that the discrimination performance of the network can be improved by using the depressing synapse.

6. Conclusion

We have proposed a spiking neuron and dynamic synapse circuit as the first step for developing architecture, for learning from the brain, that operates correctly even in a noisy environment. These represent the model of the neuron and synapse in a form closer to the brain. We showed the dynamic performance of the spiking neuron circuit and dynamic synapse circuit by simulation. Using the circuit we propose electronically implemented functional network having synapse and neuron with dynamic properties (network to achieve neural competition under noisy environment and network to achieve active pattern recognition extracting information of firing frequency from input information). We examined the performance of the networks by measurement and electronic circuit simulation. From simulation of the network to achieve neural competition, we confirmed that the network has tolerance for the noise (though not perfect). From the measurement and simulation result of the network to achieve active pattern recognition, we confirmed that the discrimination performance has tolerance for the change in the firing frequency by using a depressing synapse.

In the analog electronic circuit, information is expressed by converting the natural physical quantity into the physical quantity in the electronic circuit (voltage or current), so noise directly influences the information handled, making it very important to take measures against noise in the analog electronic circuit. In a natural environment without noise measures, it is naturally probable that spiking neuron generates erroneous spike. Tolerance for the change of firing frequency means that the network cancels erroneous spiking information. The network to achieve active pattern recognition, such as the competitive neural network, is said to have tolerance for noise. We showed that the network to achieve active pattern recognition and the neural competition network have tolerance for noise although no special noise measures are taken. Although the problem of noise cannot be completely overcame, the result that analog circuits can be made naturally noise-tolerant by assembling network circuit learning from the organism structure is very promising in development as an antinoise measure in analog LSI.

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