PAPER

Neuromorphic MOS Circuits Exhibiting Precisely Timed Synchronization with Silicon Spiking Neurons and Depressing Synapses

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Abstract **A neural network exhibiting precisely timed synchronization in a noisy environment with depressing synapses was proposed by Fukai and Kanemura [1]. Based on this network, we constructed neural network hardware using silicon neurons and depressing synapse circuits and evaluated timing precision among the neurons using a simulation program with integrated circuit emphasis (SPICE). Consequently, timing jitter among the neurons was significantly reduced with depressing synapse circuits compared to nondepressing synapses. Moreover, a novel analog circuit mimicking characteristics of spike-timing dependent plasticity (STDP) was proposed to construct a neural network that exhibits robust synchronization in a noisy environment. We demonstrate the circuit's basic learning characteristics using SPICE.**

Keywords: neuromophic VLSI, depressing synapse, spiking neuron, recurrent neural network, spike-timing dependent plasticity

1. Introduction

Although neurons in the cerebral cortex have firing variations, they often synchronize very precisely [2–4]. The discovery of this synchronous phenomenon was almost concurrent with the appearance of synchronization (clock skew) problems in digital large-scale integrated circuits (LSIs), which are due to the device's parasitic capacitances and resistances. Semiconductor device mismatches have also recently become even more common with the rapid development of sub-micron fabrication processes. Since guaranteeing an appropriate timing margin has so far been difficult, major LSI designers have started using advanced genetic algorithms in post-manufacturing processes to calculate the required margin [5].

Against such a background, reports describing that the population of neurons, each of which has markedly larger variations than present semiconductor devices, exhibits exceptionally accurate synchronization have been extremely inspiring because neurons could provide a possible way to solve the clock skew problem in digital LSIs. A neural network model with depressing synapses that exhibits such precisely timed synchronization even in a noisy environment was recently proposed by Fukai and Kanemura [1]. In this paper we designed analog MOS circuits that 'qualitatively' imitate this network model. The circuit is constructed with silicon neurons and depressing synapse circuits. Using a simulation program with integrated circuit emphasis (SPICE), we demonstrate that depressing synapses facilitate precise synchronization among silicon neurons. Since a higher tolerance to external noises could be achieved by introducing spike-timing dependent plasticity (STDP) learning in the network model [1], we also propose an analog circuit for the STDP learning.

2. Precisely Timed Pulse Synchronization Network

Let us briefly review a neural network model for precisely timed synchronization and its dynamic behavior. Then we will introduce two basic MOS circuits that imitate the integrate-and-fire neurons and depressing synapses used in the neural network model.

2.1 Network model

The dynamics of a neural network model for precisely-timed synchronization [1] are given by

$$\begin{aligned}
\tau_m \frac{dV_i}{dt} &= -(V_i - V_{\rm rest}) - \frac{1}{NR}\sum_{j\neq i} c_{ij} g_{ij}^{\rm ee}(V_i - V_{\rm syn}) \\
&\quad -g^{\rm ei}(V_i - V_{\rm cl}) + E_i \\
\tau_e \frac{dE_i}{dt} &= -E_i + E_0\,\delta(t - t_i^{\rm inp}), \quad (i = 1, \cdots, N) \\
\tau_i \frac{dV}{dt} &= -(V_i - V_{\rm rest}) - g^{\rm ie}(V - V_{\rm syn})
\end{aligned}$$

where V_i and V represent the membrane potentials of the i-th pyramidal (integrate-and-fire) neuron and an interneuron; E_i the postsynaptic potential of the i-th pyramidal neuron; $\tau_{m,e,i}$ the time constants of pyramidal neu-

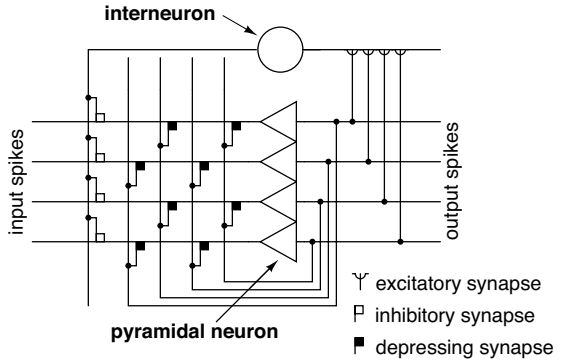

Fig. 1 Neural network model for precisely-timed pulse synchronization

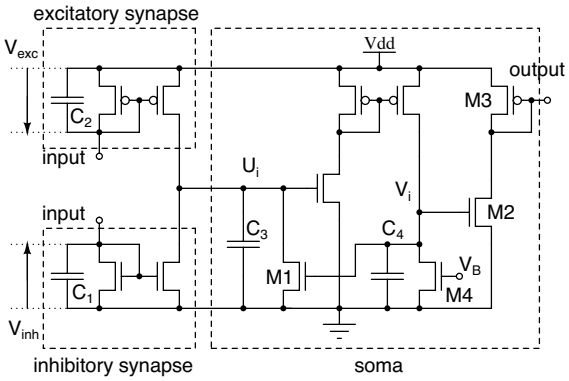

Fig. 2 Silicon neuron with conventional excitatory and inhibitory synapses

rons, excitatory synapses, and interneurons; N the number of pyramidal neurons; R the positive-feedback connectivity between the pyramidal neurons as described below; $V_{\mathrm{rest,syn,cl}}$ the resting potential of pyramidal neurons, depressing synapse, and interneurons; t_i the time at which the i-th input spike is given; c_{ij} the binary representing the existence of feedback connections between the i-th and j-th pyramidal neurons; and $g^{\mathrm{ee,ei,ie}}$ the synaptic conductance between excitatory-to-excitatory, excitatory-to-inhibitory, and inhibitory-to-excitatory neurons.

Figure 1 illustrates the network model. Four pyramidal neurons (triangles) are shown. All of the outputs of the pyramidal neurons are sent to an interneuron (circle in the figure) through excitatory synapses, whereas the interneuron inhibits all of the pyramidal neurons through inhibitory synapses. Outputs of the pyramidal neurons are randomly connected to pyramidal neurons through depressing synapses (R represents the connection ratio). Since these synapses provide positive feedback connections to pyramidal neurons [1], firing one pyramidal neuron induces firing of other pyramidal neurons, which results in synchronous firing of pyramidal neurons. The divergence due to the positive feedback is attenuated by the interneuron that inhibits all of the pyramidal neurons.

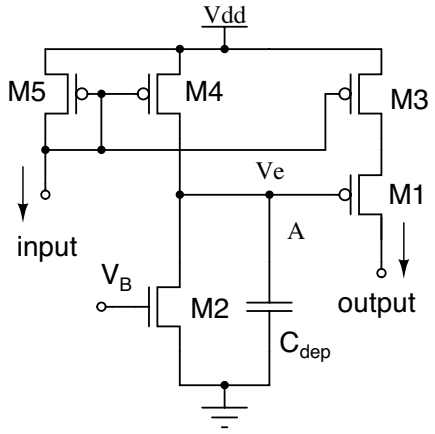

Fig. 3 Depressing synapse circuit

2.2 Silicon neurons and depressing synapse circuits

Asai and Kanazawa *et al.* proposed using silicon neurons and hardware depressing synapses to implement functional spiking neural networks on analog LSIs [6, 7]. We introduce using silicon neurons and depressing synapse circuits to construct the network model described in the preceding subsection and explain the circuit's operational principles.

Figure 2 shows a circuit diagram of a silicon neuron that imitates the basic operations of an integrate-and-fire neuron. Excitatory and inhibitory synapses are constructed by pMOS and nMOS current mirrors that receive input spikes as currents. Delayed synaptic potentials (V_{inh} and V_{exc}) are generated by capacitors C_1 and C_2. The excitatory postsynaptic current generated by V_{exc} charges C_3 and consequently increases the membrane potential U_i, whereas the inhibitory postsynaptic current generated by V_{inh} decreases it. An increase in the membrane potential in the soma circuit induces an increase in potential V_i by charging C_4. Thus, when the membrane potential exceeds a certain threshold, the membrane node (U_i) is suddenly shunted by transistor M1. Although the shunted current increases exponentially with increasing membrane potential, the current is then decreased when C_4 is discharged by M4 with control voltage V_{B}. This sudden increase and decrease of shunting currents generate a spike. The spike output is obtained by the current of transistor M2 and converted to voltage by the diode-connected transistor M3. For the detailed dynamics and mathematical explanations, see ref. [6].

Figure 3 shows a MOS circuit for a depressing synapse constructed with a pMOS current mirror (M3, M4 and M5) and pMOS common-source amplifier (M2 and M4). It should be noticed that M4 of the common-source amplifier is shared by the current mirror with M5. When there is no input (current), voltage V_{e} at junction A is zero because of a leak current from transistor M2. Therefore, transistor

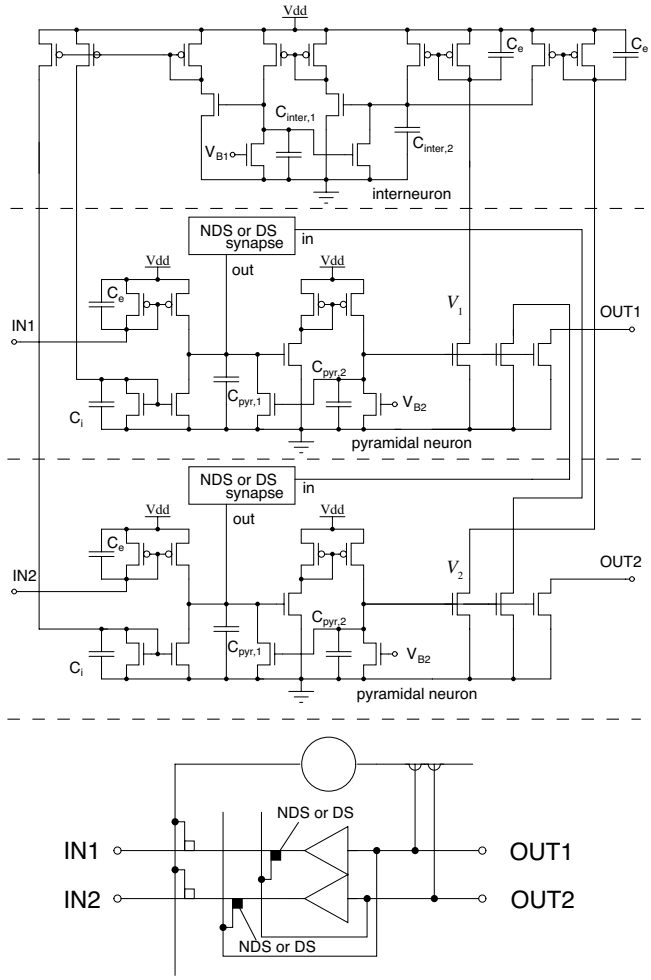

Fig. 4 Circuit diagram of network model with two pyramidal neurons and one interneuron: Each pyramidal neuron circuit has positive feedback connection through nondepressing (NDS) or depressing synapses (DS).

M1 is on. When there is an input current that increases $V_{\rm e}$, M1 is turned off. The current is therefore mirrored to output $I_{\rm out}$ through transistor $\rm M_1$. Because there is a parasitic capacitance ($C_{\rm dep}$) at junction A, the increase in $V_{\rm e}$ has a short time delay. Therefore, M1 is turned on for a short time, and the output current is generated. When the input current becomes zero again, M2 discharges the capacitance $C_{\rm dep}$, and $V_{\rm e}$ returns to zero. Remarkably, the Mirror effect of the pMOS common-source amplifier, which amplifies the value of additional parasitic capacitance between the drain and gate terminal of M4, increases this discharging time. When the spike current is given at a short interval and subsequent spikes enter before $V_{\rm e}$ returns to zero, the amplitude of the output spikes decreases when $V_{\rm e}$ increases. Because the current of transistor M2 increases monotonically when $V_{\rm B}$ increases, the time until $V_{\rm e}$ returns to zero decreases. Thus by adjusting voltage $V_{\rm B}$, the duration of the depression can be changed. Notice that, when $V_{\rm B}$ is

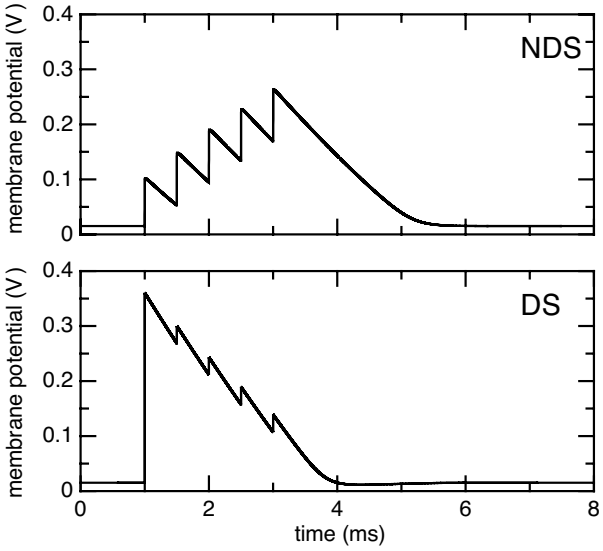

Fig. 5 Membrane potentials of pyramidal neuron circuits for short time input spike trains through nondepressing (NDS) or depressing synapses (DS)

set t0 $V_{\rm dd}$, the circuit behaves as a nondepressing synapse because $V_{\rm e}$ is zero and M1 is always on.

Neural network hardware that is qualitatively equivalent to the network model shown in Fig. 1 is illustrated in Fig. 4. To evaluate basic operations of the network hardware, we used two silicon neurons for pyramidal neurons and one silicon neuron for an interneuron. Outputs of the pyramidal neuron circuits are sent to the interneuron circuit through nondepressing excitatory synapses constructed with pMOS current mirrors, whereas the output of the interneuron circuit is connected to nondepressing inhibitory synapses (nMOS current mirrors) of the pyramidal neuron circuits. Outputs of the pyramidal neuron circuits are also fed back to themselves through nondepressing or depressing synapses, each of which is an excitatory connection. The network accepts external spikes at terminals IN1 and IN2 and produces the output spikes at terminals OUT1 and OUT2.

3. Circuit Simulation Results

We used a simulation program with integrated circuit emphasis (SPICE) to evaluate the proposed circuit with MOSIS parameters (Vendor AMIS, feature size: 1.5 μm). All the transistor dimensions (channel width and length) were fixed at 2.3 and 1.5 μm, except for the channel length of M5 in depressing synapse circuits. To compare the effects of depressing synapses on timing precision of synchronization among pyramidal neurons, we evaluated the network with nondepressing and depressing synapses for feedback connections between pyramidal neurons.

Figure 5 shows membrane potentials of a pyramidal neuron circuit in response to short time burst spike inputs (five spikes with interspike intervals of 500 μs) through

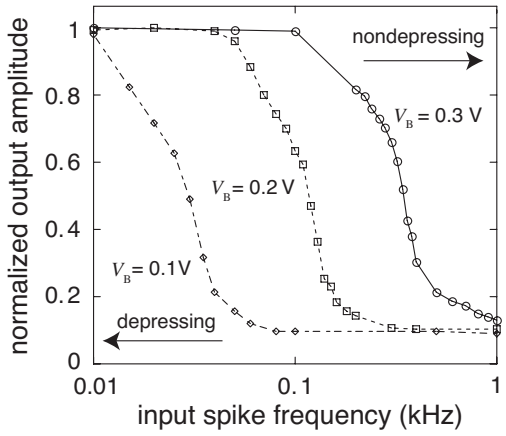

Fig. 6 Changes in amplitude of output of depressing synapse circuit against firing rate of presynaptic neuron

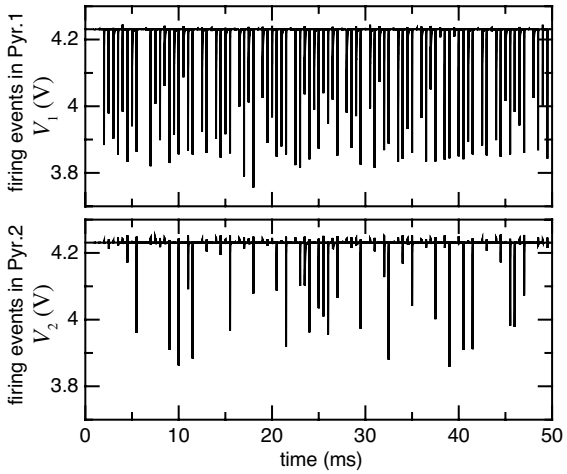

Fig. 7 Output spike trains of pyramidal neuron circuits with nondepressing synapses

nondepressing and depressing synapse circuits. Amplitudes of spike inputs, $V_{\rm dd}$, $C_{\rm dep}$, and $V_{\rm B}$ were set at 10 nA, 5 V, 100 fF, and 350 mV. The channel length of M5 was set at 3 μm for depressing synapses and 6.5 μm for nondepressing synapses, which evoked on average the same excitatory postsynaptic potential (EPSP), i.e., charges in membrane capacitances during the burst spike input were fixed to constant values regardless of the type of synapse (nondepressing or depressing). This result ensures that the EPSP generated by the depressing synapse circuit has a larger response at the burst onset than that of the nondepressing synapse circuit. Figure 6 shows the change in amplitude of the output spike against the input firing rate where $V_{\rm B}$ was set at 0.1, 0.2, and 0.3 V. As the spike frequency increases, the amplitude of the output pulse decreased. By increasing $V_{\rm B}$, the cutoff frequency was successfully shifted toward the higher frequency (toward the nondepressing operation).

Based on the extracted parameter results of nondepressing and depressing synapse circuits, we evaluated the

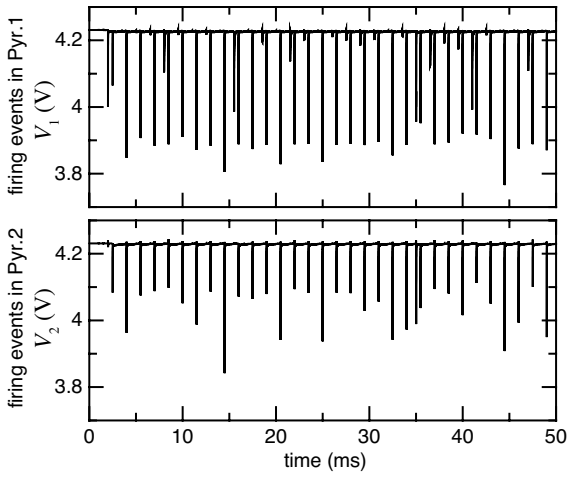

Fig. 8 Output spike trains of pyramidal neuron circuits with depressing synapses

Table 1 Comparison of results averaged timing jitters and their standard deviations (σ^2) between nondepressing (NDS) and depressing synapses (DS)

	NDS	DS
average jitter (μs)	0.92	0.82
σ^2 (μs)	0.36	0.21

timing precision of synchronization in the network. In the following simulations, the input spike frequency was fixed at 2 kHz. Capacitance values of $C_{\rm inter,1}$, $C_{\rm inter,2}$, $C_{\rm pyr,1}$, and $C_{\rm pyr,2}$ were set at 1 pF, 100 fF, 300 fF, and 1 pF, whereas capacitors of nondepressing inhibitory and excitatory synapses were removed in this simulation ($C_{\rm i} = C_{\rm e} = 0$). The neuron's bias voltages $V_{\rm B1}$ and $V_{\rm B2}$ were set at 650 and 560 mV. Figures 7 and 8 show output spike trains of pyramidal neuron circuits (V_1 and V_2 in Fig. 4) when nondepressing and depressing synapses were used to connect pyramidal neurons to each other. In both figures, each pyramidal neuron circuit tends to be synchronized in the phase space. For a simple evaluation of the synchronization, we calculated

$$S(t) = H(V_1(t) - \theta) \times H(V_2(t) - \theta) \qquad (1)$$

where $H(\cdot)$ represents the step function and $\theta = 4.2$ V. When V_1 and V_2 are fired simultaneously at time t, $S(t)$ becomes 1. Normalizing neuron circuit's intrinsic firing frequency at the ratio of 3 μm (depressing) to 6.5 μm (nondepressing), $\sum_{t=0}^{40\ \rm ms} S(t)$ was 6 for nondepressing whereas it was 17 for depressing synapses, which quantitatively showed an improved synchronization between neuron circuits when depressing synapses were used. We also calculated the timing jitters of output spikes of pyramidal neuron circuits. Table 1 shows a comparison of the results of averaged timing jitters and their standard deviations (σ^2) between nondepressing and depressing synapses. We

found that when depressing synapse circuits were used, the average jitter was 0.1 μs better than that of nondepressing synapse circuits. In addition, values of the standard deviation were 60 % better than those of nondepressing synapse circuits. Therefore, we concluded that depressing synapse circuits improve the timing precision of synchronization. Remember that an EPSP generated by a depressing synapse circuit has a larger response at a spike onset than that of a nondepressing synapse circuit (Fig. 5). When nondepressing synapses are used, several spikes are required to evoke enough EPSPs to fire, whereas EPSPs evoked by depressing synapses easily make a pyramidal neuron fire with a few spikes, e.g., even a single spike is sufficient if the threshold potential is set at a very low value. The resultant firing gives rise to the subsequent firing of other pyramidal neurons, which results in fast synchronization among all of the pyramidal neurons.

Synaptic depression is indeed able to detect partial synchrony in the burst times [8]. With nondepressing synapses, the postsynaptic membrane potential follows the presynaptic mean firing rate and is able to be set continuously below the threshold of a neuron. With depressing synapses, however, the partially synchronized bursts push the postsynaptic membrane potential across the threshold repeatedly during stimulus.

4. MOS Circuit for STDP Learning

According to the Hebb principle, synapses increase their efficacy if two connected neurons are simultaneously fired. Simultaneous is to be defined by some time window of coincidence. This window of coincidence has being a function of the exact timing of the activity of the presynaptic and postsynaptic neuron, and this phenomenon is called spike-timing-dependent plasticity (STDP). By introducing STDP learning in the original network, Fukai and Kanemura demonstrated that the network exhibited robust synchronization in a noisy environment [1]. In this section, we propose a novel analog circuit emulating the STDP learning. The circuit consists of two basic circuits: a spike-timing detector and an analog memory circuit.

To construct a spike-timing detector, we used a simple correlation neural network [9–11]. Figure 9 shows a local correlation scheme used to account for timing-sensitive responses of output neurons to input spike trains. A primitive correlation neural network consists of two input neurons (P_1 and P_2), a delay neuron (D), and a correlator (C), as shown in Fig. 9(a). The arrival of spikes from P_1 at the correlator is delayed by the delay neuron. The output is a correlation value representing the product of delayed and undelayed signals from D and P_2.

When an input spike is given to P_1 and then to P_2 within the time t_s, which is longer than the delay time t_d, the delayed and undelayed signals from D and P_2 do not coincide at the correlator, as shown in Fig. 9(b). If an input spike is given to P_1 and then to P_2 in a time equal to the delay time, the delayed and undelayed signals coincide at the correlator [Fig. 9(c)]. Namely, the output signal of the correlator reaches its maximum at the point of coincidence. On the other hand, if an input is given to P_1 and then to P_2 in a time shorter than the delay time, the output signal monotonically decreases as the time decreases [Fig. 9(d)]. Thus, the network can measure the degree of temporal difference by monotonically increasing output signals as the spike intervals between P_1 and P_2 decrease.

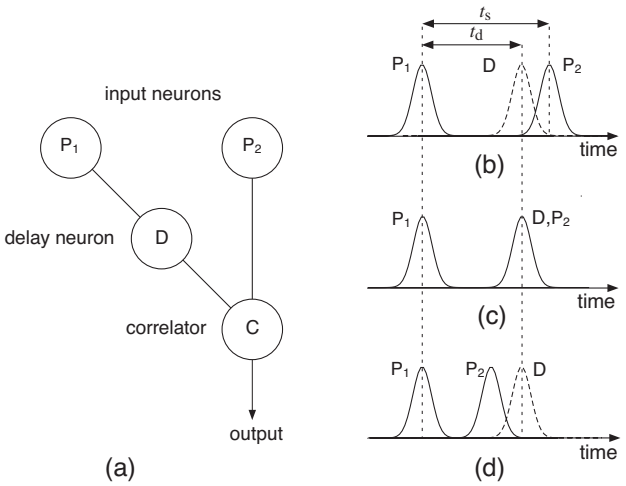

Fig. 9 Primitive correlation neural network consisting of two input neurons (P_1 and P_2), delay neuron (D), and correlator (C)

Figure 10 show a circuit diagram of spike-timing detectors implementing the correlation neural networks. The circuit consists of a delay circuit (a source-common amplifier and a capacitor), which we denote CMA in Fig. 10(b); a pMOS unity-gain amplifier (UGA); and a current converter (diode-connected MOS transistor DCM). A circuit shown in Figs. 10(a) and (b) detects sequential inputs of pre-to-post spikes. If one spike input is given to terminal **pre** and then the subsequent spike input is given to terminal **post** ($t_{\rm post} - t_{\rm pre} \equiv \Delta t > 0$), $V_{\rm pot}$ increases because input of terminal **pre** is delayed by the source-common amplifier, while the unity-gain amplifier that accepts the delayed voltage is driven by the **post** input. Note that the source-common circuit amplifies not only the pre voltage input but also the decay time due to the Miller effect. Since the output of the unity-gain amplifier ($V_{\rm pot}$) is sent to a diode-connected nMOS transistor, we can obtain a current output as a result of the current inputs (terminals **pre** and **post**). Similarly, Figs. 10(c) and (d) show the inverted circuit of Figs. 10(a) and (b) that detects sequential inputs of post-to-pre spikes ($\Delta t < 0$).

An analog memory circuit for STDP learning is illustrated in Fig. 11. The circuit consists of a pMOS differential pair, a storage capacitor ($C_{\rm memory}$), and pMOS and nMOS current sources that receive the output of spike-timing detectors ($V_{\rm pot}$ and $V_{\rm dep}$) constructing pMOS and nMOS current mirrors. The storage capacitor is dis-

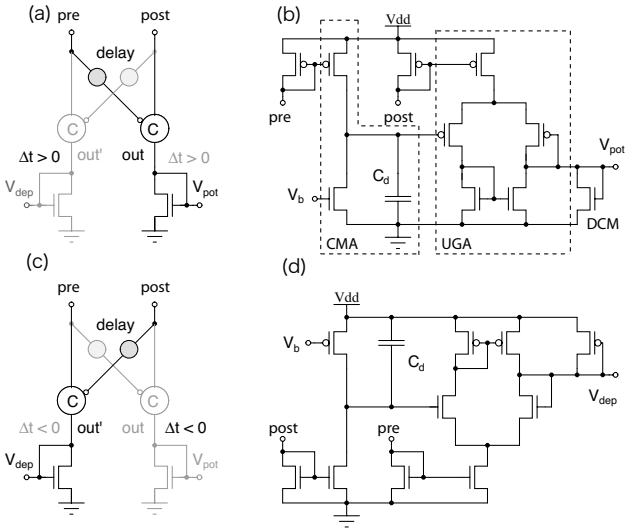

Fig. 10 Spike-timing detectors

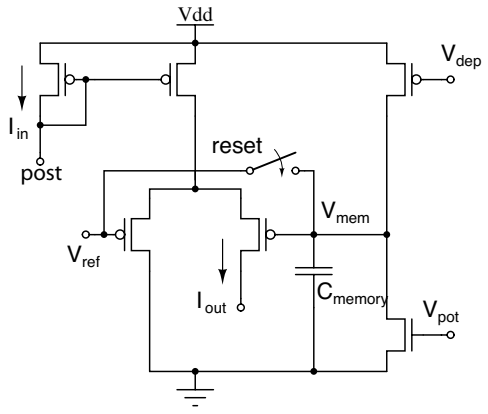

Fig. 11 Analog memory circuit for weight storage

charged (or charged) by pre-to-post (or post-to-pre) input spikes through $V_{\rm pot}$ (or $V_{\rm dep}$), e.g., when $\Delta t > 0$, $V_{\rm pot}$ is increased and thus the storage capacitor is discharged. Synaptic weight strength w between pre and post neurons is defined by the ratio of input current $I_{\rm in}$ to output current $I_{\rm out}$ and controlled by the difference between capacitor voltage $V_{\rm mem}$ and reference voltage $V_{\rm ref}$. Initially $V_{\rm mem}$ is set to $V_{\rm ref}$ by manual reset switching, i.e., $I_{\rm out} = I_{\rm in}/2$ and thus $w = 2$. When all the transistors operate in their subthreshold regions, weight strength w is given by

$$w = \frac{I_{\rm in}}{I_{\rm out}} = \frac{1}{f(V_{\rm mem} - V_{\rm ref})}$$
$$\left[f(x) = \frac{1}{1 + \exp(-\kappa x / V_T)} \right]$$

where κ represents the effectiveness of the gate potential, and $V_T \equiv kT/q \approx 26$ mV at room temperature (k is Boltzmann's constant, T the temperature, and q the electron charge) [12, 13].

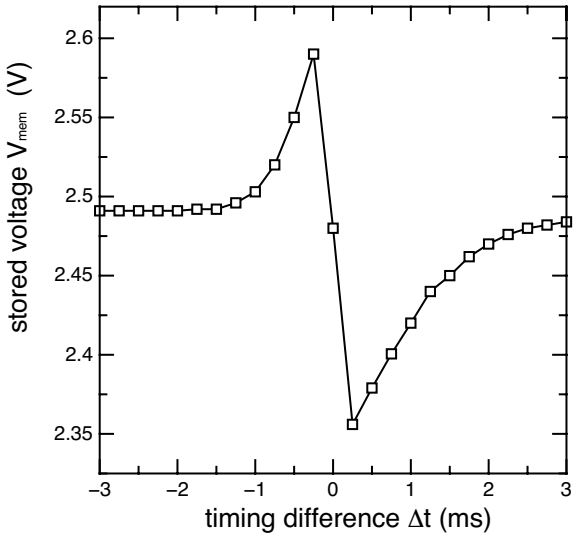

Fig. 12 Simulation results of STDP circuit

Figure 12 shows simulation results of the proposed STDP circuit. The horizontal and vertical axes represent $t_{\rm post} - t_{\rm pre}$ (Δt) and capacitor voltage $V_{\rm mem}$. The power-supply and reference voltages were set at 5 and 2.5 V. The memory capacitance value was set at 500 fF. As expected, the circuit mimicked basic characteristics of STDP learning; however, the asymmetry characteristic was observed. This is simply due to the unbalanced saturating properties of pMOS and nMOS current sources in Fig. 11, which could be improved by using relatively long channels for the current sources.

5. Conclusion

We designed a neural network circuit to demonstrate precisely timed synchronization among silicon neurons with depressing synapse circuits. The network circuit was designed using popular metal-oxide-semiconductor (MOS) devices. The key to synchronizing neurons precisely was introducing positive feedback to the neurons and using depressing synapses instead of nondepressing (conventional) synapses for the feedback connections. Consequently, in our demonstration assuming a 1.5-μm CMOS process, precision was improved by 60% when depressing synapse circuits were used instead of nondepressing synapses. Furthermore, we designed a novel synapse circuit that qualitatively mimics spike-timing dependent plasticity (STDP) learning characteristics. By circuit simulations, we demonstrated the learning characteristics.

Acknowledgments

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