

PAPER

# Critical Temperature Sensor Based on Oscillatory Neuron Models

Gessyca Maria Tovar, Tetsuya Asai, Tetsuya Hirose and Yoshihito Amemiya

Graduate School of Information Science and Technology, Hokkaido University  
 Kita 14, Nishi 9, Kita-ku, Sapporo 060-0814, Japan  
 E-mail: gessyca@sapiens-ei.eng.hokudai.ac.jp

**Abstract** We developed a critical temperature sensor that can be implemented on monolithic CMOS IC. The circuit consists of subthreshold CMOS circuits whose dynamical behavior changes at a given threshold temperature, i.e., switches to and from oscillatory and stationary. The threshold temperature is set to a desired value by adjusting an external bias voltage. The circuit operation was investigated through theoretical analysis, numerical simulations and circuit simulations using the Simulation Program of Integrated Circuit Emphasis (SPICE). We experimentally demonstrate the operation of the proposed circuit using discrete MOS devices.

**Keywords:** neuromorphic LSI, spiking neurons, oscillator

## 1. Introduction

Temperature is the most often-measured environmental quality. This might be expected since temperature control is fundamental to the operation of electronic and other systems. In the present, there are several passive and active sensors for measuring system temperatures, including thermocouples, resistive-temperature detectors (RTDs), thermistors, and silicon temperature sensors [1]. Among present temperature sensors, thermistors with a positive temperature coefficient (PTC) are widely used because they exhibit a sharp increase of resistance at a specific temperature. Therefore, PTC thermistors are suitable for implementation in temperature-control systems that make decisions, like shutting down equipments above a certain threshold temperature or to turning cooling fans on and off, general purpose temperature monitors.

The temperature characteristics of PTC thermistors made of ceramic material are determined by the material's characteristics and its relative proportions [1, 2]. Therefore, electrical resistivities of PTCs are shifted due to a phenomenon called leaching, which occurs during soldering processes. In addition to the resistance shift, leaching also causes degradation of solder-electrodes and electrode-semiconductor bonds, which may result in thermistors having greatly reduced stability and reliability. To avoid these post-manufacture effects, we have developed a critical temperature sensor that can be implemented on monolithic CMOS ICs. The sensor has a sharp transition characteristic similar to that of PTC thermistors. Key features of the circuit include low-power subthreshold operation of MOSFETs, extended range of threshold temperatures, and small packages. In this paper we demonstrated the operation of the sensor through theoretical analysis, nu-

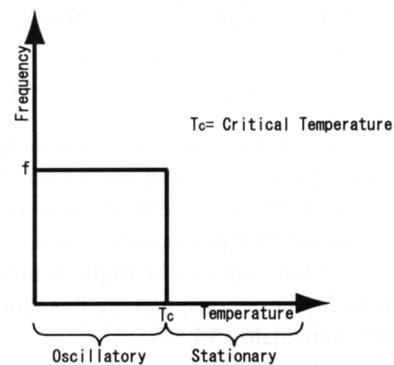


Fig. 1 Critical temperature sensor operation model

merical and circuit simulations using the Simulation Program of Integrated Circuit Emphasis (SPICE). Moreover, we experimentally confirmed the operation of the circuit using discrete MOS devices.

## 2. The Model

The temperature sensor operation model is shown in Fig. 1. The model consists of a nonlinear neural oscillator that changes its state between oscillatory and stationary when it receives an external perturbation (temperature). The key idea is the use of excitable circuits that are strongly inspired by the operation of biological neurons. A temperature increase causes a regular and reproducible increase in the frequency of the generation of pacemaker potential in most *Aplysia* and *Helix* excitable neurons [3]. Generation of the activity pattern of the Br-type neuron located in the right parietal ganglion

of *Helix pomatia* is a temperature-dependent process. The Br neuron shows its characteristic bursting activity only between 12 and 30°C. Outside this range, the burst pattern disappears and the action potentials become regular. This means that excitable neurons can be used as sensors to determine temperature ranges in a natural environment.

There are many models of excitable neurons, but only a few of them have been implemented on CMOS LSIs, e.g., silicon neurons that emulate cortical pyramidal neurons [4], FitzHugh-Nagumo neurons with negative resistive circuits [5], artificial neuron circuits based on by-products of conventional digital circuits [6, 7, 8], and ultralow-power subthreshold neuron circuits [9]. Our model is based on the Wilson-Cowan system [10] because it is easy to both analyze theoretically and implement in subthreshold CMOS circuits.

The dynamics of the temperature sensor can be expressed as:

$$\tau \dot{u} = -u + \frac{\exp(u/A)}{\exp(u/A) + \exp(v/A)} \quad (1)$$

$$\dot{v} = -v + \frac{\exp(u/A)}{\exp(u/A) + \exp(\theta/A)} \quad (2)$$

where  $\tau$  represents the time constant,  $\theta$  is an external input, and  $A$  is a constant proportional to temperature. The second term of the r.h.s. of Eq.(1) represents the sigmoid function, a mathematical function that produces an S-shaped (sigmoid) curve. The sigmoid function can be implemented in VLSIs by using differential-pair circuits, making this model suitable for implementation in analog VLSIs.

To analyze the system operation, it is necessary to calculate its nullclines. Nullclines are curves in the phase space where the differentials  $\dot{u}$  and  $\dot{v}$  are equal to zero. The nullclines divide the phase space into four regions. In each region the vector field follows a specific direction. Along the curves the vector field is either completely horizontal or vertical; on the  $u$  nullcline the direction of the vector is vertical; and on the  $v$  nullcline, it is horizontal. The  $u$  and  $v$  nullclines indicating the direction of vector field in each region are shown in Fig. 2.

The trajectory of the system depends on the time constant  $\tau$ , which modifies the velocity field of  $u$ . In Eq. (1), if  $\tau$  is large, the value of  $u$  decreases, and for small  $\tau$ ,  $u$  increases. Figures 3(a) and (b) show trajectories when  $\tau = 1$  and  $\tau \ll 1$ . In the case where  $\tau \ll 1$ , the trajectory on the  $u$  direction is much faster than that in the  $v$ , so only close to the  $u$  nullcline movements of vectors in vertical direction are possible.

Let us suppose that  $\theta$  is set at a certain value where the critical temperature ( $T_c$ ), which is proportional to  $A$  is 27°C. The critical temperature represents the threshold temperature we desire to measure. When  $\theta$  changes, the  $v$  nullcline changes to a point where the system will be stable as long as the external temperature is higher than  $T_c$ . This is true because the

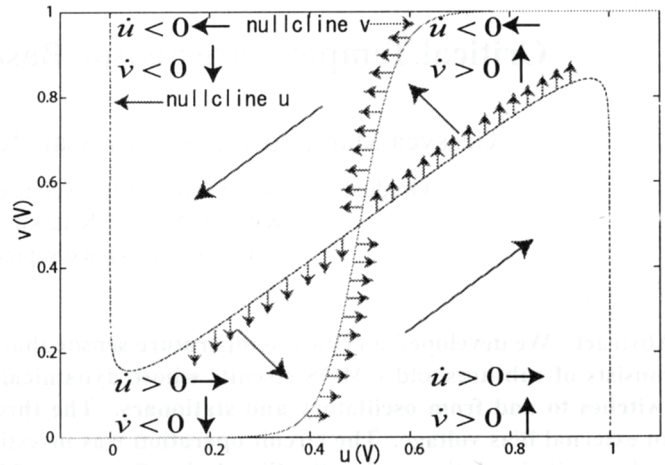


Fig. 2  $u$  and  $v$  nullclines with vector field direction

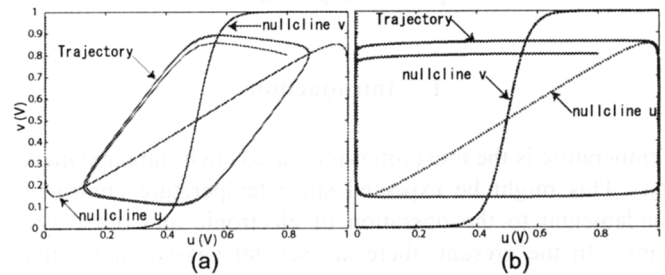


Fig. 3 Trajectory when a)  $\tau = 1$  and b)  $\tau \ll 1$

system is unstable only when the fixed point exists in a negative resistive region of the  $u$  nullcline. The fixed point, defined by  $\dot{u} = \dot{v} = 0$  is represented in the phase space by the intersection of the  $u$  nullcline with the  $v$  nullcline. At this point the trajectory stops because the vector field is zero, and the system is thus stable. On the other hand, when the external temperature is below  $T_c$ , the nullclines move, and this will correspond to a periodic solution to the system. In the phase space we can observe that the trajectory does not pass through the fixed point but describes a closed orbit or limit cycle, indicating that the system is oscillatory. Figure 4 shows examples when the system is stable (a) and oscillatory (b). In (a) the external temperature is greater than the critical temperature, hence, the trajectory stops when it reaches the fixed point, and the system is stable. In (b), where the temperature changes below the critical temperature, the trajectory avoids the fixed point, and the system becomes oscillatory.

Deriving the nullclines equation ( $\dot{u} = 0$ ) and equaling to zero, we calculated the local minimum ( $u_-, v_-$ ) and local maximum ( $u_+, v_+$ ), representing the intersection point of the nullclines given by:

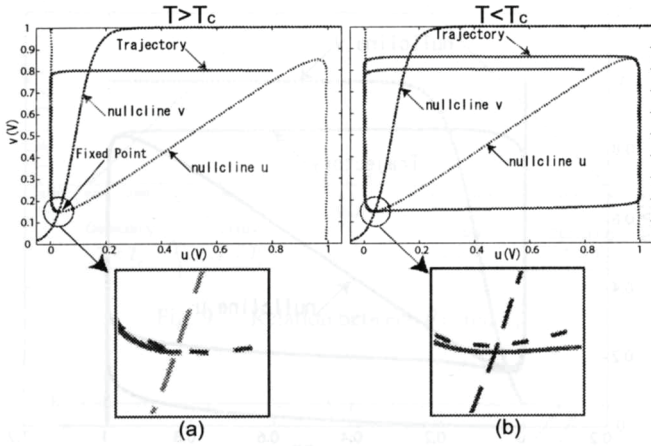


Fig. 4 Nullclines showing the fixed point and the trajectory when a) system is stable b) system is oscillatory

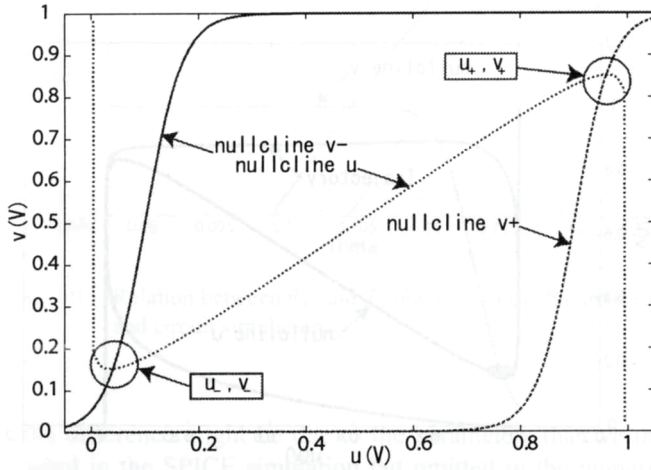


Fig. 5  $u$  and  $v$  local maximum and local minimum

$$u_{\pm} = \frac{1 \pm \sqrt{1 - 4A}}{2} \quad (3)$$

$$v_{\pm} = u_{\pm} + A \ln\left(\frac{1}{u_{\pm}} - 1\right) \quad (4)$$

The nullclines giving the local minimum and local maximum ( $u_{\pm}, v_{\pm}$ ) are shown in Fig. 5.

From the local minimum and maximum equations (Eq. (3) and Eq. (4)), the nullcline equation ( $\dot{v} = 0$ ) and remembering that  $A$  is proportional to temperature, we determined the relationship between  $\theta$  and the temperature, to be given by:

$$\theta_{\pm} = u_{\pm} + A \ln\left(\frac{1}{v_{\pm}} - 1\right) \quad (5)$$

When  $\tau \ll 1$  the trajectory jumps from one side to the other side of the  $u$  nullcline, so only along the  $u$  nullcline movement in the  $v$  direction are possible as shown in Fig. 3(b). It is necessary to emphasize this fact because this characteristic is necessary for the system operation; thus, we assume  $\tau \ll 1$ .

### 3. CMOS Circuit

The critical temperature sensor circuit is shown in Fig. 6. The sensor section consists of two pMOS differential pairs ( $M_1 - M_2$  and  $M_3 - M_4$ ) operating in their subthreshold region. External components are required for the operation of the circuit. These components consist of two capacitors ( $C_1$  and  $C_2$ ) and two temperature-insensitive off-chip metal-film resistors ( $g$ ). In addition, for the experimental purpose, two current mirrors were used as the bias current of differential pairs. Note that for the final implementation of our critical temperature sensor a current reference circuit with low-temperature dependence [11] should be used.

Differential-pairs subthreshold currents,  $I_1$  and  $I_2$ , are given by [12]:

$$I_1 = I_a \frac{\exp(\kappa u/v_T)}{\exp(\kappa u/v_T) + \exp(\kappa v/v_T)} \quad (6)$$

$$I_2 = I_a \frac{\exp(\kappa u/v_T)}{\exp(\kappa u/v_T) + \exp(\kappa \theta/v_T)} \quad (7)$$

where  $I_a$  represents the differential pairs bias current,  $v_T$  is the thermal voltage ( $v_T = kT/q$ ),  $k$  is the Boltzmann's constant,  $T$  is the temperature, and  $q$  is the elementary charge.

The circuit dynamics can be determined by applying Kirchhoff's current law to both differential pairs, which is represented as follows:

$$C_1 \dot{u} = -gu + \frac{I_a \exp(\kappa u/v_T)}{\exp(\kappa u/v_T) + \exp(\kappa v/v_T)} \quad (8)$$

$$C_2 \dot{v} = -gv + \frac{I_a \exp(\kappa u/v_T)}{\exp(\kappa u/v_T) + \exp(\kappa \theta/v_T)} \quad (9)$$

where  $\kappa$  is the subthreshold slope,  $C_1$  and  $C_2$  are the capacitances representing the time constants, and  $\theta$  is bias voltage.

Note that Eqs. (8) and (9) correspond to the system dynamics (Eqs. (1) and (2)) previously explained. Therefore, applying the same analysis, we calculated the local minimum ( $u_-, v_-$ ) and local maximum ( $u_+, v_+$ ) for the circuit equations, expressed by:

$$u_{\pm} = \frac{I_a/g \pm \sqrt{(I_a/g)^2 - 4v_T I_a/(\kappa g)}}{2} \quad (10)$$

$$v_{\pm} = u_{\pm} + \frac{v_T}{\kappa} \ln\left(\frac{I_a}{g u_{\pm}} - 1\right) \quad (11)$$

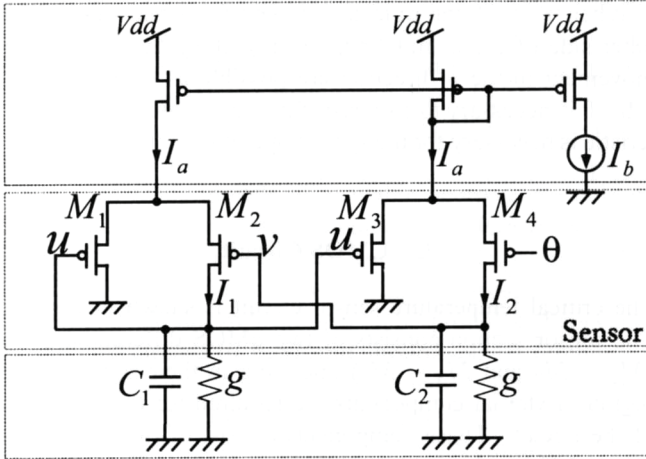


Fig. 6 Critical temperature sensor circuit

and the relationship between the external bias voltage ( $\theta$ ) and the external temperature ( $T$ ):

$$\theta_{\pm} = u_{\pm} + \frac{v_T}{\kappa} \ln \left( \frac{I_a}{g v_{\pm}} - 1 \right) \quad (12)$$

where the relation with the temperature is given by the thermal voltage defined by  $v_T = kT/q$ . At this point the system temperature is equal to the critical temperature which can be obtained from:

$$T_c = \frac{q\kappa(\theta_{\pm} - u_{\pm})}{k \ln \left( \frac{I_a}{g v_{\pm}} - 1 \right)} \quad (13)$$

The threshold temperature  $T_c$  can be set to a desired value by adjusting the external bias voltage ( $\theta$ ). The circuit changes its dynamic behavior, i.e., oscillatory or stationary behaviors, depending on its operation temperature and bias voltage conditions. At temperatures lower than  $T_c$  the circuit oscillates, but the circuit is stable (does not oscillate) at temperatures higher than  $T_c$ .

#### 4. Simulations and Experimental Results

Circuit simulations were conducted by setting  $C_1$  and  $C_2$  to 0.1 pF and 10 pF, respectively,  $g$  to 1 nS, and reference current ( $I_b$ ) to 1 nA. Note that for the numerical and circuit simulations, two current sources were used instead of the current mirrors. The parameter sets we used for the transistors were obtained from MOSIS AMIS 1.5- $\mu\text{m}$  CMOS process. Transistor sizes were fixed at  $L = 40 \mu\text{m}$  and  $W = 16 \mu\text{m}$ . The supply voltage was set at 5 V. Figure 7 shows the nullclines and trajectory of the circuit with the bias voltage ( $\theta$ ) set at 200 mV and the external temperature ( $T$ ) set at 27°C; the system was in oscillatory state. Figure 8 shows the nullclines when the system is stationary with the bias voltage ( $\theta$ ) set at 90 mV.

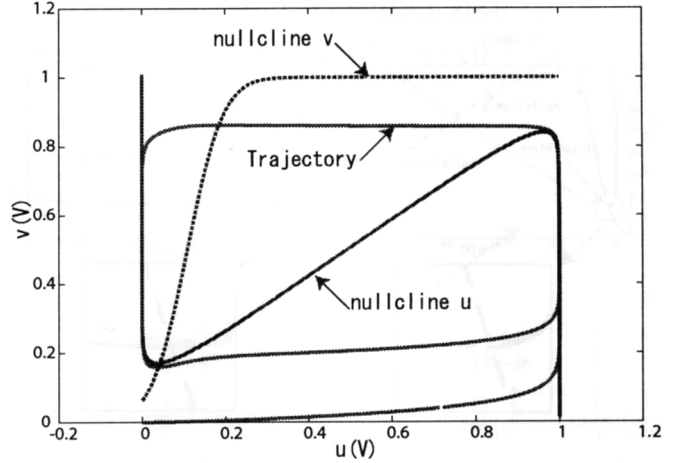


Fig. 7 Trajectory and nullclines obtained through simulation results when the system is oscillatory

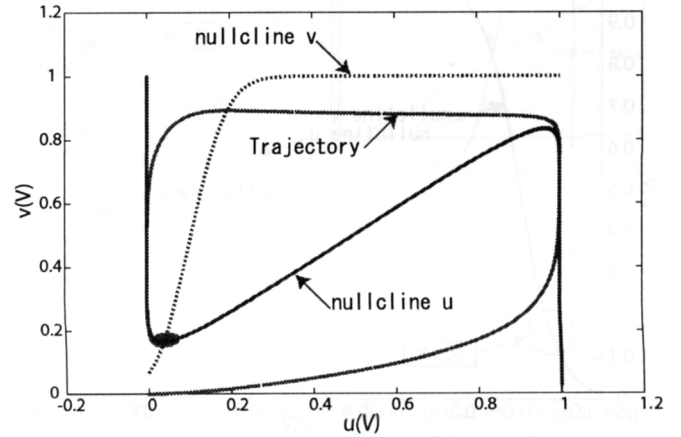


Fig. 8 Simulation results when the system is stationary

Through numerical simulations with  $\kappa = 0.75$ , by setting the values for the critical temperature ( $T_c$ ) and changing the bias voltage ( $\theta$ ) until the system changed its state, we established a numerical relation between  $T_c$  and  $\theta$ ;  $\theta_-$  for  $u$  and  $v$  local minimums and  $\theta_+$  for  $u$  and  $v$  local maximums. The relation between the bias voltage  $\theta_{\pm}$  and the critical temperature  $T_c$  is shown in Fig. 9. When  $\theta_-$  is used to set  $T_c$ , the system is stable at external temperatures higher than  $T_c$ ; while when  $\theta_+$  is used, the system is stable when the external temperature is lower than  $T_c$  and oscillatory when it is higher than  $T_c$ .

When comparing the relationship between  $\theta$  and  $T_c$  obtained through different methods, we found a mismatch between the numerical simulations and the circuit simulations.

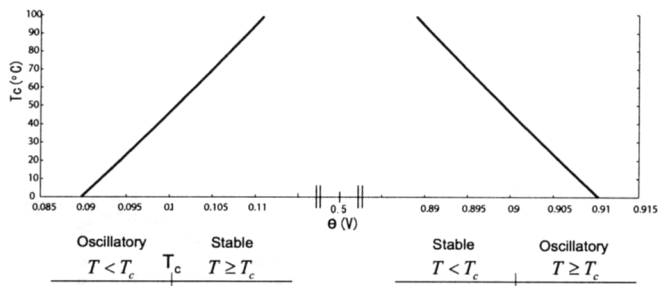


Fig. 9 Relation between  $\theta_{\pm}$  and  $T_c$

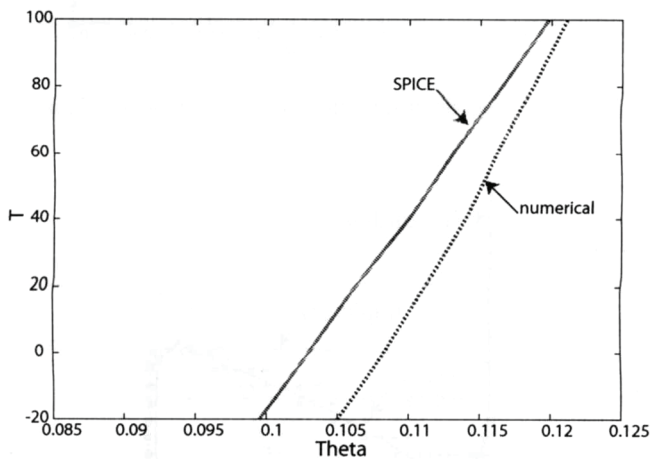


Fig. 10 Relation between  $\theta_{\pm}$  and  $T_c$  obtained through numerical and circuit simulations

This difference might be due to the parameters that we included in the SPICE simulation but omitted in the numerical simulation and theoretical analysis. Many of these parameters might be temperature dependent; thus, their value changes with temperature, and as a result of this change, the  $T_c$  characteristic changes. The difference between the two simulations is shown in Fig. 10.

We successfully demonstrated the critical temperature sensor's operation using discrete MOS circuits. Parasitic capacitances and a capacitance of  $0.033 \mu\text{F}$  were used for  $C_1$  and  $C_2$  respectively, and the resistances ( $g$ ) were set to  $10 \text{ M}\Omega$ . The input current ( $I_b$ ) for the current mirrors was set to  $100 \text{ nA}$  and we obtained an output current ( $I_a$ ) of  $78 \text{ nA}$ .

Measurements were performed at room temperature ( $T = 23^\circ\text{C}$ ). With the bias voltage ( $\theta$ ) set to  $500 \text{ mV}$  the voltages of  $u$  and  $v$  were measured. Under these conditions, the circuit was oscillating. The voltages of  $u$  and  $v$  for different values of  $\theta$  were also measured. The results showed that for values of  $\theta$  lower than  $170 \text{ mV}$ , the circuit did not oscillate (was stable), but that for values higher than  $170 \text{ mV}$ , the circuit became oscillatory. Figures 11 and 12 shows the oscillatory and stable states of  $u$  and  $v$  with  $\theta$  set to  $170$  and  $150 \text{ mV}$ , respectively.

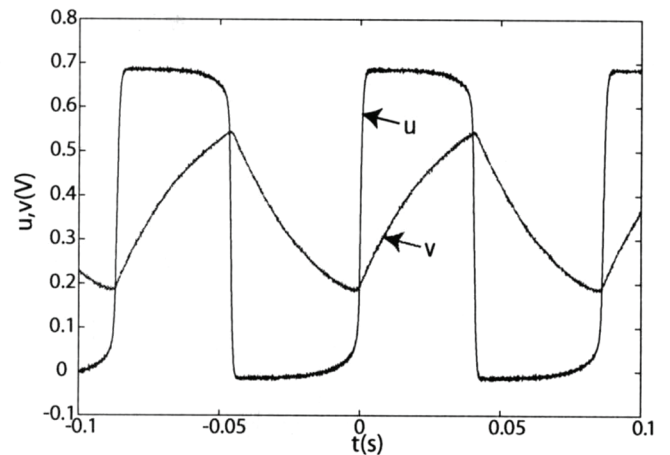


Fig. 11 Experimental results:  $\theta = 170 \text{ mV}$  at  $T = 23^\circ\text{C}$  (oscillatory state)

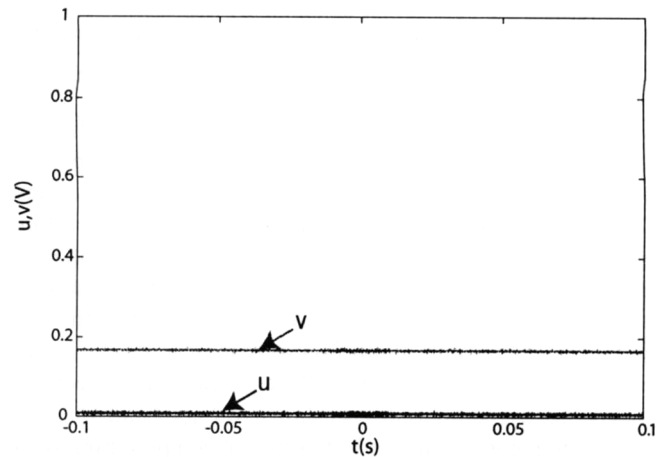


Fig. 12 Experimental results:  $\theta = 150 \text{ mV}$  at  $T = 23^\circ\text{C}$  (stationary state)

In addition, we also measured the nullclines (steady state voltage of the differential pairs). The  $v$  nullcline (steady state voltage  $v$  of differential pair  $M_3 - M_4$ ) was measured by applying a variable DC voltage (from  $0$  to  $1 \text{ V}$ ) on  $u$  and measuring the voltage on  $v$ . For the measurement of the  $u$  nullcline (steady state voltage  $u$  of differential pair  $M_1 - M_2$ ), a special configuration of the first differential pair of the circuit was used. Figure 13 shows the circuit used for the  $u$  nullcline measurement. We applied a variable DC voltage (from  $0$  to  $1 \text{ V}$ ) on  $v$ . For each value of  $v$  we changed the voltage on  $u_1$  (from  $0$  to  $1$ ) and then measured the voltage on  $u_o$  and  $u_1$ . This enabled us to obtain the  $u$  nullcline by plotting the points where  $u_o$  and  $u_1$  had almost the same value. In this way, we obtained a series of points showing the shape of the  $u$  nullcline. The series of points was divided into three sections, and

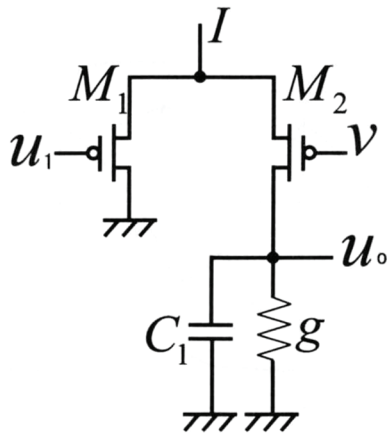


Fig. 13 Circuit used for calculation of the  $u$  nullcline

the average was calculated to show the  $u$  nullcline. Figure 14 shows the  $u$  nullcline divided into the three sections used for the average calculation. The trajectory and nullclines of the circuit with  $\theta$  set to 500 mV are shown in Fig. 15.

Notice that in the experimental results there is a difference in the amplitude of the potentials  $u$  and  $v$  with respect to results obtained from the numerical and circuit simulations. This is due to the difference in the bias current of the differential pairs. From Eqs. (10) and (11), we can see that by making  $g$  and  $I_b$  (used in numerical and circuit simulations) the same value, they cancel each other out; however, the output currents of the current mirrors were in the order of 78 nA, and  $g$  was set to 100 nS. This difference caused the decrease in the potentials amplitudes, as shown in Figs.7 and 15.

Measurements performed at different temperatures were made. The bias voltage ( $\theta$ ) was set to a fixed value and the external temperature was changed to find the value of the critical temperature ( $T_c$ ) where the circuit changes from one state to the other. With the bias voltage  $\theta$  set to 170 mV at room temperature ( $T = 23^\circ\text{C}$ ), the circuit oscillated. When the external temperature was increased to ( $T = 26^\circ\text{C}$ ), the circuit changed its state to stationary (did not oscillate). Once again, when the external temperature was decreased one degree ( $T = 25^\circ\text{C}$ ), the circuit started to oscillate; therefore, the critical temperature was  $T_c = 26^\circ\text{C}$ . Measures of the critical temperature ( $T_c$ ) for different values of the bias voltage ( $\theta$ ) were made.

In order to compare experimental results with theoretical ones, the actual  $\kappa$  (subthreshold slope) of the discrete MOS devices was measured and found to be in the order of 0.1. The critical temperature for each value of  $\theta$  obtained experimentally compared with the critical temperature obtained with theoretical analysis using Eq. (12) (with  $\kappa = 0.1$ ) is shown in Fig. 16. The curves have positive slopes in both cases. This is because the temperature difference between one value of bias voltage and the other decreases as the bias voltage increases. For  $\theta = 140$  and 150 mV the experimentally obtained

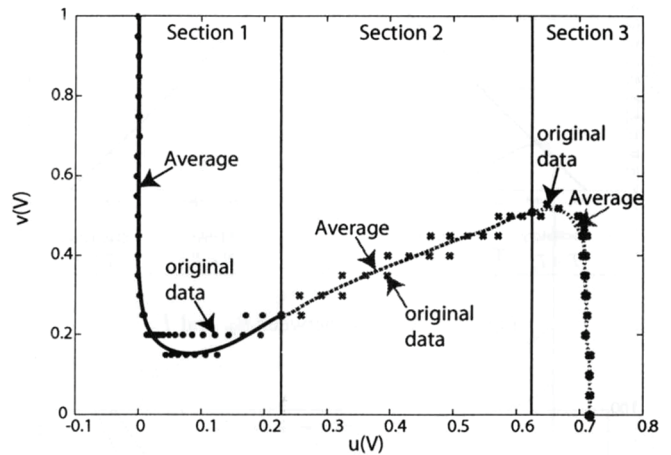


Fig. 14 Sections used for the calculation of the  $u$  nullcline

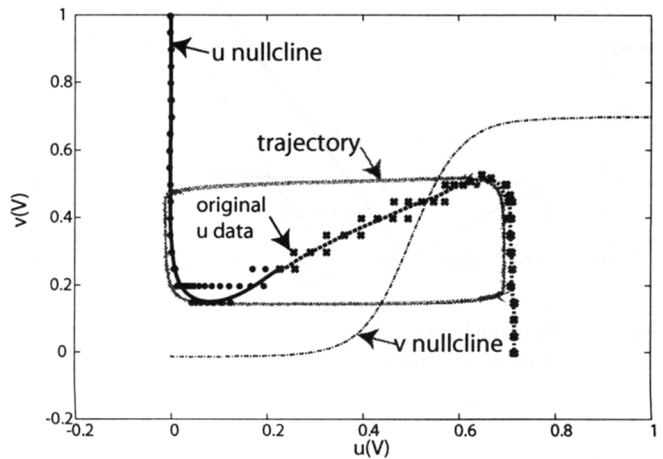


Fig. 15 Experimental nullclines and trajectory

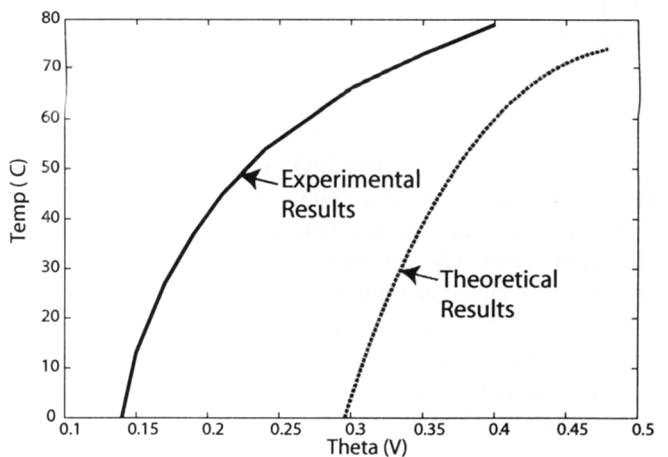


Fig. 16 Bias voltage vs temperature, experimental results

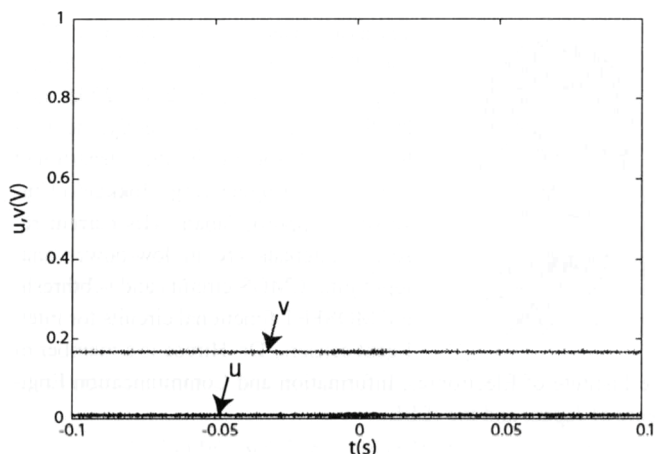


Fig. 17 Stationary state with  $\theta = 140$  mV and  $T = 23^\circ\text{C}$

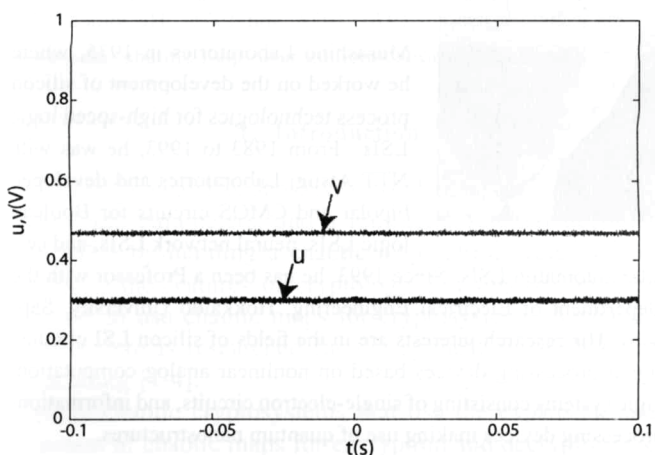


Fig. 18 Stationary state with  $\theta = 140$  mV and  $T = 75^\circ\text{C}$

critical temperatures ( $T_c$ ) are  $0^\circ\text{C}$  and  $13^\circ\text{C}$ , respectively, a difference of  $13^\circ\text{C}$ . For  $\theta = 240$  and  $250$  mV the critical temperatures ( $T_c$ ) are  $54^\circ\text{C}$  and  $56^\circ\text{C}$ , respectively: a difference of only  $2^\circ\text{C}$ .

The difference between the experimental and theoretical results is due to the leak current caused by plastic diodes between the source (drain) and the well or substrate of the discrete MOS devices. In addition, because of the leak current, when temperature increases, the stable voltages of  $u$  and  $v$  also increase. Figures 17 and 18 shows the stationary state with  $\theta$  set to 140 mV and temperature set to 23 and  $75^\circ\text{C}$ , respectively.

## 5. Conclusion

We developed a critical temperature sensor that can be implemented on monolithic CMOS ICs. The sensor consists of a

subthreshold CMOS circuit that changes its dynamic behavior, i.e., oscillatory or stationary behavior, at a given threshold temperature. We analyzed the circuit's operation theoretically and also conducted numerical and circuit simulations. Furthermore, the operation of the circuit was demonstrated using discrete MOS devices through experimental results. The threshold temperature ( $T_c$ ) was set to a desired value by adjusting the external bias voltage ( $\theta$ ). We demonstrated that the circuit changed its state between oscillatory and stationary when the external temperature was lower or higher than the critical temperature ( $T_c$ ). Moreover, we experimentally calculated the circuit nullclines, indicating the trajectory of the circuit when it is in oscillatory state.

## Acknowledgments

This study was partly supported by the Industrial Technology Research Grant Program in '04 from New Energy and Industrial Technology Development Organization (NEDO) of Japan, and a Grant-in-Aid for Young Scientists [(B)17760269] from the Ministry of Education, Culture Sports, Science and Technology (MEXT) of Japan.

## References

- [1] W. Gopel, J. Hesse and J. N. Zemel: Sensors. A comprehensive survey, T. Ricolfi and J. Scholz, Eds. Vol. 4, VCH, "Thermal sensors," pp. 235-239, 1990.
- [2] C. C. Wang, S. A. Akbar and M. J. Madou: Ceramic based resistive sensors, Vol. 2, No. 4, pp. 273-282, 1998.
- [3] D. S. Fletcher and L. J. Ram: High temperature induces reversible silence in *Aplysia* R15 bursting pacemaker neuron Comp. Biochem. Physiol. Vol. 98A, pp. 399-405, 1990.
- [4] R. Douglas, M. Mahowald and C. Mead: Neuromorphic analogue VLSI, Ann. Rev. Neurosci., Vol. 18, pp. 255-281, 1995.
- [5] B. L. Barranco, E. S. Sinencio, A. R. Vazquez and J. L. Huertas: A CMOS implementation of FitzHugh-Nagumo neuron model, IEEE J. Solid-State Circuits, Vol. 26, pp. 956-965, 1991.
- [6] S. Ryckebusch, J. M. Bower and C. Mead: Modelling small oscillating biological networks in analog VLSI, Advances in Neural Information Processing Systems 1 D. S. Touretzky, Ed., Los Altos, CA: Morgan Kaufmann, pp. 384-393, 1989.
- [7] A. F. Murray, A. Hamilton and L. Tarassenko: Programmable analog pulse-firing neural networks, Advances in Neural Information Processing Systems 1. D. S. Touretzky, Ed., Los Altos, CA: Morgan Kaufmann, pp. 671-677, 1989.
- [8] J. L. Meador and C. S. Cole: A low-power CMOS circuit which emulates temporal electrical properties of neurons, Advances in Neural Information Processing Systems 1. D. S. Touretzky, Ed., Los Altos, CA: Morgan Kaufmann, pp. 678-685, 1989.

- [9] T. Asai, Y. Kanazawa and Y. Amemiya: A subthreshold MOS neuron circuit based on the Volterra system, *IEEE Trans. Neural Networks*. Vol. 14, No. 5, pp. 1308-1312, 2003.
- [10] H. R. Wilson and J. D. Cowan: Excitatory and inhibitory interactions in localized populations of model neurons, *Biophys. J*, Vol. 12, pp. 1-24, 1972.
- [11] T. Hirose, T. Matsuoka, K. Taniguchi, T. Asai and Y. Amemiya: Ultralow-power current reference circuit with low-temperature dependence, *IEICE Transactions on Electronics*, Vol. E88-C, No. 6, pp. 1142-1147, 2005.
- [12] S. Liu, J. Kramer, G. Indiveri, T. Delbruck and R. Douglas: *Analog VLSI: Circuit and Principles*, The MIT press, 2002.



**Testuya Hirose** received the B.S., M.S. and Ph.D. degrees from Osaka University, Osaka, Japan, in 2000, 2002, and 2005, respectively. Currently, he is a Research Associate in the Department of Electrical Engineering, Hokkaido University, Sapporo, Japan. His current research interests are in low-power analog/digital CMOS circuits and subthreshold MOSFET functional circuits for intelligent sensors. Dr. Hirose is a member of the Institute of Electronics, Information and Communication Engineers of Japan, and the IEEE.



**Gessyca Maria Tovar** was born in Venezuela in 1981. She received the B.S. degree in Electronic Engineering from Jose Antonio Paez University, Venezuela, in 2004. Currently she is working towards her Master degree in the Department of Electrical Engineering at Hokkaido University, Japan. Her research interests include neuromorphic computation and hardware implementation.



**Tetsuya Asai** is an Associate Professor in the Graduate School of Information Science and Technology, Hokkaido University, Sapporo, Japan. His research interests concentrate around developing nature-inspired integrated circuits and their computational applications. Current topics that he is involved with include; intelligent image sensors that incorporate biological visual systems or cellular automata in the chip, neuro

chips that implement neural elements (neurons, synapses, etc.) and neuromorphic networks, and reaction-diffusion chips that imitate vital chemical systems.



**Yoshihito Amemiya** received the B.E., M.E., and Ph.D. degrees from the Tokyo Institute of Technology, Tokyo, Japan, in 1970, 1972, and 1975. He joined NTT Musashino Laboratories in 1975, where he worked on the development of silicon process technologies for high-speed logic LSIs. From 1983 to 1993, he was with NTT Atsugi Laboratories and developed bipolar and CMOS circuits for Boolean logic LSIs, neural network LSIs, and cellular automaton LSIs. Since 1993, he has been a Professor with the Department of Electrical Engineering, Hokkaido University, Sapporo. His research interests are in the fields of silicon LSI circuits, signal processing devices based on nonlinear analog computation, logic systems consisting of single-electron circuits, and information-processing devices making use of quantum nanostructures.

(Received May 14, 2007; revised August 31, 2007)