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Noise-Induced Phase Synchronization among Simple Digital Counters

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Abstract

We demonstrate noise-induced phase synchronization among simple digital counters, aiming at its practical application to phase synchronization among isolated digital systems (driven by precise clock sources) accepting common noisy pulse sequences. We employ a simple digital up-counter where i) relaxation oscillations in nonlinear analog oscillators are emulated by linear counting and carry overflow in a low-bit digital counter and ii) the counter value, which is equivalent to the phase of the digitally emulated oscillator, is increased by the precise base clocks, as well as by external noisy pulses, and the autonomous increase of the value (by the base clock) is inhibited by the noisy pulses, depending on the phase of the counter at which the pulse is given. Through extensive Verilog simulations, we demonstrate that the proposed digital counters can be synchronized by applying a common noise sequence, even if initial values of both the counters and phases of the counter's base clocks have different values.

1. Introduction

Synchronization among nonlinear oscillators can be observed everywhere in the world, and has attracted much attention from many scientific and engineering fields. Noise-induced synchronization among nonlinear oscillators has been one of the topics of great relevance and long-standing controversy (*e.g.*, [1, 2, 3, 4, 5, 6]), where individual nonlinear oscillators can be synchronized by applying common random noise to the oscillators. This implies that when one considers embedding multiple oscillators on hardware, phases of the oscillators could be synchronized by applying common random noises, and the oscillators distributed on the hardware (*e.g.*, large-scale integrated circuits) can be utilized as synchronized "clock sources".

Inspired by the results and implications above, we previously proposed hardware oscillator circuits based on the Wilson-Cowan oscillator model [7], which is suitable for hardware implementation, and showed that synchronization properties of the Wilson-Cowan model were qualitatively equivalent to those of the conventional model [8]. Through circuit simulations, we demonstrated noise-induced synchronization among the hardware oscillators, and evaluated the synchrony dependence on device mismatch between two oscillator circuits. The results showed that i) the oscillators exhibited phase-locked oscillation and ii) the circuit had low tolerance to device mismatch, although a small phase difference exists [8]. Also, we have "experimentally" tested noise-induced synchronization among electrical oscillator circuits receiving common random impulses [9], where two analog oscillator circuits having small difference in their intrinsic frequencies had the same peak frequency in the power spectrum when they received the same random impulses.

We are trying to find practical applications for noise-induced synchronization. Possible candidates are i) distributed multiple clocks on a semiconductor chip where the phase can be synchronized by applying common noise to the power supply, and ii) phase-lock loops among different circuit blocks, chips, or systems. Among them, phase locking between isolated digital systems is a very important task to ensure their synchronous operation; *e.g.*, communication between two digital systems where a "sender" and a "receiver" are operating with the same clock frequency, but their initial phases are different, which may result in mis- or wrong capture of data at the receiver. The present solution to this problem is to employ a "phase-locked loop", which accepts the clock of the sender, compensates the difference between the sender's clock phase and the receiver's phase, and then acts as the clock source of the receiver. Noise-induced phase synchronization may be utilized in this phase-lock operation; *i.e.*, a "sender" and a "receiver" operating with the same clock frequency, but having different initial phases, can be synchronized by applying common noise. To demonstrate this, we designed a simple digital counter that emulates nonlinear oscillation and can accept temporal noise.

2. The Circuit

To observe noise-induced phase synchronization among digital oscillators, each oscillator must implement the follow-

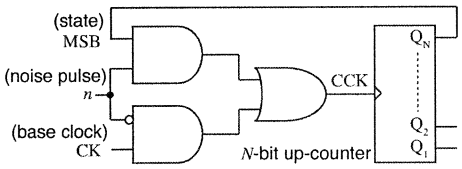

Figure 1: Simple digital counter for observing noise-induced phase synchronization

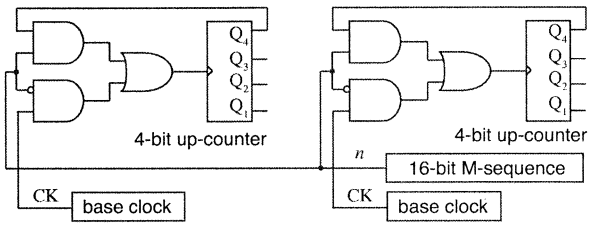

Figure 2: Simulation setup: two 4-bit digital counters accepting a common random sequence

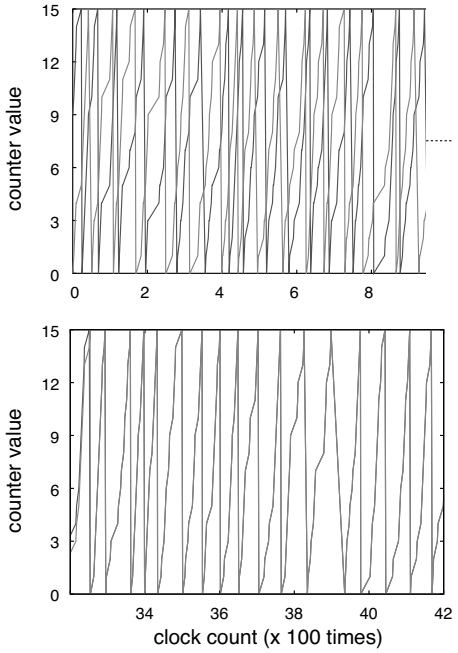

Figure 3: Simulation results of two 4-bit digital counters accepting a common base clock and common noise sequence

ing features: i) the oscillator's state is represented by two logical values depending on the phase ϕ (state "0" for $0 < \phi < \pi$ and state "1" for $\pi < \phi < 2\pi$), ii) the oscillator accepts noise as a pulse at time t_i, where i represents the index number of the given single-shot pulse, iii) when $t = t_i$, the phase must be advanced if the oscillator's state is "0", whereas the phase must be delayed if the oscillator's state is "1". We employ a conventional digital counter where the most significant bit (MSB) of the counter represents the oscillator's two states. In state "0", whenever a counter accepts noise pulses, the counter "up-counts" the noise pulse (the phase is advanced), whereas in state "1", the counter's clock input is suppressed by the noise pulse (the phase is delayed). We represent these requirements in terms of the counter's input clock (CCK) as

$$\mathrm{CCK} = \overline{\mathrm{MSB}} \cdot n + \mathrm{CK} \cdot \overline{n} \qquad (1)$$

where MSB represents the most significant bit of the counter, n the noise pulse, and CK the base clock. When n = "0", the counter up-counts CK only, regardless of the value of MSB. When n = "1" and MSB = "0", the counter up-counts the noise pulse only, whereas CCK = "0" when n = "1" and MSB = "1", which results in blocking the up-counting. Figure 1 shows circuit diagrams of the proposed digital counter.

It should be noted that when $\mathrm{CK} = n =$ "1", the circuit shown in Figure 1 is not able to satisfy all the requirements for noise-induced phase synchronization, which may result in requiring much time for complete phase synchronization. In state "0" (for $0 < \phi < \pi$; $\Delta\phi$ should be positive), $\Delta\phi$ becomes zero (CCK is kept zero) when $\mathrm{CK} = n =$ "1". This might happen at the rising edge of CK after the rise of n. Similarly, in state "1" (for $\pi < \phi < 2\pi$; $\Delta\phi$ should be negative), $\Delta\phi$ becomes positive (CCK raises), and this might happen at the rise of CCK before the falling edge of n when CK = "0". Therefore, one must decrease the probability such that $\mathrm{CK} = n =$ "1" simultaneously, and this may easily be attained by decreasing the duty ratios of CK and n.

3. Simulation and Experimental Results

Figure 2 illustrates our simulation setup. First, we employed two 4-bit circuits, and simulated them by a Verilog simulator (Icarus Verilog). Figure 3 shows simulation results (time evolution) of counter values of the circuits. They accepted a common base clock and a common noise sequence generated by a 16-bit M-sequence circuit (Galois LFSR). The initial phase difference was set at π. After around 200 ($= 3,200$ clock counts / 2^4) iterations, the circuits were synchronized. In the simulation, duty ratios of CK and n were set at 50%. When the ratio was decreased, the number of iterations was significantly decreased, because the probability of $\mathrm{CK} = n =$ "1" was decreased, as explained in the last paragraph of Section 2.

The synchronization may be disturbed when the phases of the base clocks of the counters are different, but one may expect that it may be compensated if one increases the number of counter bits, because the phase difference is roughly given by $1/2^N$, where N represents the number of counter bits. Figure 4 shows numerical simulation results exhibiting correlation values between the counter values versus the number of counter bits (N), where the phase difference between the base clock was set at π (maximum). From this, we

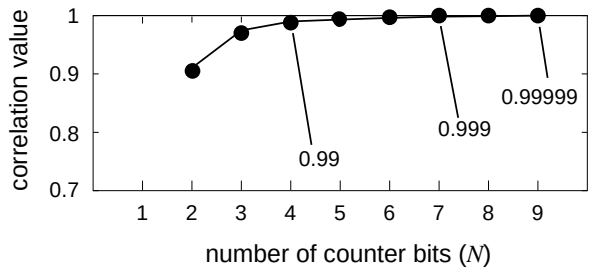

Figure 4: Correlation values between two identical digital counters having phase difference (π) between their base clocks versus the number of counter bits

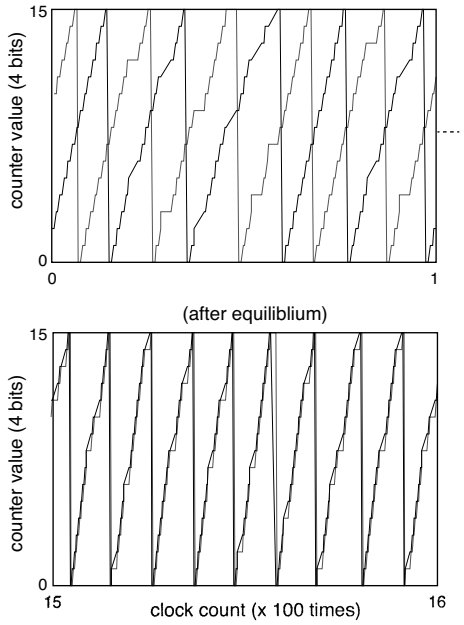

Figure 5: Time evolution of counter values of two 4-bit digital counters having phase difference (π) between their base clocks

conclude that isolated digital counters having different base clock phases can be synchronized if we employ digital counters with a large number of bits. Figure 5 shows the time evolution of counter values of two 4-bit digital counters having phase difference (π) between their base clocks. The initial phase difference of counter values was set at π. After many iterations (around $1,500/2^4 \approx 94$ iterations in this example), it reached an equilibrium state where the two counter values had only a small difference (Figure 5 bottom). The error was caused by the phase difference in the base clock (the maximum time difference is $T/2$, where T represents the period of the base clock). Since the time difference is divided by 2^N by the counter, by increasing N, the error can become negligible.

When the number of counter bits is increased in a fixed

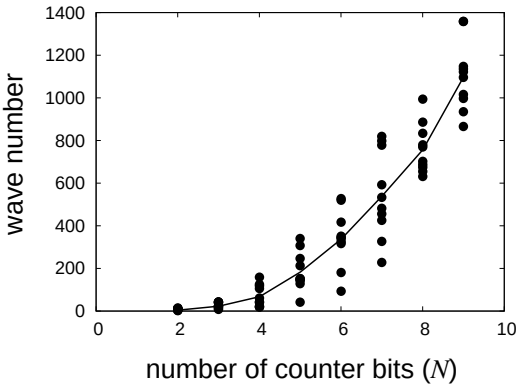

Figure 6: Estimated number of base-clock pulses (wave number) until equilibrium versus number of counter bits (N)

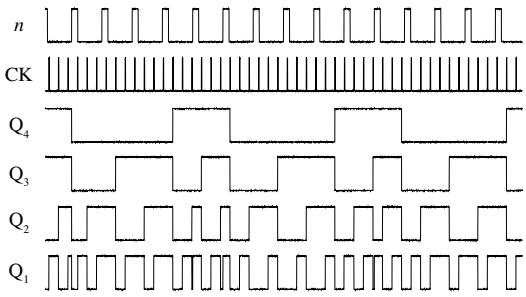

Figure 7: Experimental results of fabricated 4-bit counter with phase modulation circuit shown in Figure 1

base-clock environment, the time required for phase synchronization (equilibrium time) would be increased. The equilibrium time would be an important factor in many practical applications, therefore, we roughly estimated the equilibrium time versus the number of counter bits. Figure 6 shows estimates of the equilibrium time in terms of the number of clock pulses, which we call "wave number", versus the number of counter bits (N). For a fixed number of bits, we conducted 10 simulations with different random seeds of the M-sequence circuit, and calculated the wave numbers (black circles in the figure) until it reached the equilibrium. The average values are also plotted in the figure (solid line). As expected, the wave numbers increased exponentially as N increased. For $N = 9$, the average wave number was about 10^3, which indicated that $10^3 f^{-1}$ seconds is required, where f represents the base clock frequency, until equilibrium (phase synchronization with the correlation value of 0.99999, as shown in Figure 4). This means, if f were set at 1 MHz, the digital counters would be synchronized within 1 ms, even if the phase difference between their base clocks was maximum (π rad = 0.5 μs).

Figure 7 shows experimental results for the fabricated 4-bit counter with the phase modulation circuit shown in Figure

Table 1: Performance summary of noise-induced synchronization among real-world circuits

	primary mismatch*1	mismatch degree	sync. stability*3	frequency band	frequency
CMOS osc. [8, 9]	MOS FET	large	unstable	middle–high	variable by bias
LC-based osc.	L and C	small	unstable	middle–very high	fixed
crystal osc.	crystal fragments	very small	stable	middle–very high	fixed
proposed	phase diff. of base clock*2	large	stable for large N	low–middle*4	variable by N

1. For simplicity, noise pulses (n) were replaced by periodic pulses in this experiment. We could observe the phase modulation by n when the counter values (Q_1 to Q_4) did not exhibit periodic oscillations. We have already confirmed real-time phase synchronization among two counter circuits at very low frequency, and are now undertaking the optimization of the noise parameters (pulse width and average interspike intervals) in terms of base-clock frequency.

Table 1 summarizes performance of noise-induced phase synchronization among analog complementary metal oxide semiconductor (CMOS), LC-based, and crystal oscillators, as compared with the proposed circuit. Since base clocks of the proposed circuits are generated by crystal oscillators that plausibly have very small frequency differences, the circuit's primary (sole) mismatch component*1 (see labelled items in Table 1) that may disturb the phase synchronization is phase differences among the base clocks*2. Among the proposed circuits, the stability of phase synchronization under the assumed degree of mismatch*3 can be improved by increasing the number of counter bits (N), as shown in Figure 4; however, as N increases, the nominal oscillation frequency of the counter is decreased because the nominal frequency is given by the base clock's frequency divided by 2^N. Therefore, the use would be limited to low to middle frequency applications*4.

4. Summary

We demonstrated noise-induced phase synchronization among simple digital counters. We designed a simple digital up-counter having phase-modulation circuitry in which nonlinear oscillations were emulated by linear counting and carry overflow in a low-bit digital counter. Through extensive Verilog simulations, we demonstrated that the proposed digital counters were able to be synchronized by applying common noise sequences, even if initial values of the two counters and the counter's base clocks had different values.

Acknowledgments

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References

[1] C. Zhou and J. Kurths: Noise-induced phase synchronization and synchronization transitions in chaotic oscillators, Phys. Rev. Lett., Vol. 88, No. 23, pp. 230602(1-4), 2002.

[2] C. Zhou, J. Kurths, I.Z. Kiss and L. Hudson: Noise-enhanced phase synchronization of chaotic oscillators, Phys. Rev. Lett., Vol. 89, No. 1, pp. 014101(1-4), 2002.

[3] J.A. Freund, S. Barbay, S. Lepri, A. Zavatta and G. Giacomelli: Noise-induced phase synchronization: Theoretical and experimental results, Fluctuation and Noise Lett., Vol. 3, No. 2, pp. L195-L204, 2003.

[4] H. Nakao, K. Arai and K. Nagai: Synchrony of limit-cycle oscillators induced by random external impulses, Phys. Rev. E, Vol. 72, No. 2, pp. 026220(1-13), 2005.

[5] H. Nakao, K. Arai and Y. Kawamura: Noise-induced synchronization and clustering in ensembles of uncoupled limit-cycle oscillators, Phys. Rev. Lett., Vol. 98, No. 18, pp. 184101(1-4), 2007.

[6] K. Arai and H. Nakao: Phase coherence in an ensemble of uncoupled limit-cycle oscillators receiving common Poisson impulses, Phys. Rev. E, Vol. 77, No. 3, pp. 036218(1-17), 2007.

[7] H.R. Wilson and J.D. Cowan: Excitatory and inhibitory interactions in localized populations of model neurons, Biophys. J., Vol. 12, No. 1, pp. 1–24, 1972.

[8] A. Utagawa, T. Asai, T. Hirose and Y. Amemiya: Noise-induced synchronization among sub-RF CMOS analog oscillators for skew-free clock distribution, IEICE Trans. on Fundamentals, Vol. E91-A, No. 9, pp. 2475–2481, 2008.

[9] A. Utagawa, T. Asai and Y. Amemiya: Noise-induced phase synchronization among analog MOS oscillator circuits, Fluctuation and Noise Lett., Vol. 11, No. 2, in press.