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Paper

A neuromorphic MOS circuit imitating jamming avoidance response of *Eigenmannia*

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Abstract: In this paper, we implement a model of an electric fish, *Eigenmannia*, that detects frequency differences between the individuals, on analog CMOS circuits. The circuit's fundamental function is equivalent to a conventional "phase frequency comparator". The circuit consists of five elemental cell units that implement neural networks of the electric fish. Using a simulation program of integrated circuit emphasis (SPICE), we demonstrate that the proposed circuit can detect the frequency difference.

Key Words: Eigenmannia, electric fish, jamming avoidance response, phase frequency comparator, analog circuit

1. Introduction

Eigenmannia (Fig. 1) is an electric fish that generates electric fields through their electric organ, which is referred as electric organ discharge (EOD), to recognize the surrounding environment (Fig. 2). Electroreceptors on their skin surface detect the local electromagnetic field, to recognize "obstacles" around the fish. Because local obstacles interfere with the electromagnetic field, by comparing the interfered field (phases and amplitudes of detected voltages) with less-interfered ones, *Eigenmannia* can recognize the surrounding environment, *e.g.*, positions and shapes of the obstacles, which results in their intelligent electrolocation ability.

When two individuals (fishes) each of which emits the same EOD frequencies are nearly located,

Fig. 1. *Eigenmannia* (electric fish).

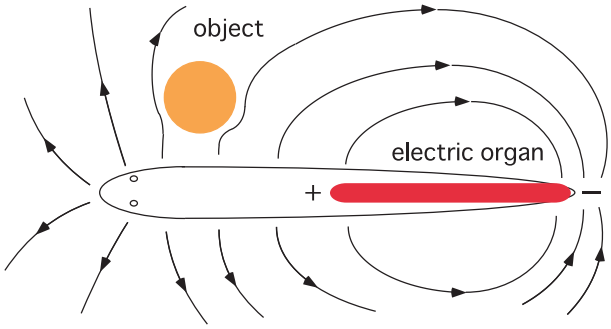

Fig. 2. Electric fields generated by *Eigenmannia* for electrolocation.

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they shift their EOD frequencies away from each other, because the electrolocation ability is vulnerable to interference with the fish's own EOD signals. This behavior is called *jamming-avoidance response* (JAR). To do this, *Eigenmannia* discriminates a sign of the frequency difference between their own EOD and the neighbor's one [1].

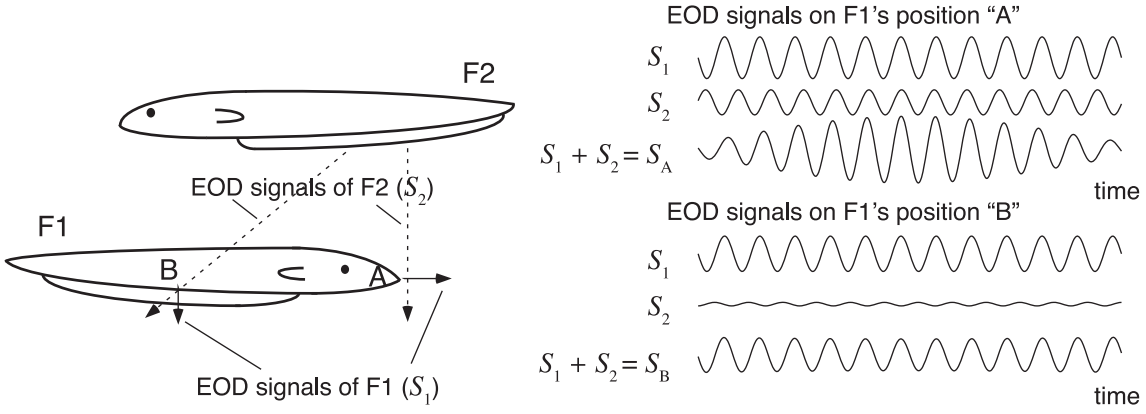
Neural computing systems of creatures sometimes exhibit significant advantages against present Neumann-based information processing systems (*e.g.*, [2–5]). To explore advantages against present computing systems, an analog VLSI model of JAR has been proposed in [6]. The circuit system precisely implemented the JAR model proposed in [1], however, it consisted of biologically-improbable circuit elements such as operational amplifiers, digital inverters, large capacitors, and so on. In this paper we thus try to employ biologically-plausible circuit elements, *i.e.*, current-mode MOS circuits utilizing time delays on the current paths, to implement a part of a neural network model of *Eigenmannia*.

The system we implement here acts as a phase frequency comparator, however, we do neither aim at the implementation of the primary functions, nor the replacement of existing (commercial) phase frequency comparators with it. Our final goal is to develop intelligent hardware system based on our present knowledge on neural systems of *Eigenmannia*, based on a bottom-up approach. Form a part of the whole development, we need to design a biologically-plausible electrical circuit implementing a model of JAR in *Eigenmannia*. We have already designed two types of fundamental cells of *Eigenmannia* which convert environmental inputs into spike density and encode the phase information into spike timing [7]. In this paper we implement additional three types of cells of *Eigenmannia* on analog CMOS circuits, and construct a network circuit of these five types of cells. We demonstrate that the network circuit can discriminate the frequency difference between two EOD signals.

2. Model of jamming avoidance response in *Eigenmannia*

The primary purpose of jamming-avoidance response (JAR) in *Eigenmannia* is to avoid generating the same electric-organ discharge (EOD) signals among them by increasing (or decreasing) their EOD frequencies. For example, when two fishes, which we denote by F1 and F2, are nearly located and they have almost the same EOD frequencies, which we denote f_1 and f_2 ($f_1 \approx f_2$), they begin to generate different EOD signals. To do this, F1 calculates the frequency difference ($\Delta f_{21} \equiv f_2 - f_1$), whereas F2 does $\Delta f_{12} \equiv f_1 - f_2$. Then, to avoid having the same EOD frequencies, F1 decreases (or increases) f_1 when $\Delta f_{21} > 0$ (or $\Delta f_{21} < 0$). Similarly, F2 decreases (or increases) f_2 when $\Delta f_{12} > 0$ (or $\Delta f_{12} < 0$).

Now let us see how F1 and F2 compare their EOD frequencies. Again, assume that F1 and F2 are nearly located in parallel, as shown in Fig. 3. They accept interfered EOD signals and less-interfered (self-generated) EOD signals via two electroreceptors located at different body positions, *e.g.*, positions A and B shown in Fig. 3(a). In the figure, solid arrows represent F1's EOD signals, while dashed ones represent EOD signals generated by F2. Because F1's EOD signal passes along



(a) Jamming of EODs. (b) EOD and interfered signals on F1.

Fig. 3. Interference of EOD signals among two *Eigenmannia*.

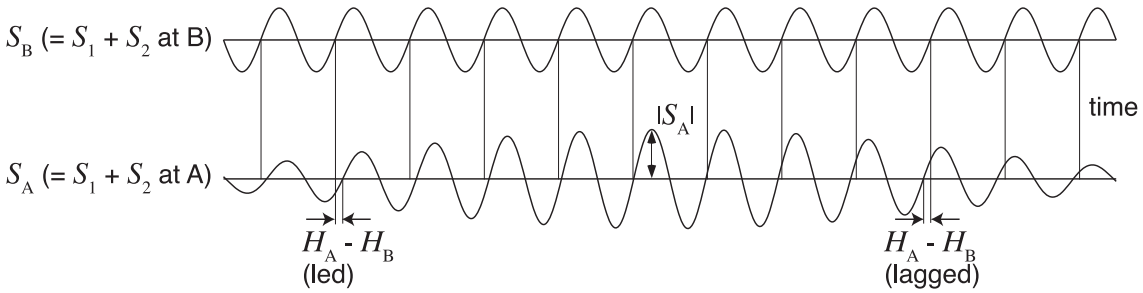


Fig. 4. Received (interfered) signals of F1 at positions A and B.

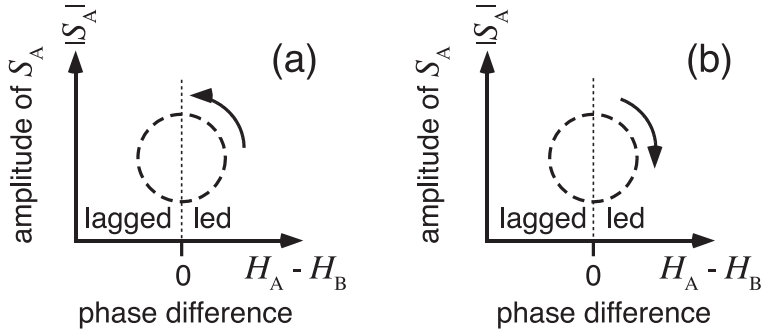


Fig. 5. Rotating direction in $|S_A|$ versus $H_A - H_B$ plane represents the phase difference between S_A and S_B.

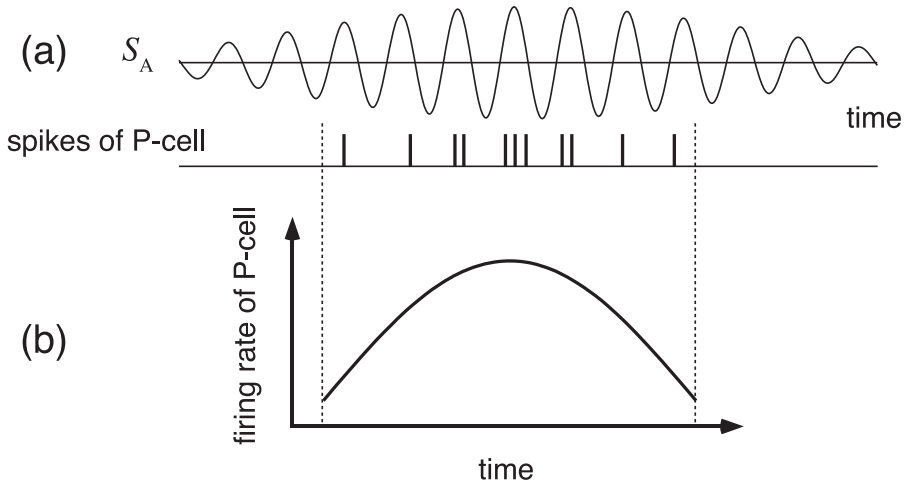


Fig. 6. Functions of P-cell.

F1's skin surface, F1's EOD signals detected by an electroreceptor at position A are almost the same as signals detected by an electroreceptor at position B (≈ F1's EOD signal). On the other hand, EOD signals generated by F2 pass through F1's trunk perpendicularly. Therefore, F2's EOD signals detected by the electroreceptor at position A would significantly be different from signals detected at position B.

F1 accepts synthesized EOD signals of its own EODs (S_1) and F2's ones (S_2) on electroreceptors at positions A and B. We denote the synthesized EOD signals at positions A and B as S_A and S_B, respectively. Figure 3(b) shows examples of the EOD signals (S_A and S_B) detected by F1 at positions A and B as well as S_1 and S_2. In this figure, we assume that S_1's EOD frequency is lower than that of S_2 ($\Delta f_{21} > 0$). In this case, F1 tries to select largely interfered EODs among S_A and S_B ($= S_A$ in this example), and then extracts the amplitude information [1].

Figure 4 shows waveforms of received (interfered) signals on F1 at positions A and B (S_A and S_B). In this example, amplitudes of S_A ($\equiv |S_A|$) is modulated significantly as compared with that of S_B. By

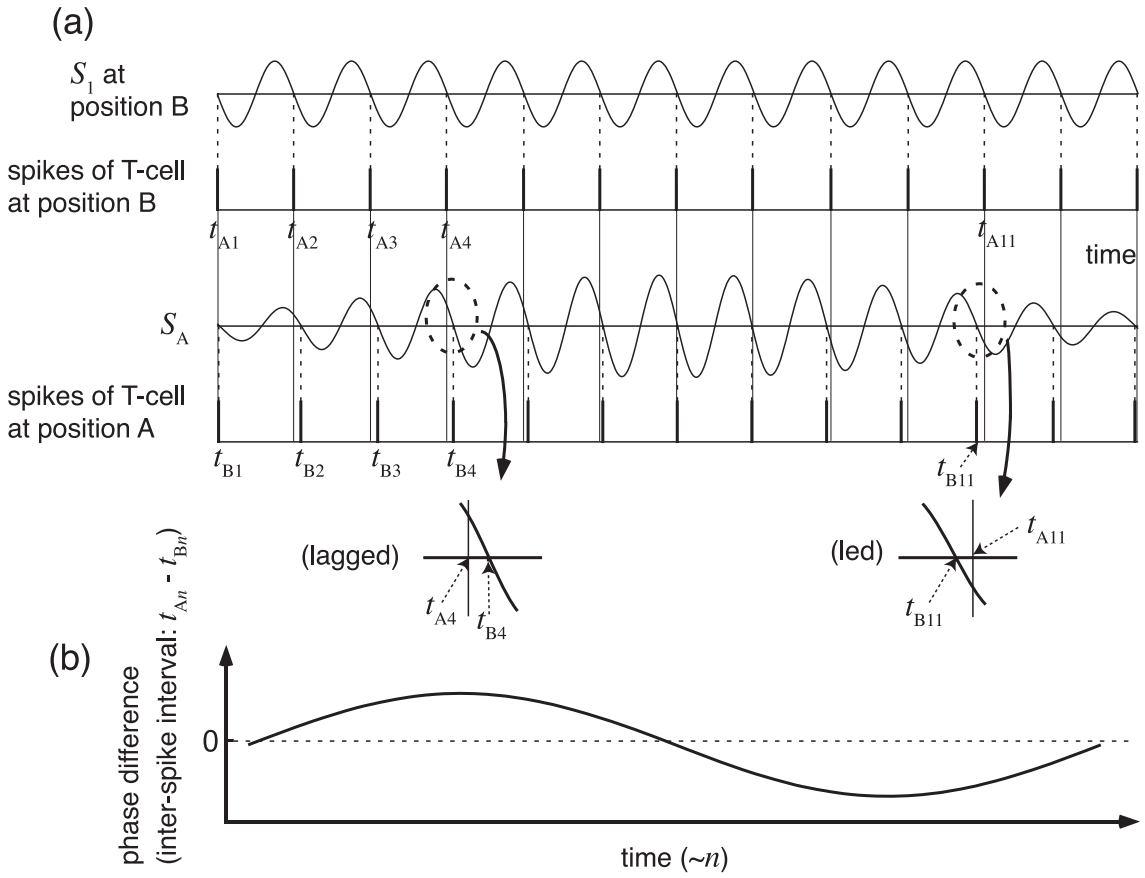


Fig. 7. Functions of T-cells.

comparing phases of S_{A} and S_{B}, which we denote by H_{A} and H_{B}, respectively, *Eigenmannia* detects whether the phase difference $(H_{\mathrm{A}} - H_{\mathrm{B}})$ is positive (phase of S_{A} is led) or negative (lagged) [1]. Figure 5 illustrates a concept of how *Eigenmannia* detects the phase lag (phase difference). The figure plots the amplitude and the phase difference on a $|S_{\mathrm{A}}|$ versus $H_{\mathrm{A}} - H_{\mathrm{B}}$ plane when $\Delta f_{21} > 0$ [Fig. 5(a)] and $\Delta f_{21} < 0$ [Fig. 5(b)]. When $\Delta f_{21} > 0$ (or $\Delta f_{21} < 0$), the plot point rotates counterclockwise (or clockwise) as time increases. By discriminating direction of the rotation on the $|S_{\mathrm{A}}|$ versus $H_{\mathrm{A}} - H_{\mathrm{B}}$ plane, *Eigenmannia* detects the phase lag [1].

How does *Eigenmannia* encode EOD signals on the $|S_{\mathrm{A}}|$ versus $H_{\mathrm{A}} - H_{\mathrm{B}}$ plane? The first step is to encode detected EOD signals into spike density. A P-cell, one kind of electroreceptors on *Eigenmannia*'s skin, encodes the amplitudes in spike densities, as shown in Fig. 6(a). Consequently, the mean-firing rate of a P-cell represents the amplitudes of the synthesized EODs (S_{A}). The second step is to detect phase differences between the electroreceptors $(H_{\mathrm{A}} - H_{\mathrm{B}})$. A T-cell, the other kind of electroreceptors on *Eigenmannia*'s skin, encodes phase information of the synthesized EOD signals. As shown in Fig. 7(a), a T-cell fires only when the synthesized EODs have a certain phase $(= \pi(2n+1)$ where n is the integer value and is proportional to time). By calculating inter-spike intervals between the firing of the T-cells on positions A and B $[t_{\mathrm{A}n} - t_{\mathrm{B}n}]$, F1 extracts the phase difference (lagged or led), as shown in Fig. 7(b).

Figures 6(b) and 7(b) represented time courses of the normalized maximal firing rates of F1's P-cell at position A ($|S_{\mathrm{A}}|$) and normalized inter-spike intervals of F1's T-cells at positions A and B, respectively, within a given period of the synthesized EOD signals. Again, when amplitude $|S_{\mathrm{A}}|$ and the phase difference are plotted in a $|S_{\mathrm{A}}|$ versus $t_{\mathrm{A}n} - t_{\mathrm{B}n}$ plane, a circular orbit appears, as shown in Fig. 5 where $H_{\mathrm{A}} - H_{\mathrm{B}}$ can be regarded as inter-spike intervals $t_{\mathrm{A}n} - t_{\mathrm{B}n}$. Directions of the rotation reflect the sign of Δf_{21}; clockwise for negative and counterclockwise for positive Δf_{21}. By detecting the direction, *Eigenmannia* makes a decision to increase or decrease their own EOD frequency [1].

Now let us see how *Eigenmannia* detects direction of rotation on a $|S_{\mathrm{A}}|$ versus $t_{\mathrm{A}n} - t_{\mathrm{B}n}$ plane

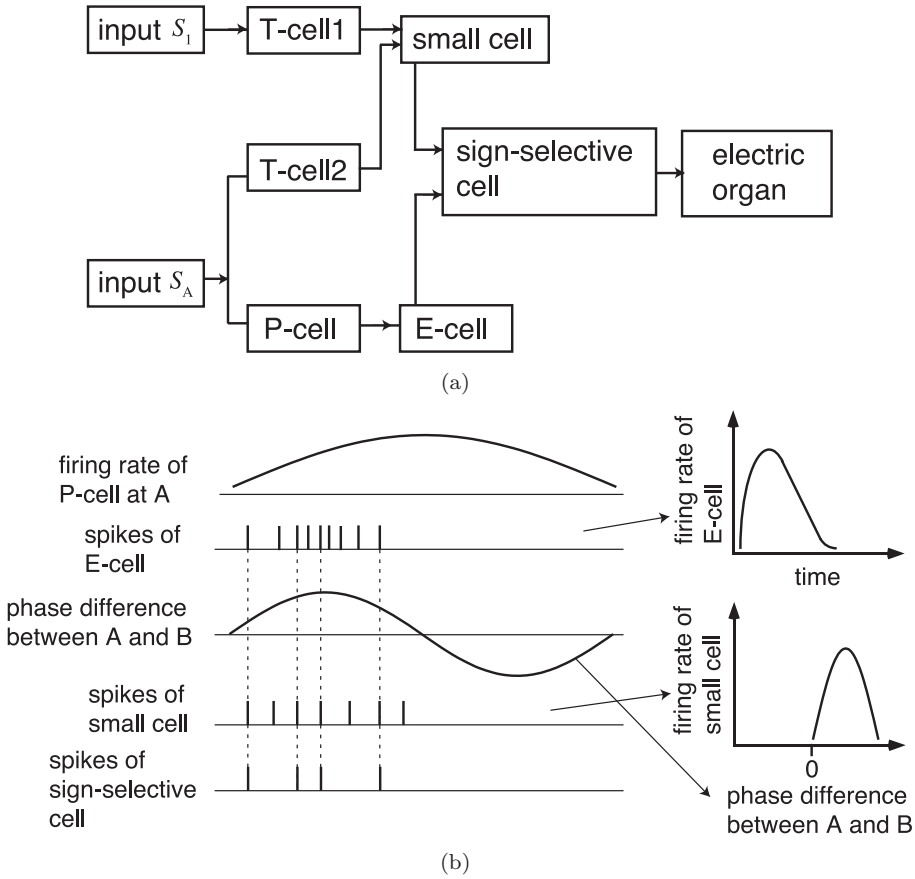


Fig. 8. Model of jamming-avoidance response (JAR) in *Eigenmannia*.

as illustrated in Fig. 5. Figure 8(a) shows the overall model which explains F1's JAR operation. Functions of E- and T-cells have been explained above. The other cells (E-, small and sign-selective cells) are employed for detecting the direction of the rotation—the sign of Δf_{21}. In this network, spikes generated by P-cells are forwarded to an E-cell. As shown in Fig. 8(b), the E-cell generates spikes only when firing rates of P-cells are increasing. On the other hand, output spikes of T-cells are forwarded to a small cell. The small cell generates spikes only when phase differences between detected EODs at positions A and B are positive ($t_{An} - t_{Bn} > 0$). A sign-selective cell generates spikes only when the E-cell and the small cell fire simultaneously. *Eigenmannia* detects the direction of the rotation in Fig. 5 by the output of the sign-selective cell. When the sign-selective cell generates output spikes, the plot point on Fig. 5 rotates counterclockwise as time increases, whereas if the cell does not generate spikes, the direction is clockwise [1]. Finally, output spikes of the sign-selective cell are forwarded to an electric organ to generate EOD signals.

3. Circuit implementation of model of jamming avoidance response

Firstly, we introduce a P-cell circuit which converts analog input currents into spike density [7]. The P-cell circuit [Fig. 9(a)] was designed based on the Volterra system [8]. Here let us assume that V_m and I_m of the P-cell circuit are zero at the initial state. The P-cell accepts I_{in}, and the current is mirrored to node V_m via current mirror M_{P1}-M_{P2}. The current is integrated by the gate capacitance of M_{P3}, which results in nonzero V_m as long as $I_{ref} < I_{in}$. The nonzero V_m induces drain currents of M_{P3}, and the current is mirrored to I_m via current mirrors M_{P4}-M_{P5} and M_{P6}-M_{P7}, which leads to the generation of nonzero I_m. Therefore, V_m starts decreasing to zero because of the nonzero I_m, which results in the decrease of I_m. This operation is repeated as long as nonzero I_{in} is given. We regard the increase and decrease of I_m as output spikes because the number of the output spike is roughly proportional to I_{in} within a certain range of I_{in}. The output spikes are read out by M_{P8} as I_{Pout}.

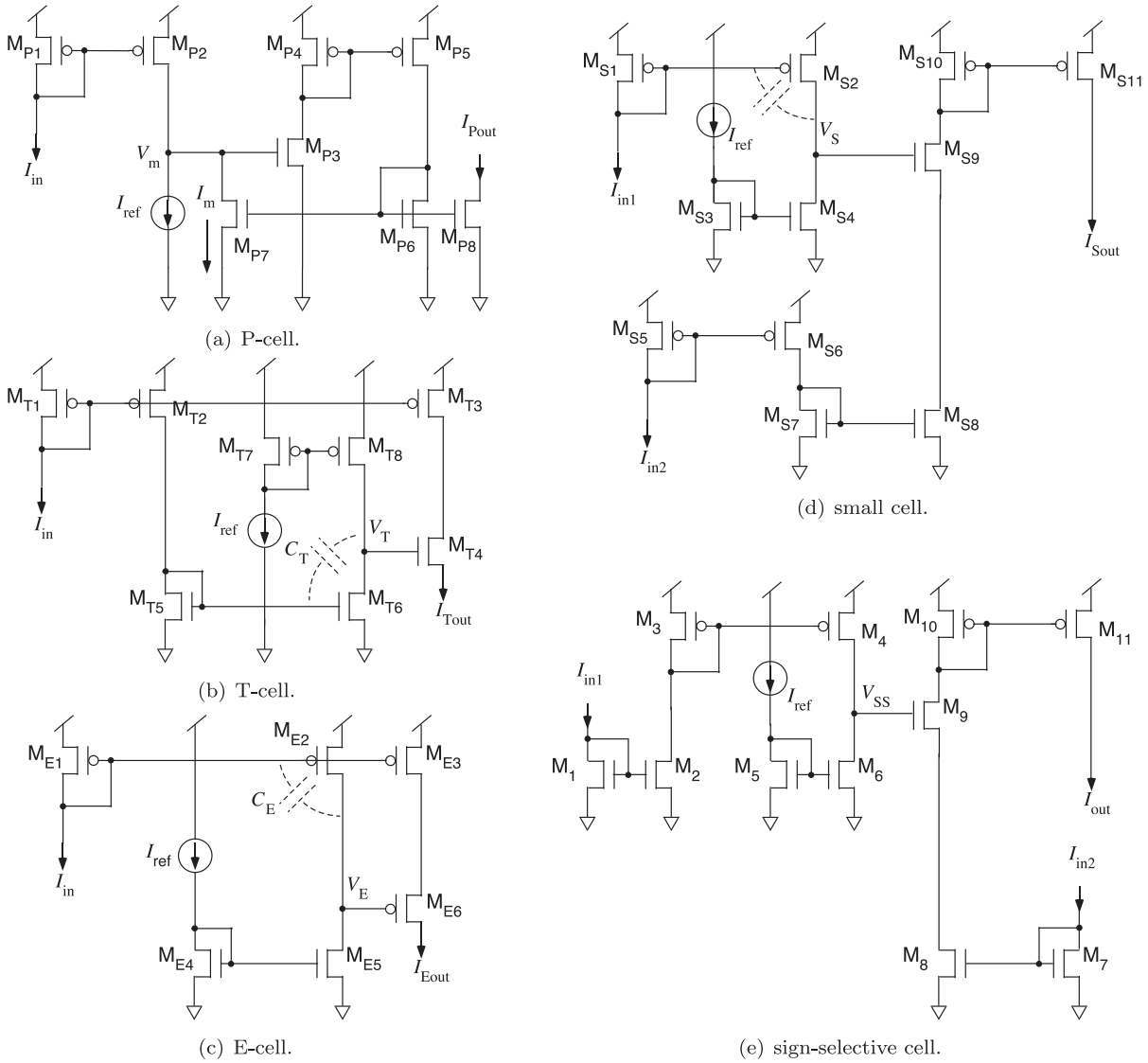


Fig. 9. Analog CMOS circuits for P-, T-, E-, small and sign-selective cells.

Figure 9(b) illustrates a T-cell circuit which we have already designed in [7]. When $I_{\rm in} = 0$, $V_{\rm T}$ is high at the equilibrium ($\rm M_{T4}$ is thus turned on) because $I_{\rm in}$ ($= 0$) is mirrored to node $V_{\rm T}$ via current mirrors $\rm M_{T1}$-$\rm M_{T2}$ and $\rm M_{T5}$-$\rm M_{T6}$, and current mirror $\rm M_{T7}$-$\rm M_{T8}$ is biased by nonzero $I_{\rm ref}$. Therefore, when the T-cell circuit accepts nonzero $I_{\rm in}$, the current ($I_{\rm in}$) is simply mirrored to the output terminal as $I_{\rm Tout}$. Because $\rm M_{T6}$ and $\rm M_{T8}$ can be regarded as a nMOS source-common amplifier where $\rm M_{T8}$ acts as the load, parasitic capacitance $C_{\rm T}$ of $\rm M_{T6}$ is amplified due to the Mirror effect. Once nonzero $I_{\rm in}$ was given, $V_{\rm T}$ is decreased because $C_{\rm T}$ is discharged by the current of $\rm M_{T6}$ ($=I_{\rm in}$). Therefore, $\rm M_{T4}$ is gradually turned off, and consequently, $I_{\rm in}$ is not mirrored to the output terminal ($I_{\rm Tout} \to 0$). This operation is equivalent to detecting rectified temporal deviations of $I_{\rm in}$, which result in detection of a certain phase for periodic $I_{\rm in}$.

We newly designed an E-cell circuit [Fig. 9(c)] which generates current spikes only at the onset of input spike trains ($I_{\rm in}$). Operations of this circuit is similar to the T-cell circuit. The input current ($I_{\rm in}$) is mirrored to node $V_{\rm E}$ via current mirror $\rm M_{E1}$-$\rm M_{E2}$, whereas $I_{\rm ref}$ is mirrored to node $V_{\rm E}$ via current mirror $\rm M_{E4}$-$\rm M_{E5}$. Therefore, when $I_{\rm in} = 0$, $V_{\rm E}$ is stable at zero ($\rm M_{E6}$ is thus turned on). Under this condition, when the circuit accepts nonzero $I_{\rm in}$ (> 0), $V_{\rm E}$ is increased, which turns $\rm M_{E6}$ off. It should be noticed that parasitic capacitance $C_{\rm E}$ of $\rm M_{E2}$ is amplified due to the Mirror effect of the pMOS source-common amplifier ($\rm M_{E2}$ and $\rm M_{E5}$ where $\rm M_{E5}$ acts as the load). Therefore $V_{\rm E}$ is increased with a (short) delay. Consequently, $\rm M_{E6}$ is turned on within an instant. During the instant

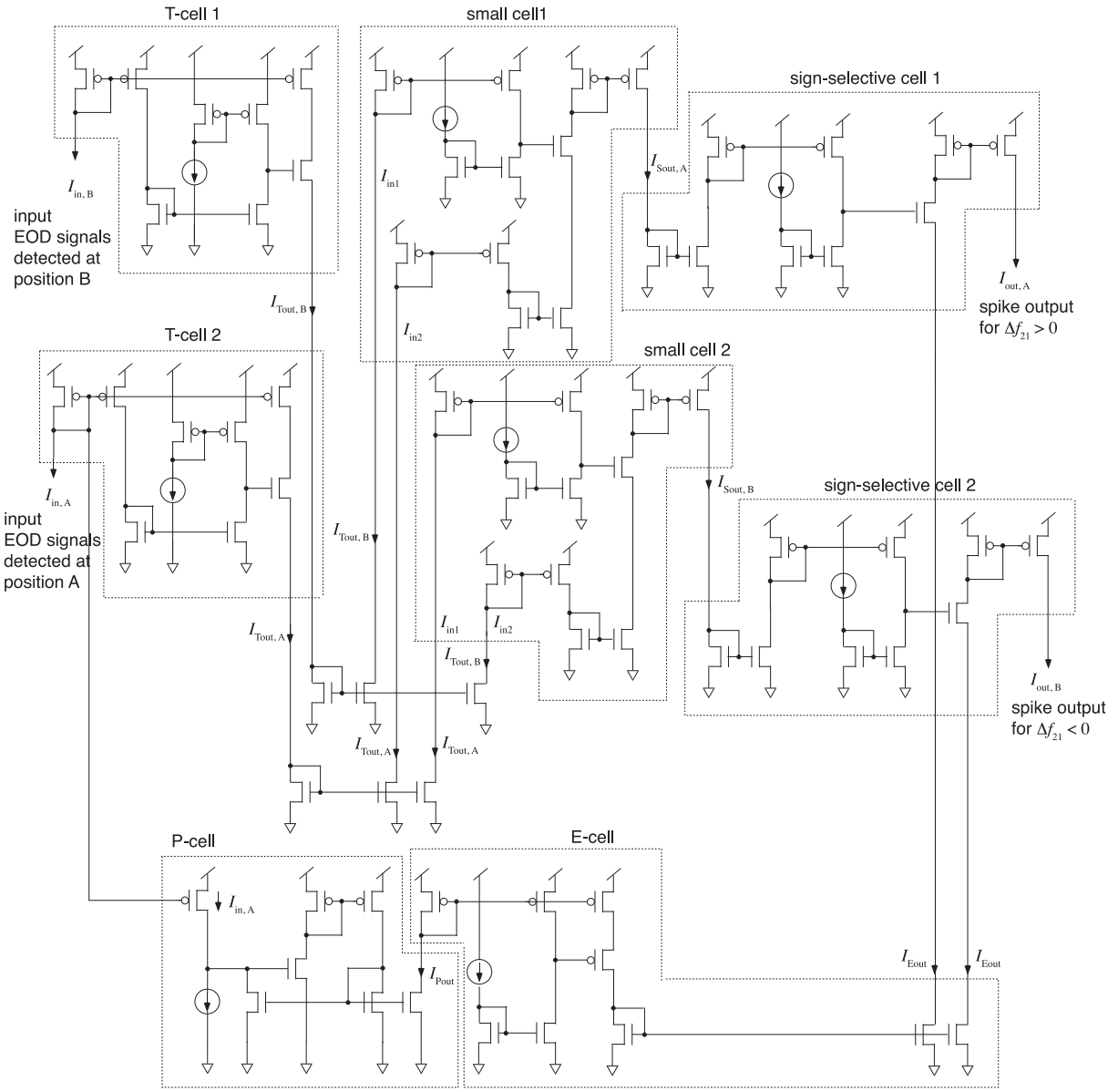


Fig. 10. Circuit network of model for jamming avoidance response of *Eigenmannia*.

term, the input current is mirrored to the output ($I_{\mathrm{E}out}$) via current mirror $\mathrm{M_{E1}}$-$\mathrm{M_{E3}}$. This operation allows the circuit to generate output spikes only at the onset of input spike trains.

We then designed a small-cell circuit [Fig. 9(d)] which generates current spikes only when a current spike is given to I_{in1} before arrival of a spike at I_{in2}, within a given time window. Input current I_{in1} is mirrored to node V_{S} via current mirror $\mathrm{M_{S1}}$-$\mathrm{M_{S2}}$. As in T- and E-cell circuits, when the small cell accepts nonzero I_{in1}, $\mathrm{M_{S9}}$ is turned on. On the other hand, when $I_{\mathrm{in1}} = 0$, V_{E} is stable at zero because nonzero I_{ref} is mirrored to node V_{S} via current mirror $\mathrm{M_{S3}}$-$\mathrm{M_{S4}}$, which turns $\mathrm{M_{S9}}$ off. When $\mathrm{M_{S9}}$ is turned on (nonzero I_{in2} is given just after the onset of I_{in1}), I_{in2} is mirrored to the output (I_{Sout}) via current mirrors $\mathrm{M_{S5}}$-$\mathrm{M_{S6}}$, $\mathrm{M_{S7}}$-$\mathrm{M_{S8}}$ and $\mathrm{M_{S10}}$-$\mathrm{M_{S11}}$.

Finally, we designed a sign-selective cell circuit [Fig. 9(e)]. The circuit is almost the same as the small-cell circuit, except for mirroring directions of the input and output currents. The circuit is biased so that the circuit can generate current spikes only when a current spike is given to I_{in1} before arrival of a spike at I_{in2}, within a short-time window, by controlling reference current I_{ref}. Large I_{ref} decrease the gain of the pMOS source-common amplifier ($\mathrm{M_4}$ and $\mathrm{M_6}$ where $\mathrm{M_6}$ acts as the load), which results in high fidelity of V_{SS} along with I_{in1}. Therefore, the circuit is able to detect one-way "coincidence" of the spikes I_{in1} and I_{in2}. In other word, the circuit detects coincidence under $t_1 < t_2$

where t_i represents the time at which $I_{\mathrm{in}i}$ receive an input spike, and does not detect coincidence when $t_1 > t_2$. Since the sign-selective cell circuit accepts outputs of E- and small cells, and the sign of $t_1 - t_2$ would randomly be fluctuated in practical environment, we did not implement a circuit that can detect coincidence under both $t_1 > t_2$ and $t_1 < t_2$.

Figure 10 shows the whole network circuit that consists of P-, T-, E-, small and sign-selective cell circuits. To detect both sign of Δf_{21}, we employed additional cells ("small cell 2" and "sign-selective cell 2" in the figure) where the "small cell 2" accepts opposite inputs from the two T-cell circuits against "small cell 1". Consequently, $\Delta f_{21} > 0$ and $\Delta f_{21} < 0$ are detected by spikes generated at $I_{\mathrm{out,A}}$ and $I_{\mathrm{out,B}}$ terminals, respectively, for the given EOD inputs ($I_{\mathrm{in,A}}$ and $I_{\mathrm{in,B}}$). The overall circuits used 86 MOSFETs (P-cell: 8, T-cell: 9×2, E-cell: 10, simple cell: 12×2, sign-selective cell:10×2 and additional nMOS current mirrors: 6) including bias current sources (they are replaced by saturated MOSFETs).

Since the proposed circuits above operate in the current mode, noise and fluctuations on I_{ref}s and mismatches of current mirrors certainly affect the circuit's quantitative behavior. Fortunately, the mismatches do not affect the qualitative behavior of the proposed circuits, as explained blow.

In the P-cell circuit [Fig. 9(a)], a current path from the input (I_{in}) to $\mathrm{M_{P7}}$ which shunts a node of V_{m} is longer than a current-charge path of a parasitic gate capacitance of $\mathrm{M_{P3}}$, the integrate-and-shunt (integrate-and-fire) operation is maintained as long as mirror rates of $\mathrm{M_{P4}}$-$\mathrm{M_{P5}}$, $\mathrm{M_{P6}}$-$\mathrm{M_{P7}}$ and $\mathrm{M_{P1}}$-$\mathrm{M_{P2}}$ are within typical matching characteristics of pair transistors in proper fabrication processes.

The T-cell circuit generates spikes only when positive I_{in} starts increasing. In the circuit [Fig. 9(b)], I_{in} is passed to I_{Tout} via $\mathrm{M_{T4}}$ which is initially turned on. After that, $\mathrm{M_{T4}}$ is turned off by delayed V_{T} generated by current paths of $\mathrm{M_{T1}}$-$\mathrm{M_{T2}}$-$\mathrm{M_{T5}}$-$\mathrm{M_{T6}}$ and $\mathrm{M_{T7}}$-$\mathrm{M_{T8}}$, which ensures the causality where $\mathrm{M_{T4}}$ is initially turned on and then is turned off, as long as we use pair transistors in standard fabrication processes. It should be noted that the parasitic capacitance (C_{T}) is amplified by the source-common amplifier ($\mathrm{M_{T6}}$-$\mathrm{M_{T8}}$). Therefore even if the capacitance is accidentally decreased by the mismatch, the delay is still larger than that of $\mathrm{M_{T1}}$-$\mathrm{M_{T3}}$, which ensures a fundamental operation of T-cell circuit where a spike is generated when positive I_{in} starts increasing.

Mismatches of mirror rates of current mirrors in P- and T-cell circuits as well as fluctuations of I_{ref} do affect quantities on Fig. 5, however, they do not affect direction of rotation on the phase plane because of the causalities of delay lines in the P- and T-cell circuits.

The E-cell circuit, which generates spike only when I_{in} is increasing, has the same delay-line structure as the T-cell circuit. Therefore small mismatches in the current mirrors do not affect the fundamental operation. Moreover, since small and sign-selective cell has the same delay-line structure as the T- and E-cell circuits, mismatches of current mirrors in the cell circuits affect quantities of the outputs, whereas they do not affect the qualitative behavior.

Of course, an unexpected outputs would be obtained when currents of MOSFETs generating I_{ref}s are accidentally buried in temporal noise and fluctuations. For real applications of the proposed circuit in phase frequency comparison, one needs to evaluate these points.

4. SPICE simulation results

In the following simulations, we used TSMC 0.35-μm typical CMOS parameters with minimum W/L. The power supply voltage was set at 3 V.

Figure 11 shows simulation results of the P-cell circuit. We assumed two fishes (F1 and F2) generated their own EODs (S_1 and S_2) as

$$S_1 = \sin(2\pi f_1 t), \tag{1}$$

$$S_2 = \sin(2\pi f_2 t), \tag{2}$$

where f_1 and f_2 were set at 1 MHz and 1.04 MHz, respectively ($\Delta f_{21} > 0$). F1 accepts interfered input I_{in} as

$$I_{\mathrm{in}} = I_0 S_1 + I_1 S_2, \tag{3}$$

where I_0 and I_1 were set at 1 μA and 0.5 μA, respectively, to emulate the interference. Figure 11(a) shows the interfered input current ($I_{\rm in}$). Outputs of the P-cell circuit ($I_{\rm Pout}$) are shown in Fig. 11(b) where $I_{\rm ref}$ of the P-cell circuit was set at 0.54 μA. Spike clusters in the dashed ellipses in the figure are enlarged in Figs. 11(c) and (d). Figure 12 shows the number of spikes (spike counts) versus time having the same time scale as in Fig. 11(a), which indicated that the spike counts per each cluster was increased (or decreased) when the amplitudes of $I_{\rm in}$ was high (or low), *i.e.*, pulse-density modulation required for P-cell operations is realized by the proposed P-cell circuit.

Figure 13 shows simulation results of the T-cell circuit. We simulated two T-cell circuits simultaneously with setups illustrated in Fig. 10. Bias current $I_{\rm ref}$ of each T-cell circuit was set at 0.1 μA. Figures 13(a) and (c) show the interfered input current detected at position A ($\equiv I_{\rm in,A} = I_0S_1 + I_1S_2$) and no-interfered current detected at position B ($\equiv I_{\rm in,B} = I_0S_1$), respectively. Outputs of the T-cells ($I_{\rm Tout,A}$ and $I_{\rm Tout,B}$) were plotted in Figs. 13(b) and (d), which represented that the output spikes were generated only when the input current had a certain phase ($\approx \pi(2n+1)$, n: integer). Figures 13(e) and (f) shows enlarged spike clusters in dashed rectangles in Figs. 13(b) and (d). The inter-spike intervals, *i.e.*, $t_{\rm A} - t_{\rm B}$ in Figs. 13(e) and (f), were calculated at every n, and output spikes at $n = 4$ and 20 were plotted in the figures. Figure 14 shows the inter-spike intervals versus time (n) having the same time scale as in Figs. 13(a) to (d). The positive (or negative) intervals represent that the phase is lagged (or led).

Now let us see the operations of frequency comparison between S_1 and S_2, by integrating the outputs of the P- and T-cell circuits. Figure 15(a) plots spike counts in Fig. 12 versus inter-spike intervals in Fig. 14. As time increases, the plot (black circles) rotated on the 2-D plane counterclockwise, and the orbit draw a closed ellipse, which indicated $\Delta f_{21} > 0$, as explained in Sect. 2. Indeed, Δf_{21} was set at 40 kHz (> 0) in our setups. In contrast, when f_1 and f_2 were set at 1 MHz and 0.96 MHz ($\Delta f_{21} < 0$), respectively, the plot rotated on the plane clockwise, as shown in Fig. 15(b). Therefore, by integrating outputs of P- and T-cell circuits, one can discriminate the sign of the frequency difference

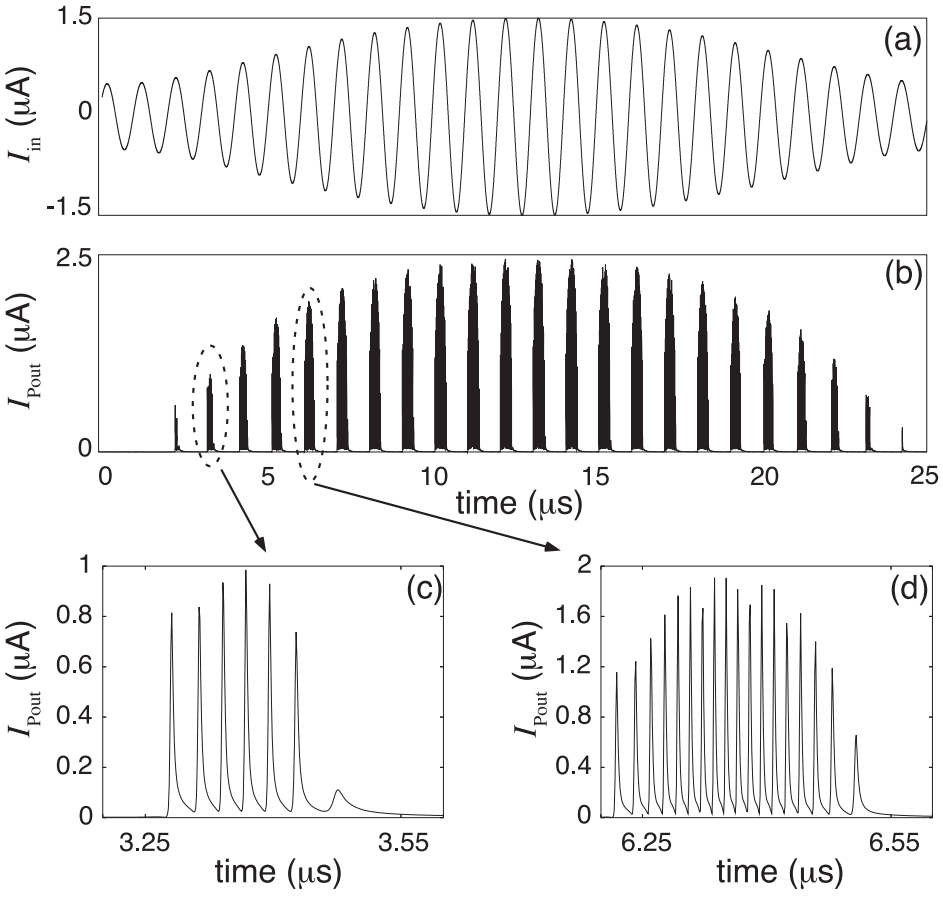


Fig. 11. Raw spike outputs of P-cell circuit.

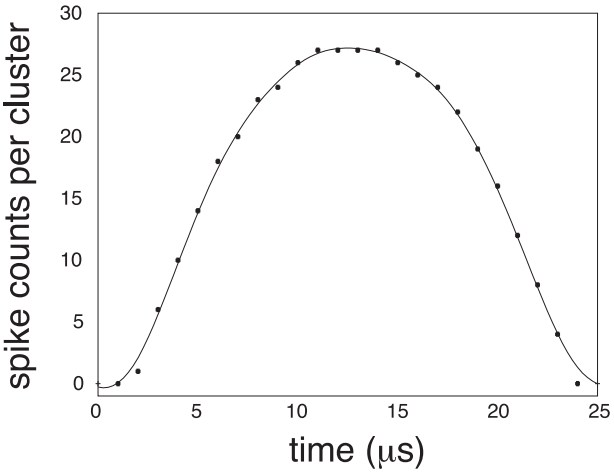


Fig. 12. Spike counts within EOD period.

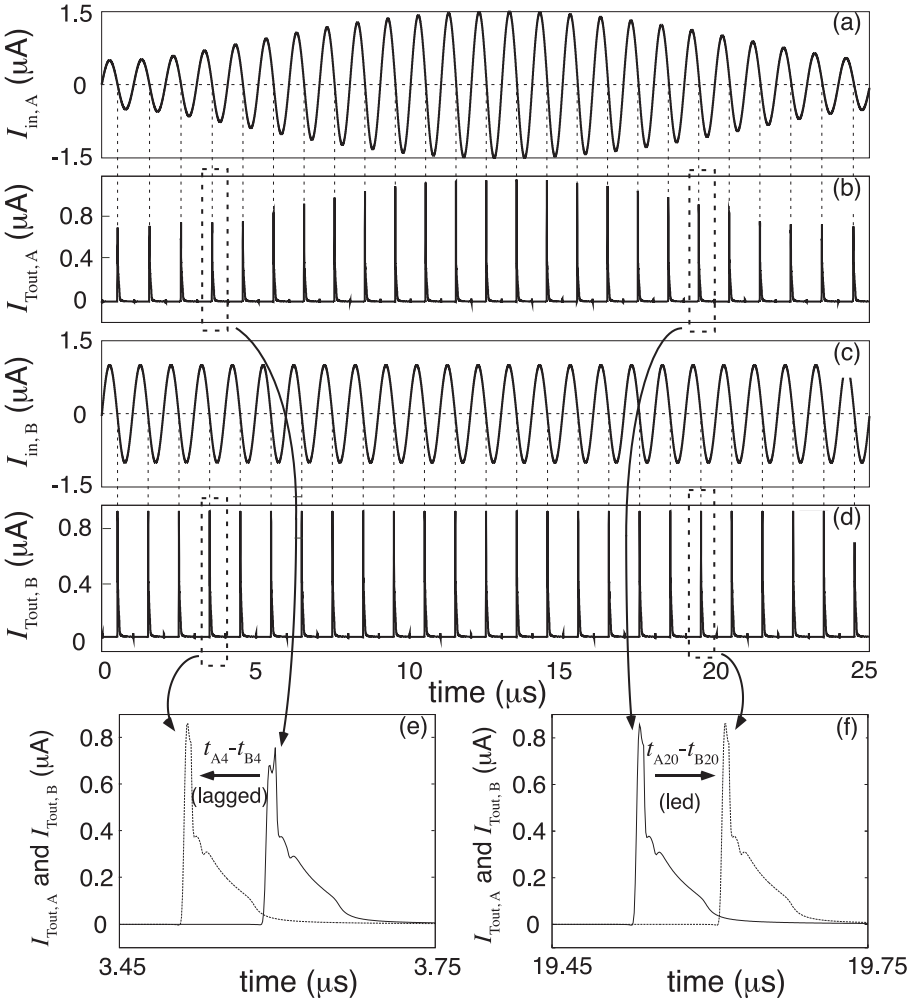


Fig. 13. Raw spike outputs of T-cell circuit.

by the rotating direction.

Simulation results of the E-cell circuit is shown in Fig. 16(a). The simulation was conducted by applying P-cell's output spike currents (I_{Pout}) shown in Fig. 11, to the E-cell circuit (connections between the P- and E-cell circuit is illustrated in Fig. 10). Bias current I_{ref} of the E-cell circuit was set at 0.5 nA. The circuit generated spikes (as several spike clusters) only when the amplitude of the P-cell's input (I_{in} in Fig. 11) were increasing, as expected. Figures 16(b) and (c) shows enlarged plots of the second and the fourth spike clusters. Figure 17 plots the number of spikes in the clusters

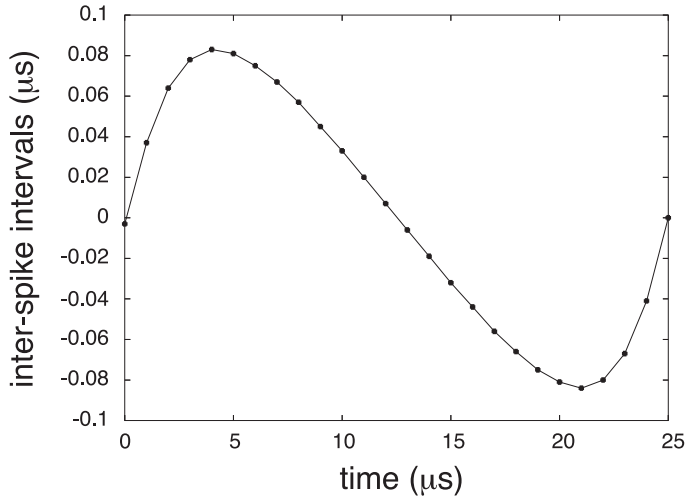


Fig. 14. Inter-spike intervals within EOD period.

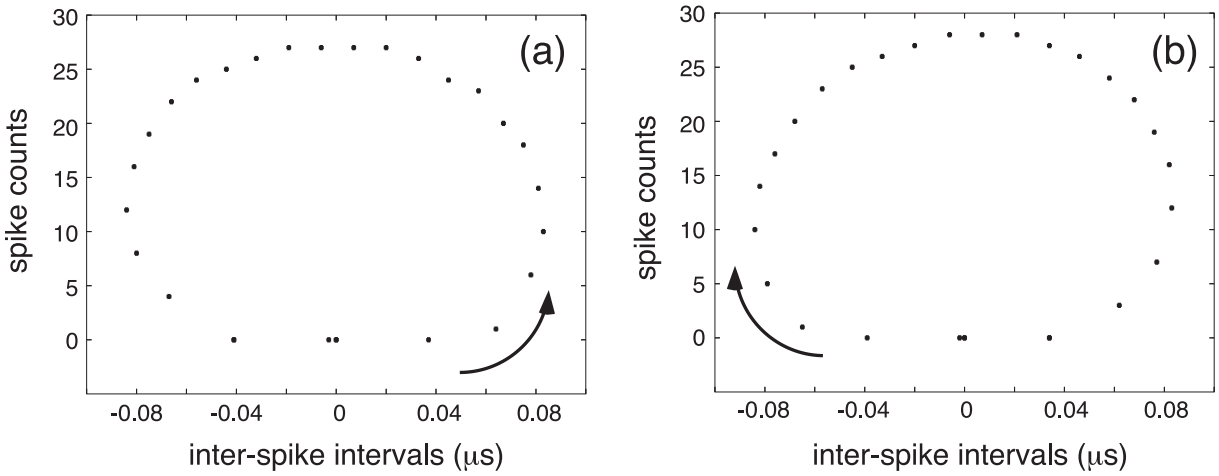


Fig. 15. Spike counts detected by P-cell circuit versus inter-spike intervals calculated from two T-cells; (a) counterclockwise ($\Delta f_{21} > 0$) and (b) clockwise rotation ($\Delta f_{21} < 0$).

within the same time window as in Fig. 16(a), which clearly indicated that the E-cell circuit generated output spikes within a time (3-8 μs) when the amplitude of the P-cell's input was increasing (0-15 μs in this simulation).

Figure 18 represents simulation results of the small-cell circuit shown in Fig. 9(d). The bias current ($I_{\rm ref}$) of the circuit was set at 0.1 μA. As shown in Fig. 10, the small-cell circuit accepts two current spike inputs ($I_{\rm in1}$ and $I_{\rm in2}$) from the T-cell circuits ($I_{\rm Tout,A}$ and $I_{\rm Tout,B}$). For simplicity, we here used ideal current spikes (amplitude: 1 μA, pulse width: 5 ns) instead of $I_{\rm Tout,A}$ and $I_{\rm Tout,B}$ in Fig. 13. The inter-spike intervals of the input spikes ($I_{\rm Tout,A}$ and $I_{\rm Tout,B}$) are plotted in Fig. 18(a). Figure 18(b) shows spike outputs of the small cell circuit ($I_{\rm Sout,A}$) for the input spikes ($I_{\rm in1} = I_{\rm Tout,B}$ and $I_{\rm in2} = I_{\rm Tout,A}$, which corresponds to "small cell 1" in Fig. 10). The circuit generated spikes when the inter-spike interval was positive. Figure 19 plots the dependence of spike amplitude $|I_{\rm Sout,A}|$ on the inter-spike intervals, which indicated the response time window of the small-cell circuit was about 0.04 μs with the given parameter sets. On the other hand, when we connected $I_{\rm in1}$ and $I_{\rm in2}$ to $I_{\rm Tout,A}$ and $I_{\rm Tout,B}$, respectively, the circuit generated spikes when the ISI was negative, which corresponds to the required operations of "small cell 2" in Fig. 10.

Finally, we show simulation results of the whole network circuits including the sign-selective circuits. In the simulations, we combined all the proposed circuits (P-, T-, E-, small- and sign-selective cell

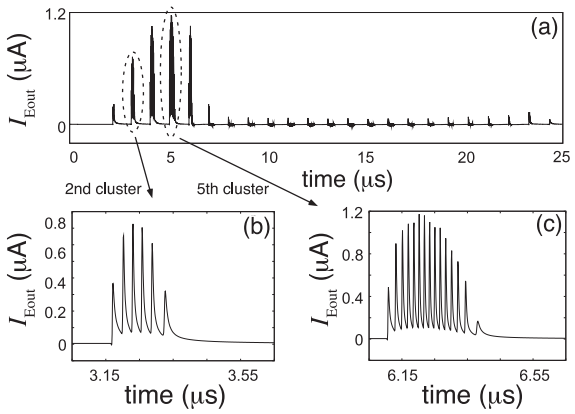


Fig. 16. Transient response of E-cell circuit.

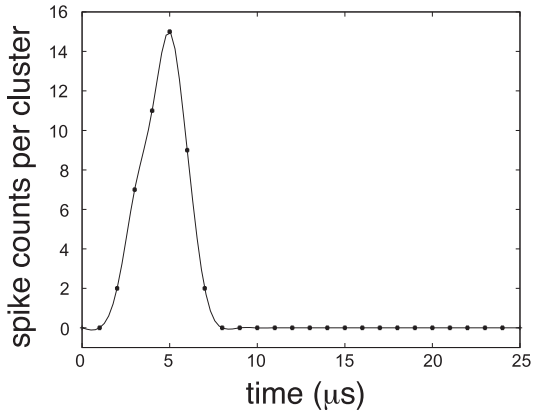


Fig. 17. E-cell's spike counts per cluster.

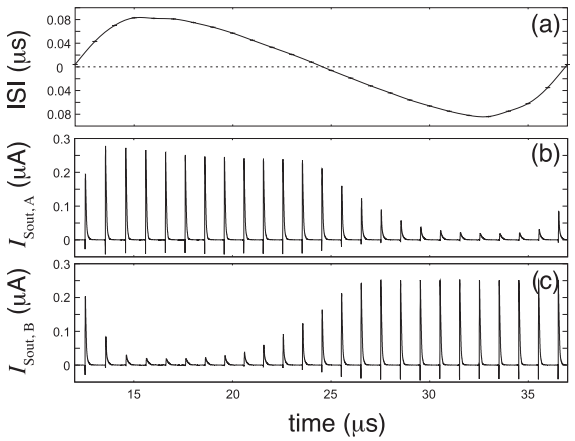


Fig. 18. Transient response of small-cell circuit.

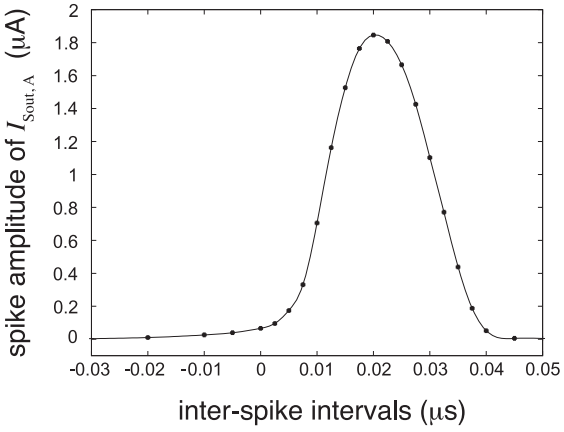
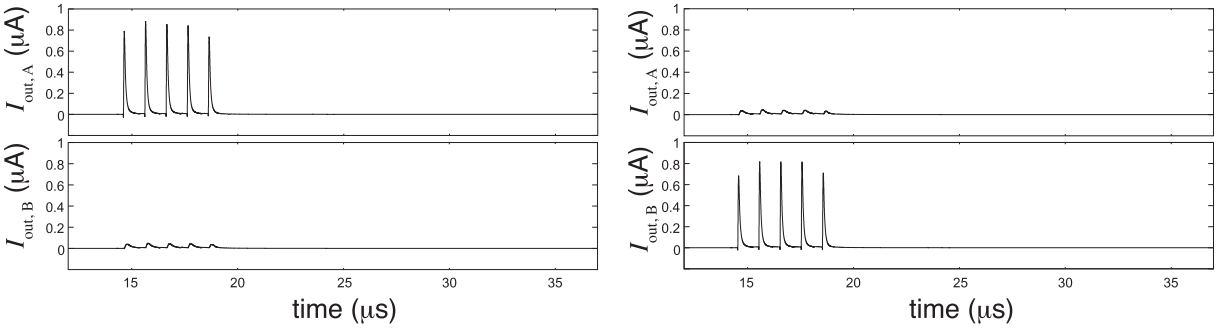


Fig. 19. Amplitudes of small cell's output spikes versus inter-spike intervals of input spikes.



(a) $\Delta f_{21} > 0$.

(b) $\Delta f_{21} < 0$.

Fig. 20. Outputs of sign-selective cell circuits; (a) $\Delta f_{21} > 0$ and (b) $\Delta f_{21} < 0$.

circuits) and constructed a network circuit shown in Fig. 10. The bias currents of the sign-selective circuit were set at 10 nA. Figure 20(a) shows the results for Δf_{21} = 40 kHz (f_1 and f_2 were set at 1 MHz and 1.04 MHz, respectively). In this case, "sign-selective cell 1" generated output spikes, whereas "sign-selective cell 2" did not. On the other hand, when f_1 and f_2 were set at 1 MHz and 0.96 MHz, respectively (Δf_{21} = -40 kHz), "sign-selective cell 1" did not generate output spikes, but "sign-selective cell 2". These results indicated that "sign-selective cell 1" fires when $\Delta f_{21} > 0$, while "sign-selective cell 2" fires when $\Delta f_{21} < 0$. Through extensive SPICE simulations, we roughly estimated the minimum "detectable" frequency difference $\Delta f_{21,\min}$ by the proposed circuit as 10 kHz, with the given parameter sets (when $|\Delta f_{21}| < 10$ kHz, amplitude of "sign-selective cell 1" ($I_{\mathrm{out,A}}$) in Fig. 20 approached to that of "sign-selective cell 2" ($I_{\mathrm{out,B}}$), which result in hard distinction of the

sign of Δf_{21}).

Our circuit was designed so that it can operate in its own way under noisy environment, *i.e.*, noise and fluctuations as well as small device mismatches do not affect the circuit's qualitative behavior, but they do affect the quantities such as the detectable frequency limit, minimum detectable frequency difference, and so on. Of course the same thing happens in real neural systems. As long as designing functional circuits based on the neuromorphic approach, such a problem (hard to define clear specifications with quantity) follows these circuits. When computationally-rich functions, *e.g.*, perception, decision, inference and so on, that may hide the problem are performed on a neuromorphic circuit, its value would significantly be increased.

5. Summary

We designed a neuromorphic CMOS frequency comparator based on a neural network model of jamming-avoidance response (JAR) of *Eigenmannia* [1]. The network model consists of five elementally cells, *i.e.*, P-, T-, E-, small- and sign-selective cells. We have already implemented P- and T-cells on analog CMOS circuits in [7]. In this paper we implemented the rest three cells (E-, small- and sign-selective cells), and constructed a neural network circuit by combining all the cell circuits. Through SPICE simulations we demonstrated that the network circuit could detect the input frequency difference.

The performance of the proposed frequency comparator is of course poor as compared with present (digital-based) phase frequency comparators for phase-locked or delay-locked loops, in terms of the precision and operating frequencies. Therefore the performance comparison between the proposed and present CMOS system is meaningless. But it should be noted that the proposed frequency comparator is a "spin off" circuit of our project to implement whole neural network structure of *Eigenmannia*, and the final goal is to create artificial life based on the neuromorphic approach [2, 4]. Indeed, outputs of all the five cells are forwarded not only to the neural area of JAR, but also to the other area of *Eigenmannia*'s small brain [1]. Therefore hardware implementation of those cells are necessary for constructing the whole brain system of *Eigenmannia*. Although understanding human brain and and recreating it on silicon devices looked over ambitious so far, we may understand small brains of lower animals and reconstruct it on silicon devices in the near future.

Acknowledgments

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